IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), September 2019.
Invited presentation 2-DI-I-1 given at ISEC, 28 July-1 August 2019, Riverside, USA.

CRAVITY AIST

Japanese activities for superconducting circuits using flip-chip configurations

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National Institute of Advanced Industrial Science and Technology (AIST)

The author would like to thank for Y. Hashimoto, H. Suzuki, K. Makise, M. Maruyama, H. Nakagawa and AIST colleagues for supplying useful data.

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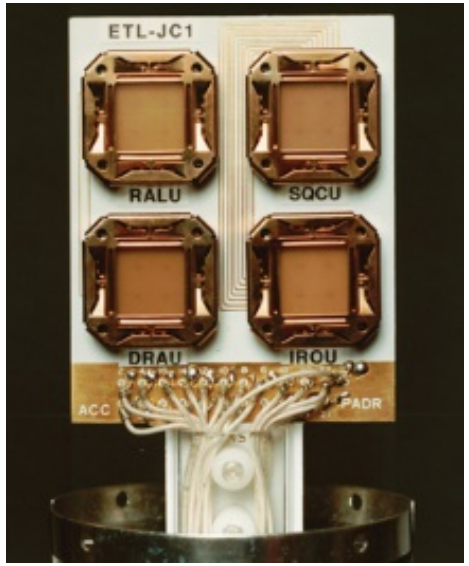
Introduction

- Extractions of high-speed performance from superconducting digital circuits to room temperature essentially require multi-chip module (MCM) using flip-chip configurations.
- Many efforts have been devoted to develop the superconducting MCM technologies for nearly 30 years in Japan.
- Recently, the flip-chip configurations enter the spotlight in superconducting quantum computing. Because it is required that qubits have to be separated from noise sources as far as possible, the flip-chip configurations are convenient to separate qubits from noisy peripheral components.
- This presentation will show Japanese activities regarding superconducting MCM using flip-chip-configurations.
  - Digital circuits
  - Quantum devices

Kyocera-ETL 1993

ETL-JC1 1991

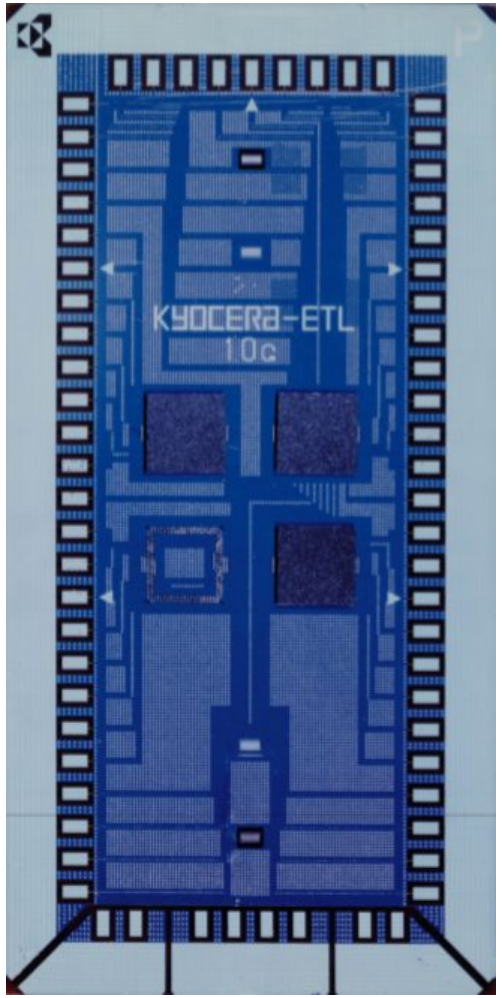


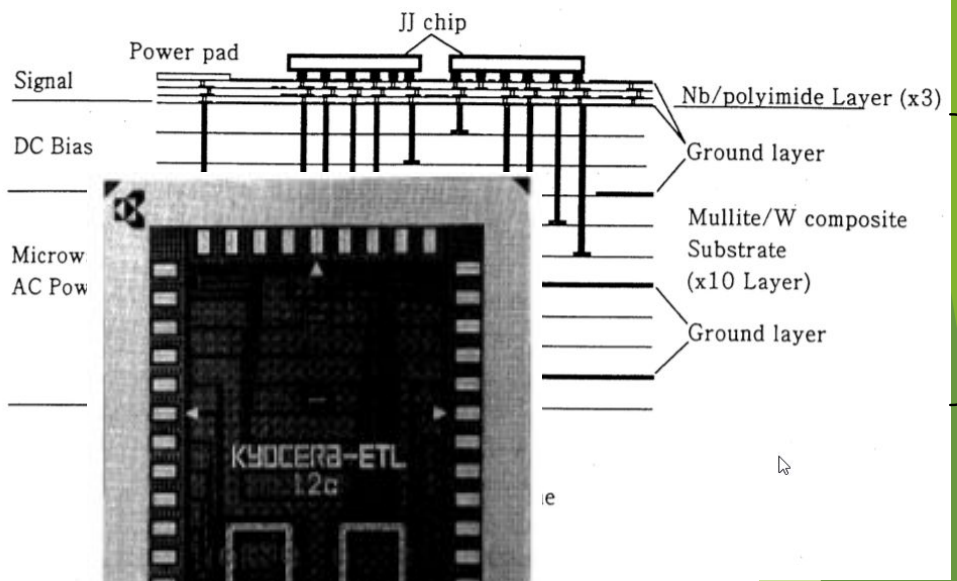
ETL developed the first Josephson computer

To fully exploit high-speed characteristics of each chip

⇩

Multi-chip-module





Chip measurements were failed

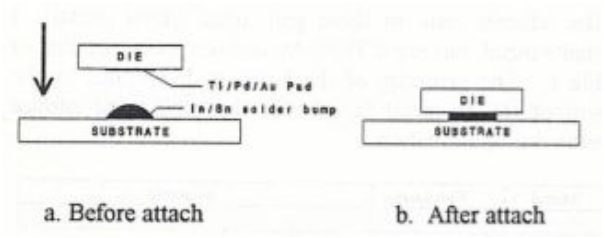
S. Takahashi, T. Kubo, K. Kawabata, R. Jikuhara, G. Kaji, M. Terasawa, H. Nakagawa, M. Aoyagi, I. Kurosawa, and S. Takada, Jpn. J. Appl. Phys., 1993, pp. L898-L900

Low-frequency test of flip-chip configuration

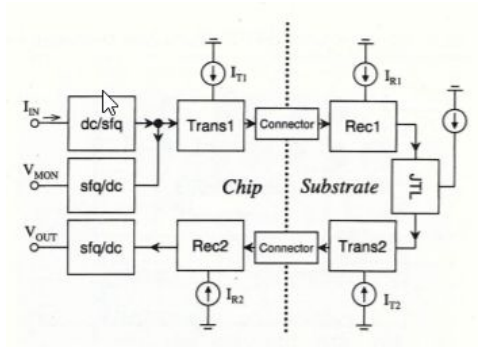
ETL=AIST

2000

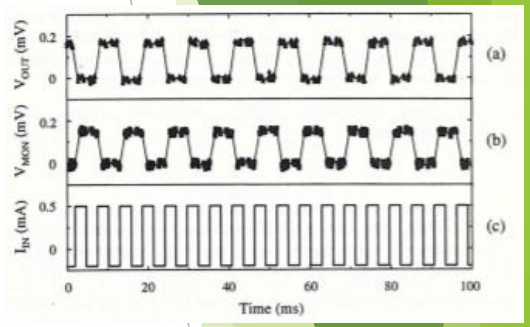
TRW



K. E. Yokoyama, G. Akerling, A. D. Smith, and M. Wire,
IEEE Trans. Appl. Superconductivity, 1997, pp. 2631-2634.

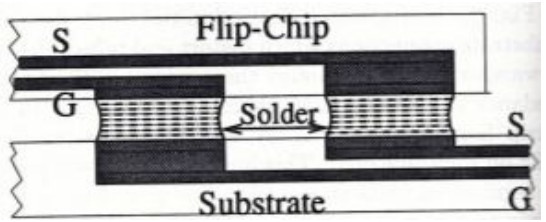


Block diagram of chip-to chip communication experiments

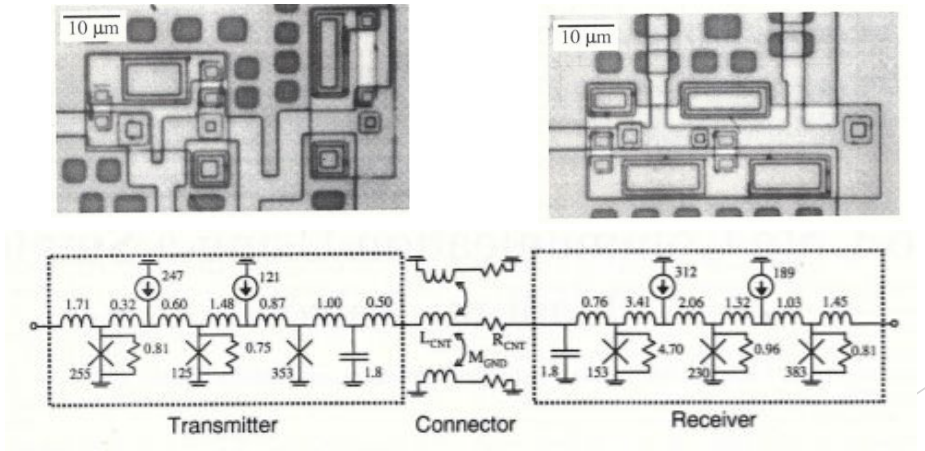


Demonstration of chip-to-chip propagation of SFQ pulses

SUNY



S. Polonsky, and D. Schneider,
IEEE Trans. Appl. Superconductivity, 1997, pp. 2818-2821.



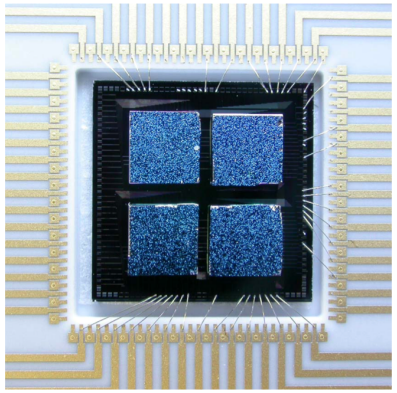
Schematic and microphotograph of SFQ chip-to-chip circuit

M. Maezawa, H. Yamamori, and A. Shoji, IEEE Trans. Appl. Superconductivity, 2000, pp. 1603-1605.

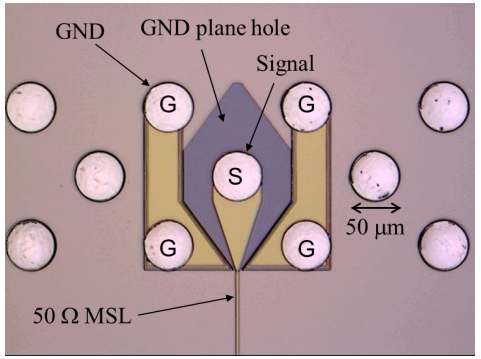
Confirmed SFQ pulse chip-to-chip transfer based on MCM scheme at low frequency

High-frequency test of flip-chip configuration

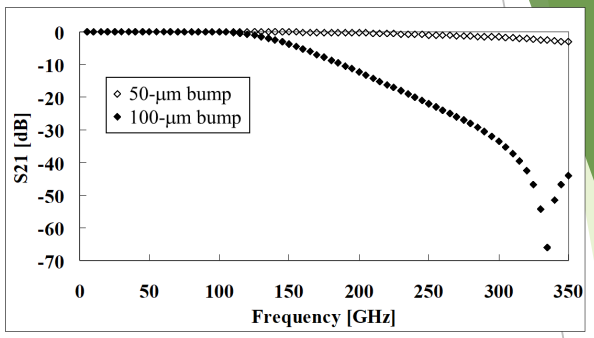
ISTEC **2005**



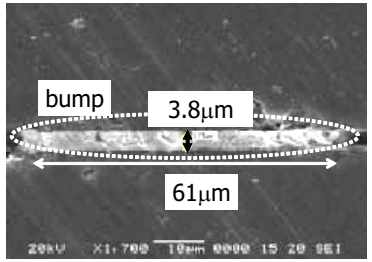
Flip-chipped four chips



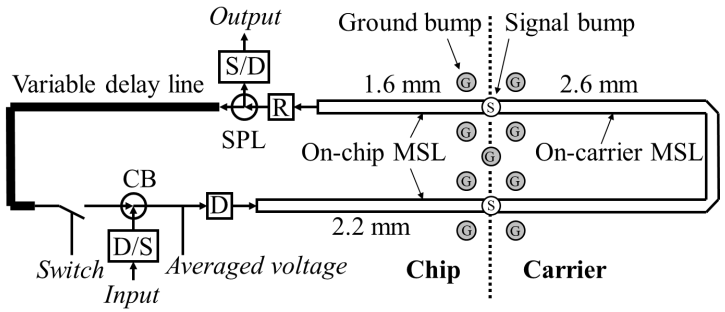
Impedance design of MCM bumps



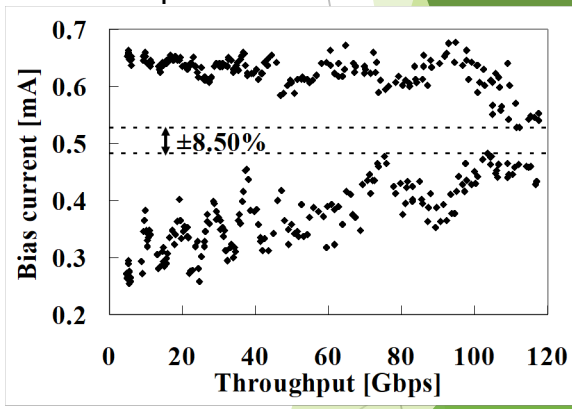
S21 dependence on bump diameter



Cross-section of 50 μmϕ flip-chipped sample



Schematic diagram of SFQ pulse transfer experiments through flip-chip configuration



Operation region on frequency of SFQ pulse transfer

SFQ pulse transfer through flip-chip configuration was confirmed up to 117 Gbps.

Error rate measurement
- Junction voltage was checked every 500 ms while circuit operated at 117 Gbps
- No error was detected for 8 hours
  → Error rate < 10^{-15} at 117 Gbps

Y. Hashimoto, S. Yorozu, T. satoh, and T. Miyazaki, Appl. Phys. Lett., 2005, 022502.

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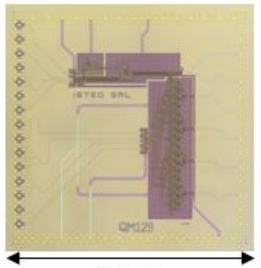
SFQ 4×4 switch system demonstration

ISTEC

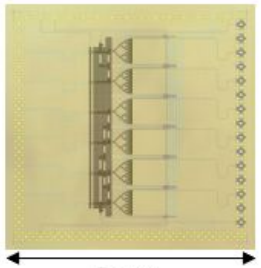
2008

4×4 switch chip



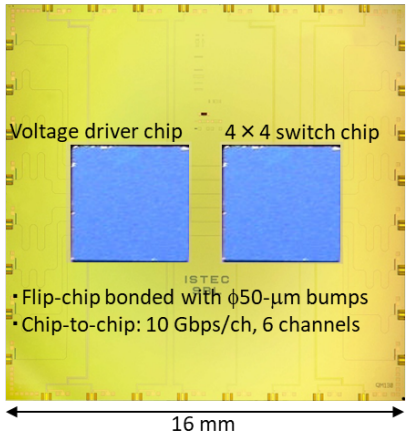
- J_C=2.5kA/cm²
- 2137 JJs
- 264 mA

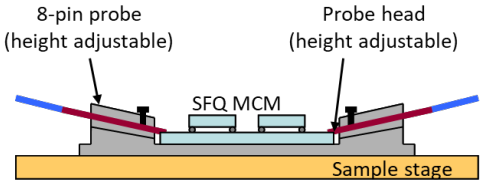
Voltage driver chip

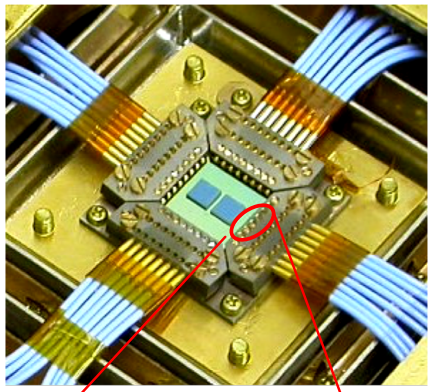


- J_C=10kA/cm²
- 2181 JJs
- 278 mA

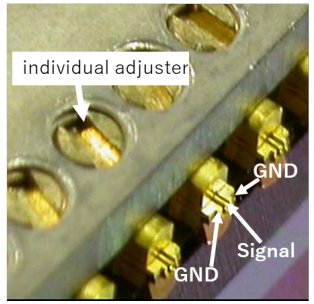
4×4 switch MCM

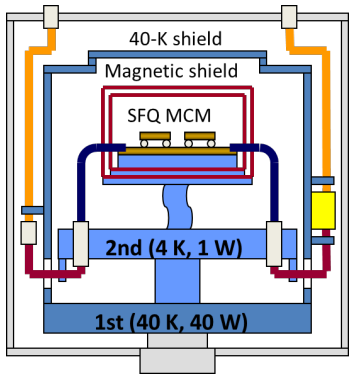






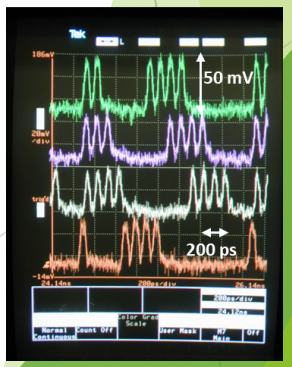
BeCu coplanar probe head





Ethernet switch demonstration

10 Gbps operation
(BER<10^{-12})



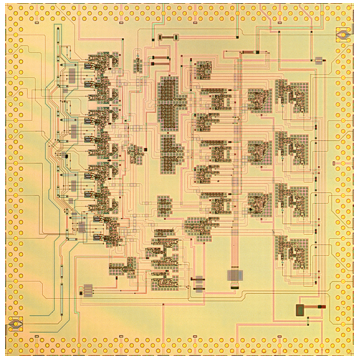
Y. Hashimoto, S. Yorozu, and Y. Kameda, IEICE Trans. Electron., 2008, pp. 325-332
Y. Kameda, Y. Hashimoto, and S. Yorozu, IEICE Trans. Electron., 2008, pp. 333-341.

Optical input demonstration

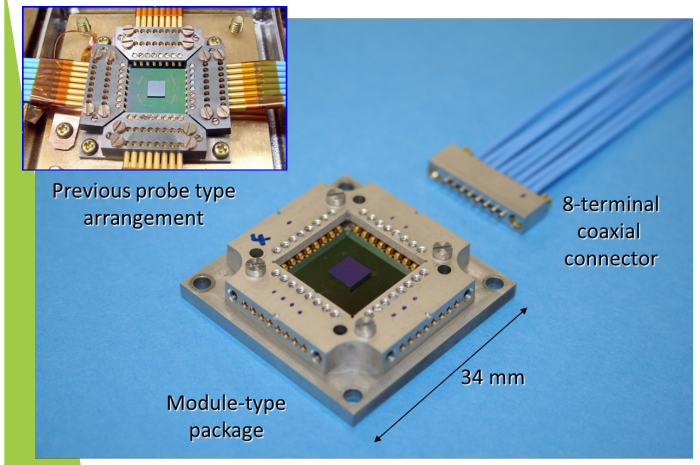
ISTEC

2011

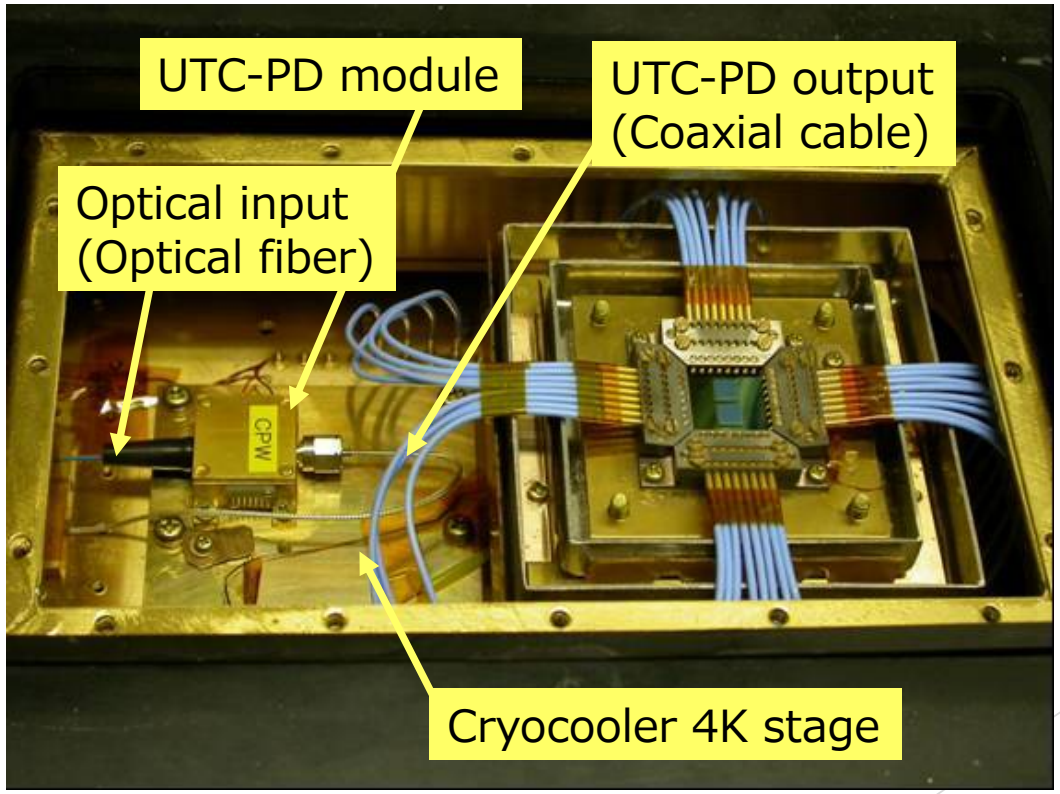
Flush-type ADC chip



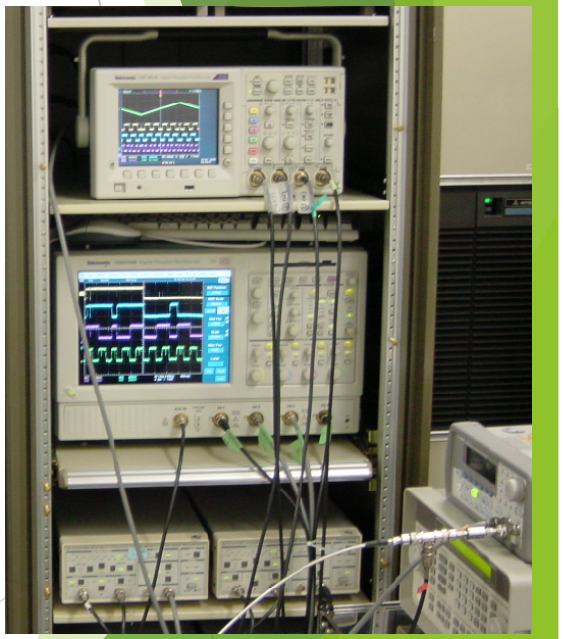
Advanced cryo-package module



Implementation at cryocooler system with UTC-PD



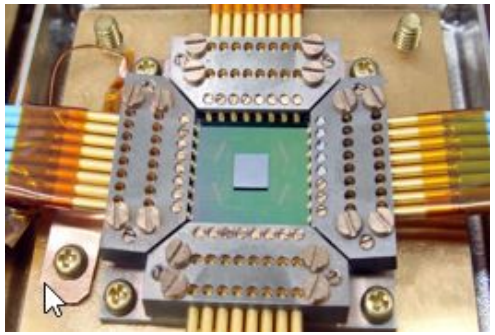
Demonstration of 40 Gbps optical waveform measurement system

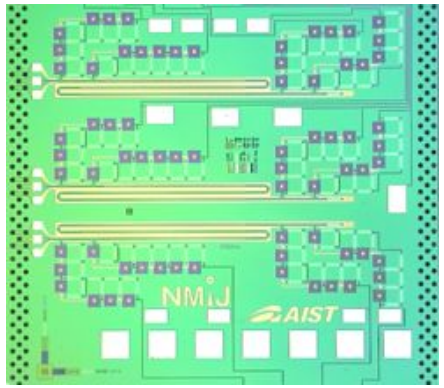


H. Suzuki, M. Oikawa, K. Nishii, K. Ishihara, K. Fujiwara, M. Maruyama, and M. Hidaka, IEEE Trans. Appl. Superconductivity, 2011, pp. 671-676.

Application of flip-chip to an analog device

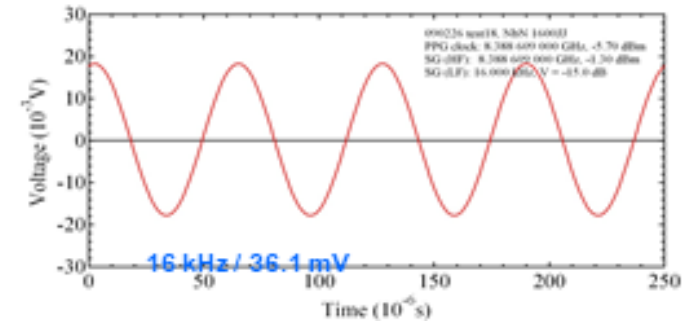
AIST Pulse driven Josephson junction array for AC voltage standard **2010**

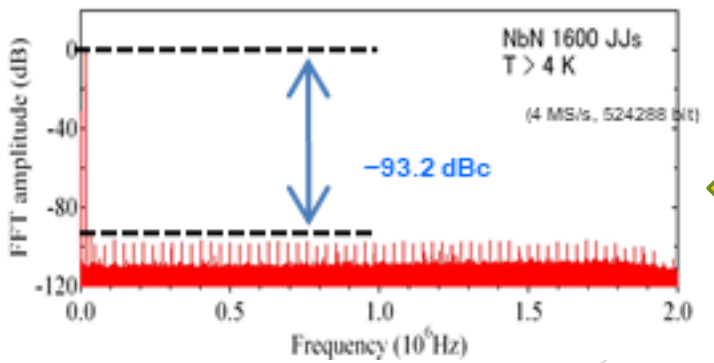




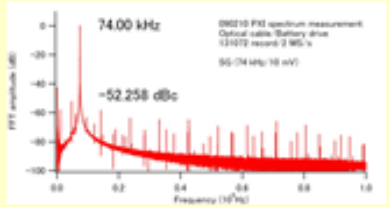
Josephson junction (JJ) array chip

Area of JJ array chip was significantly reduced by separating JJ array and high frequency I/Os on an interposer.





Generated 16 kHz sine wave



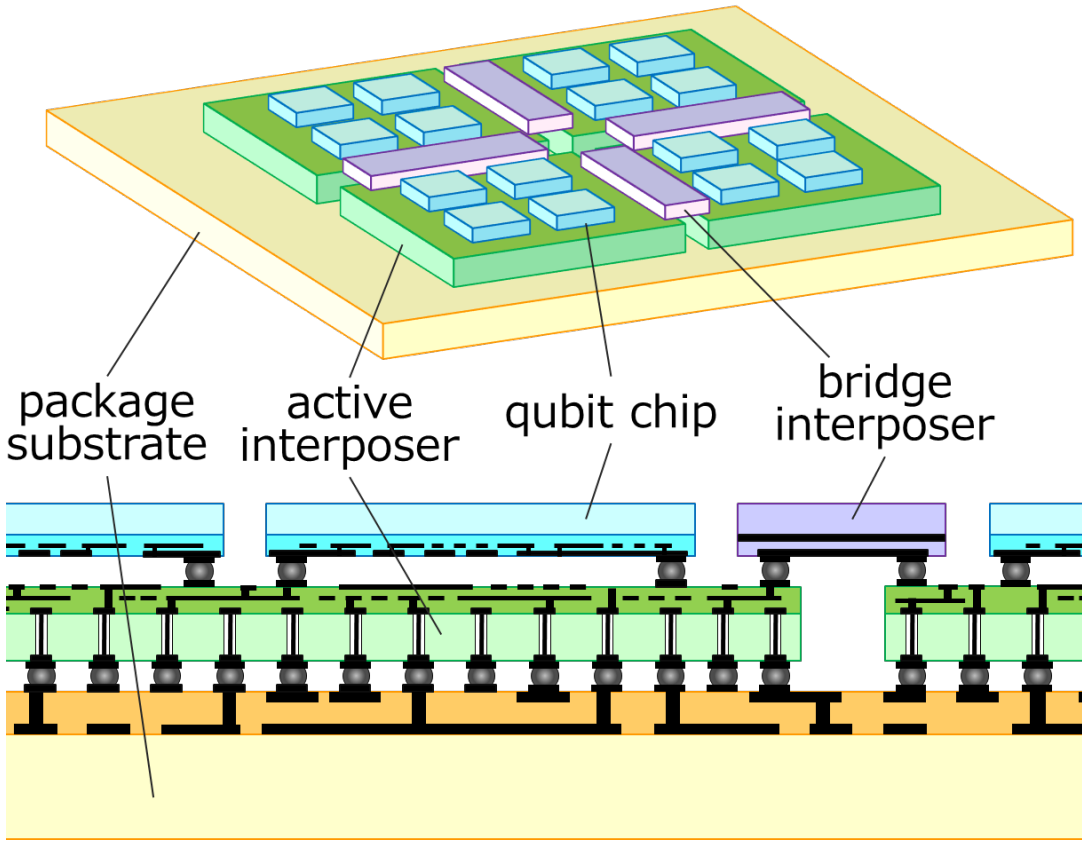
FFT spectrum for a sine wave generated with a commercial signal generator.

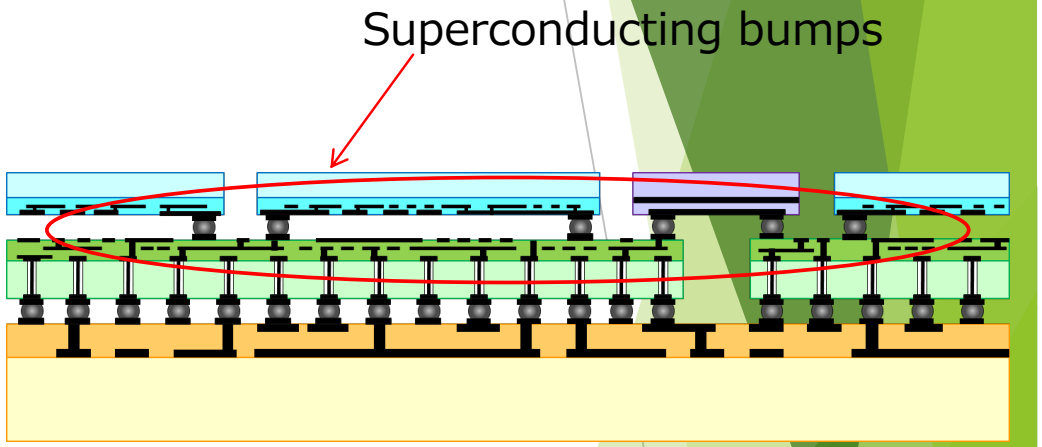
M. Maruyama, C. Urano, N. Kaneko, H. Yamamori, A. shoji, Y. Hashimoto, H. Suzuki, S. Nagasawa, T. Satoh, M. Hidaka, and S. Kiryu, J. of Physics, 2010, 042020.

Towards large scale quantum annealer

AIST

QUbit-chip/Interposer/Package-substrate (QUIP) 2.5D packaging





- **1 million qubits require 16 chips**
- **62,500 qubits / 20 × 20 mm chip**
- **1 qubit : 6400 μm²/bit**

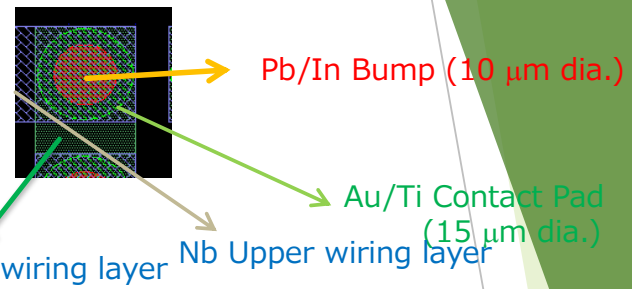
→Over 1000 bump/mm² and alignment margin ± 1 μm

Superconducting connections are essential for the bumps

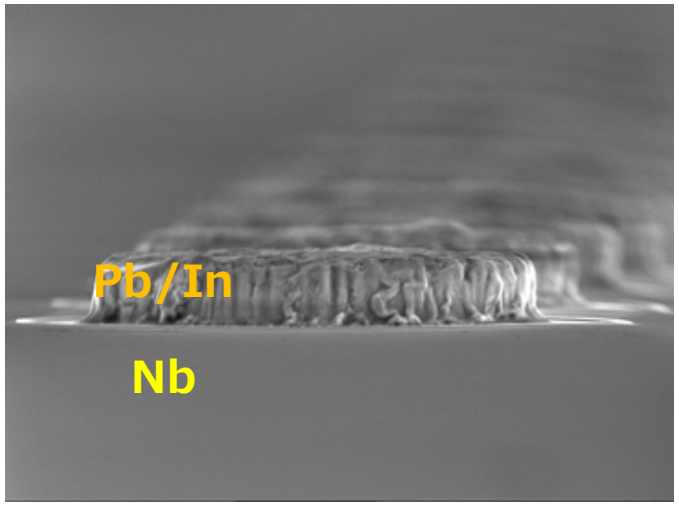
M. Maezawa, G. Fujii, M. Hidaka, K. Imafuku, K. Kikuchi, H. Koike, K. Makise, S. Nagasawa, H. Nakagawa, M. Ukibe, and S. Kawabata, J. Phys. Soc. Jpn., 2019, 061012.

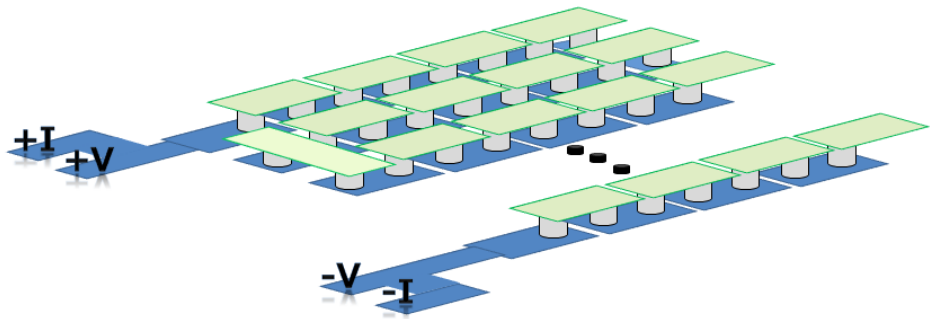
Superconducting bump fabrication

Bump structure



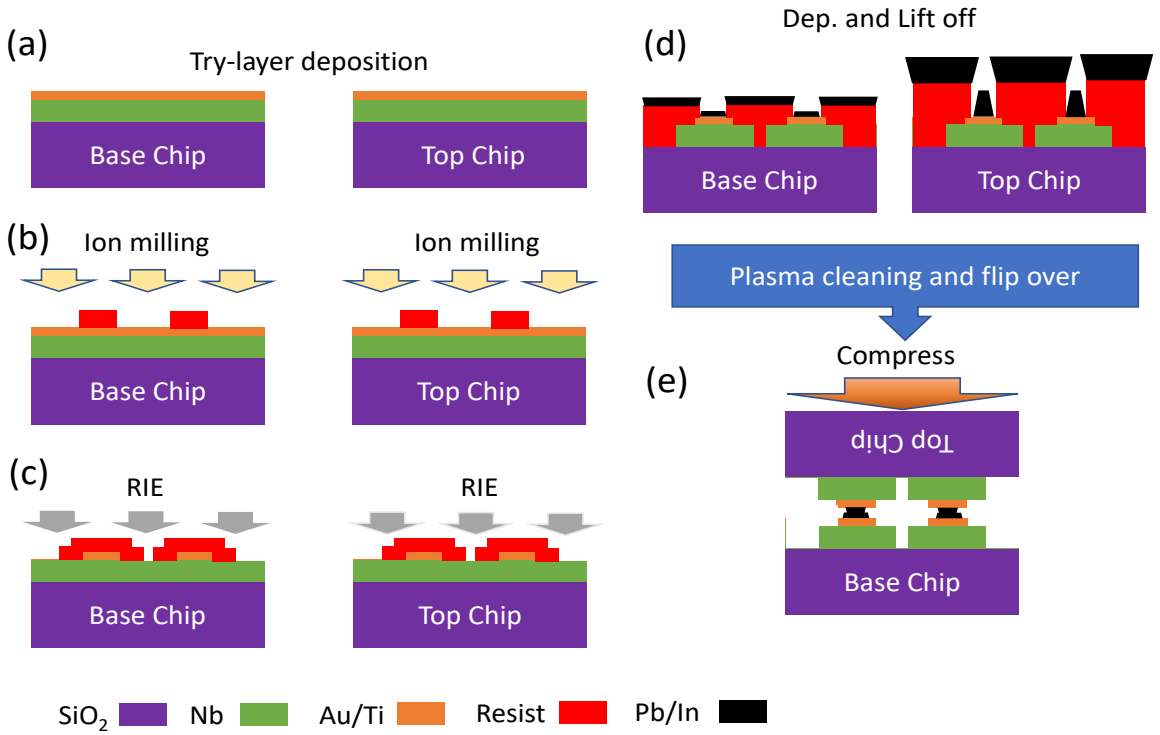
Daisy chain





(~ 1200 bumps/mm²)

Bump fabrication process



K. Makise, M. Maezawa, M. Hidaka, H. Nakagawa, K. Kikuchi, and S. Kawabata, APS spring meeting, 2019.

Summary

- Developments of superconducting MCM in Japan started at early 90's.
- High speed characteristics of SFQ circuits were effectively brought out from SFQ chips to room temperature by the MCMs and a few systems demonstrated their performances.
- AIST succeeded to make flip-chip superconducting connections at 15000 bumps. The MCM technologies become increasingly important for quantum computers.
- The MCM using flip-chip configurations is one of the key technologies to realize superconducting systems in future electrical field.