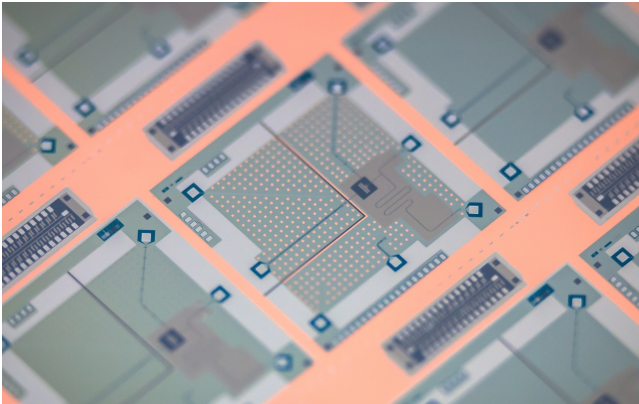
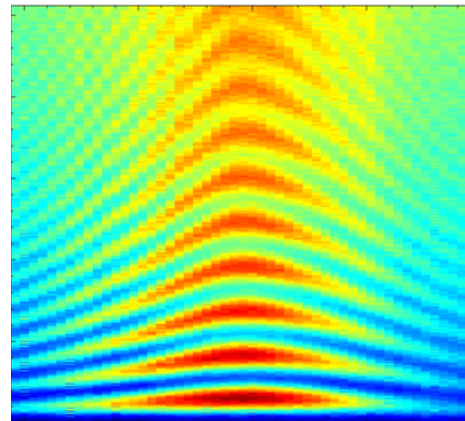
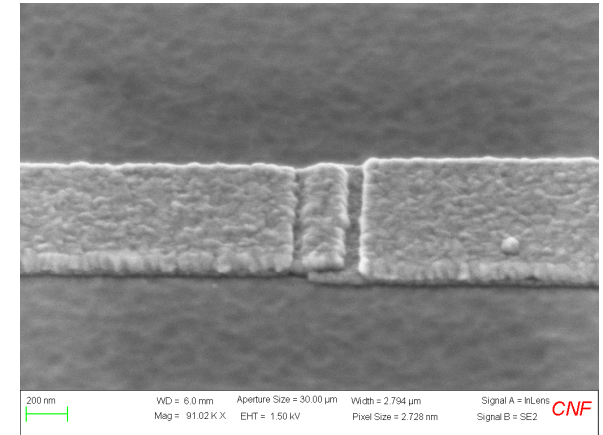


# Cryogenic Control of Coherent Quantum Systems

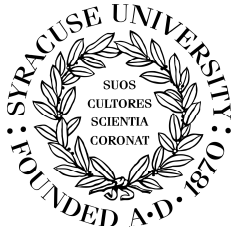


Britton L. T. Plourde  
Syracuse University



Applied Superconductivity Conference  
November 4, 2020

# Acknowledgments



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Patel, I. Pechenezhskiy, M. Vavilov, R. McDermott  
*University of Wisconsin, Madison*



L. Govia, P. Liebermann, E. Pritchett, F. Wilhelm  
*Saarland University*



T. Ohki, *Raytheon BBN Technologies*

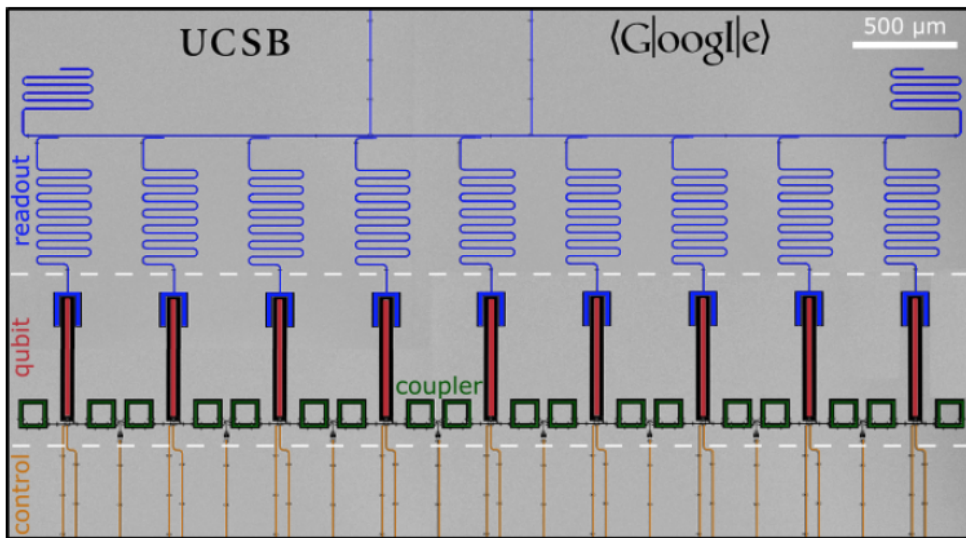
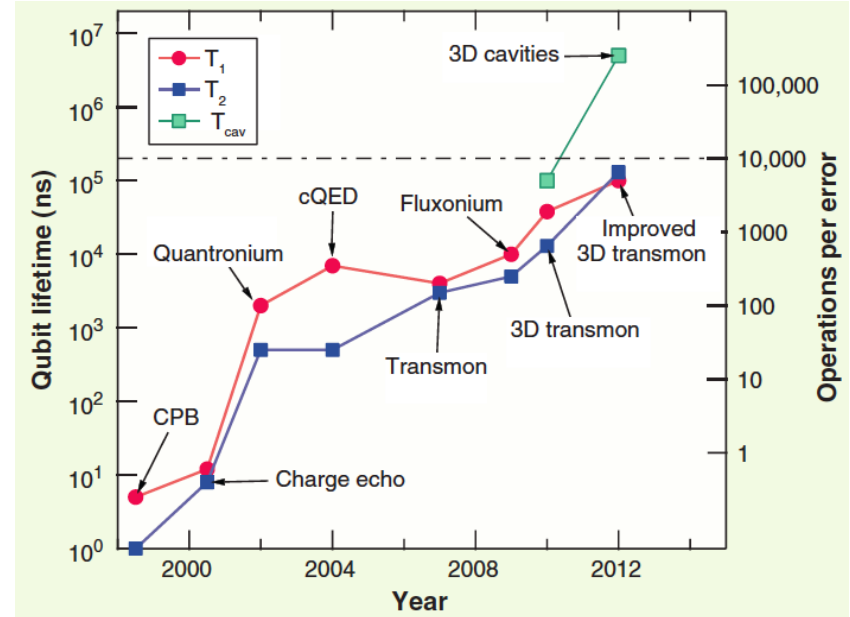
O. Mukhanov *Hypres (SeeQC)*



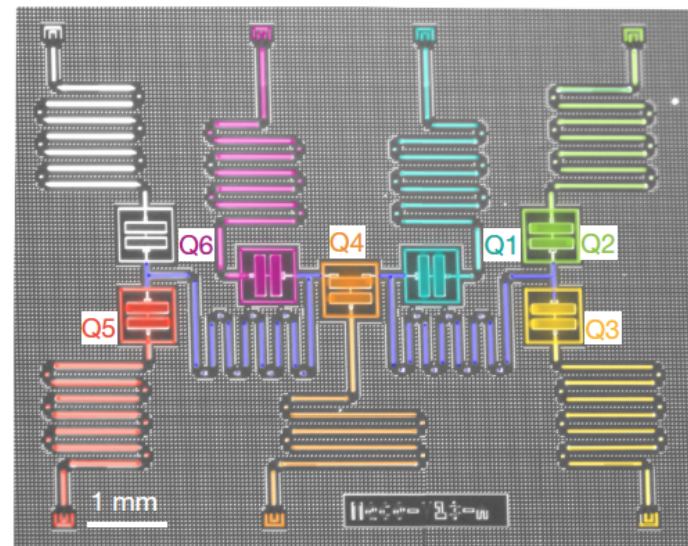
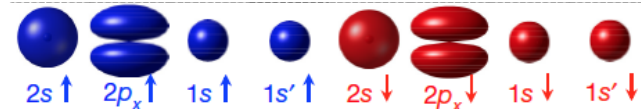
# Superconducting qubits

- $10^5$  improvement in qubit performance
- Promising architecture for quantum information processors

\*Devoret & Schoelkopf (2013)

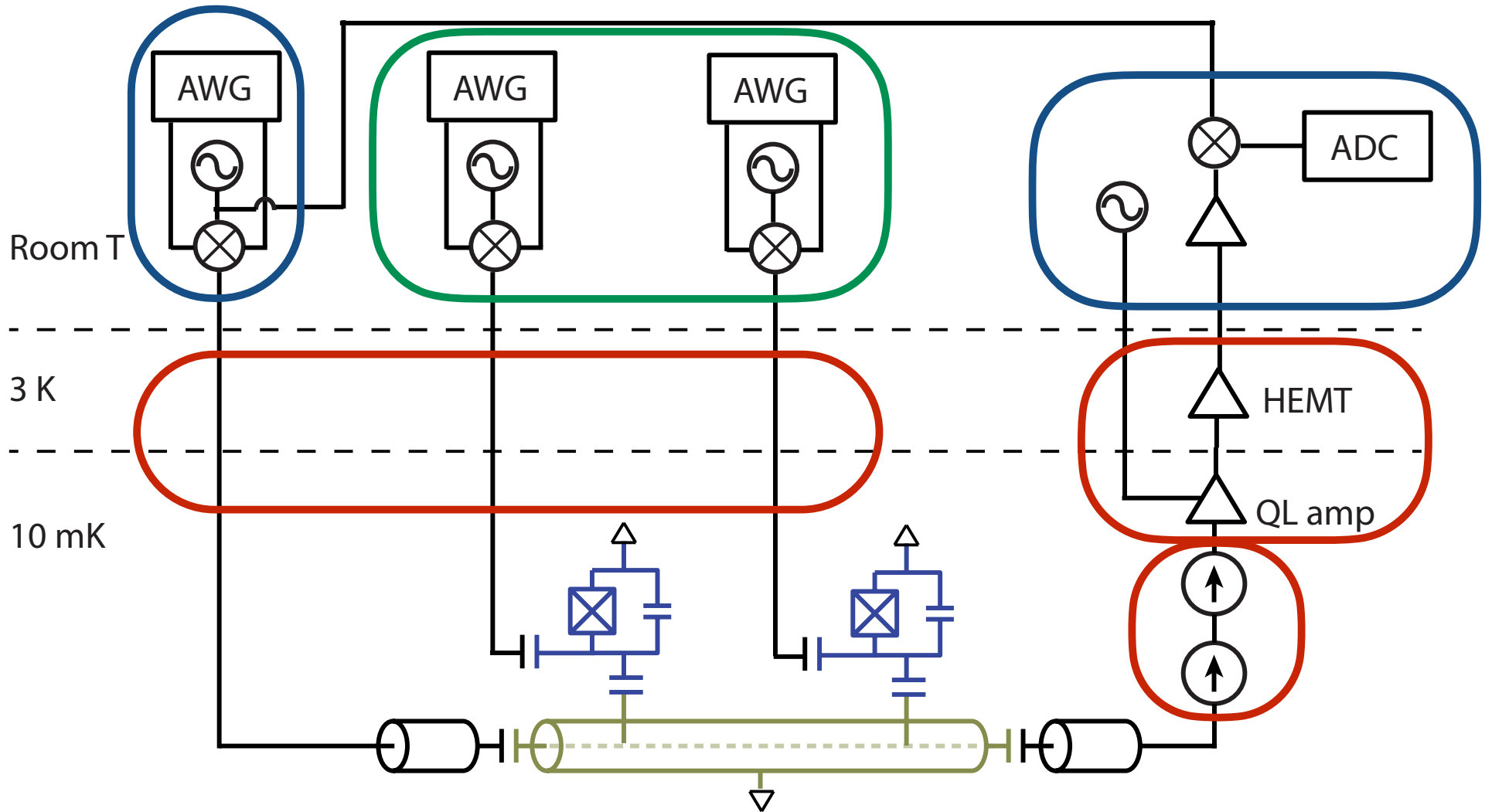


\*C. Neill et al., Science (2018)



\*A. Kandala et al., Nature (2017)

# Microwave-based qubit control and readout



★ Works well..., but significant hardware overhead

*Single-qubit gate fidelities > 99.9%*

\*R. Barends et al., Nature (2014)

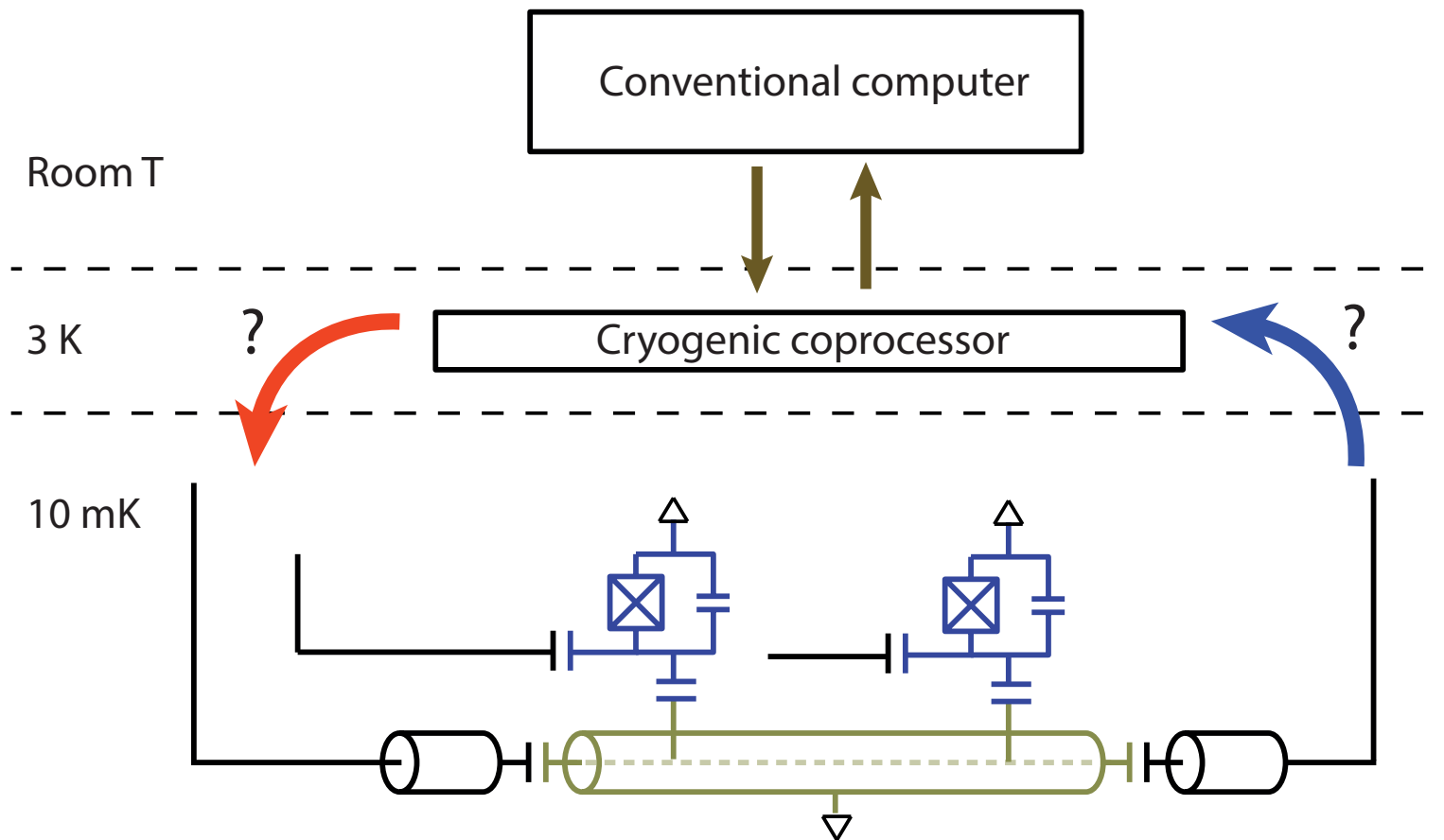
\*S. Sheldon et al. PRA (2016)

*Single-shot readout fidelities > 99% in under 500 ns*

\*T. Walter et al., PR Applied (2017)

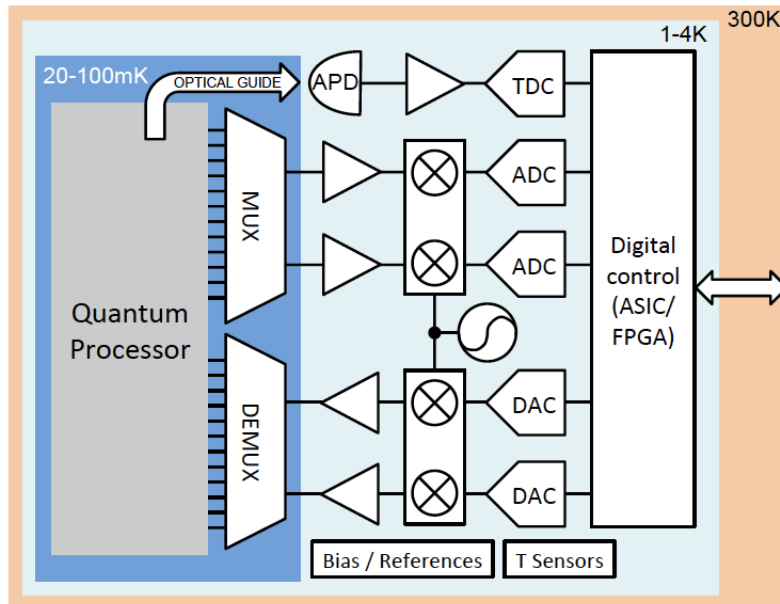
# Reducing room-temperature hardware overhead

- Can we move some of the room-temperature control and readout hardware into the cryogenic environment?
- How can we implement cryogenic control and readout of qubits?

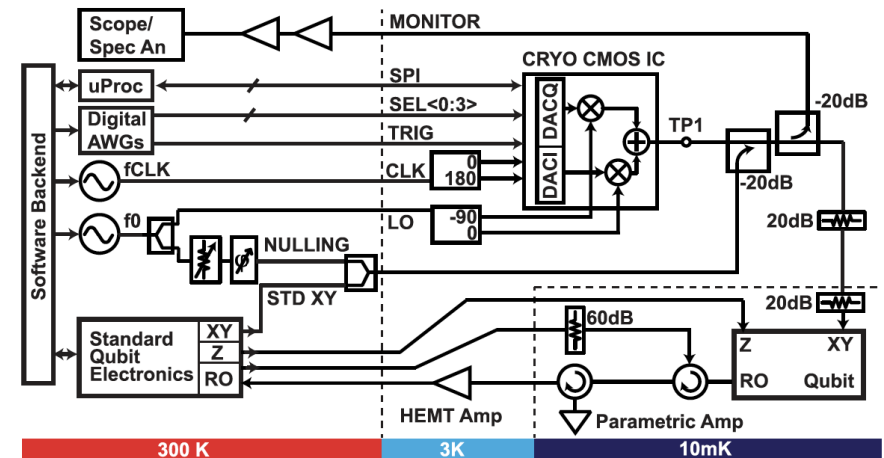
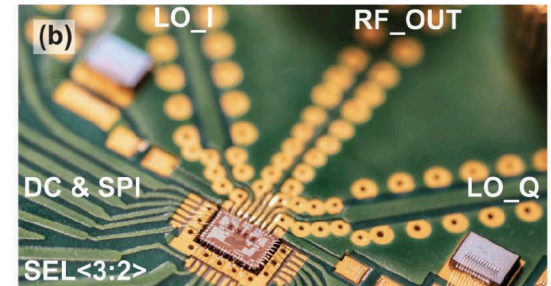


# Cryogenic CMOS and Microwave Control

- One approach: miniaturize some of the room-T hardware and move to the 3 K level
- CMOS-based IQ modulator running at 3 K for generating microwave pulses for qubit gates



\*E. Charbon et al., IEDM (2016)



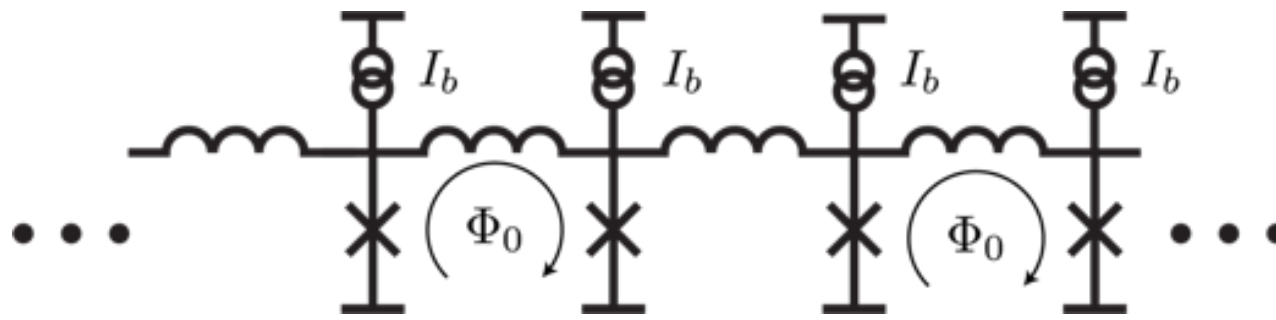
\*J. Bardin et al., IEEE J. Solid State Circuits (2019)

- Besides superconducting qubits, consider integrating semiconductor-based spin quantum dot qubits with cryo CMOS control and readout
- also, Intel, Microsoft...

# Superconducting digital logic

- Classical superconducting digital logic — Single Flux Quantum (SFQ)
- Logical 1 (0) = presence (absence) of propagating fluxon

\*Likharev and Semenov, *IEEE Trans. Appl. Supercon.* 1991



$$\Phi_0 = \frac{h}{2e}$$

- Low power consumption; high speed logic
- Recent intensive effort to implement SFQ-based large-scale processor — IARPA C3 program

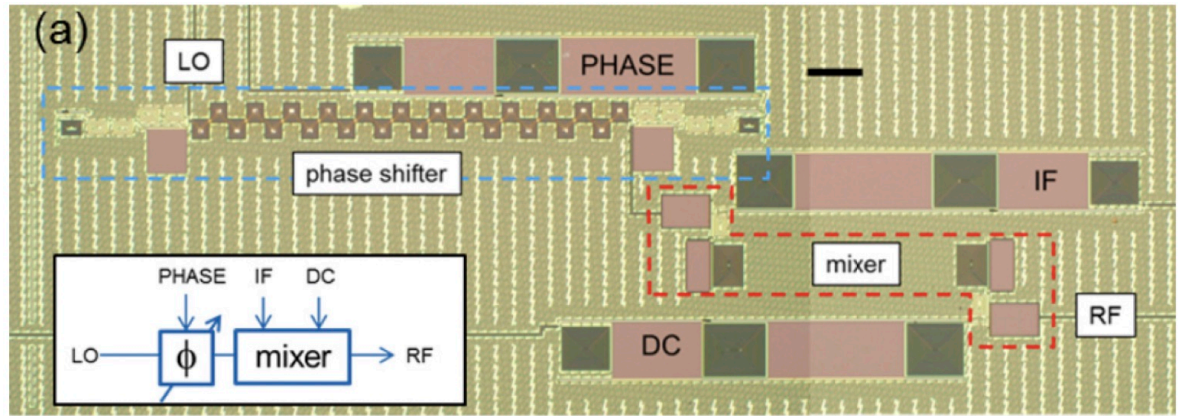
$$\Phi_0 \approx 2 \text{ mV} \times \text{ps}$$

\*Manheimer, *IEEE Trans. Appl. Supercon.* 2015

$$V(t) = \frac{\Phi_0}{2\pi} \frac{\partial \delta}{\partial t}$$

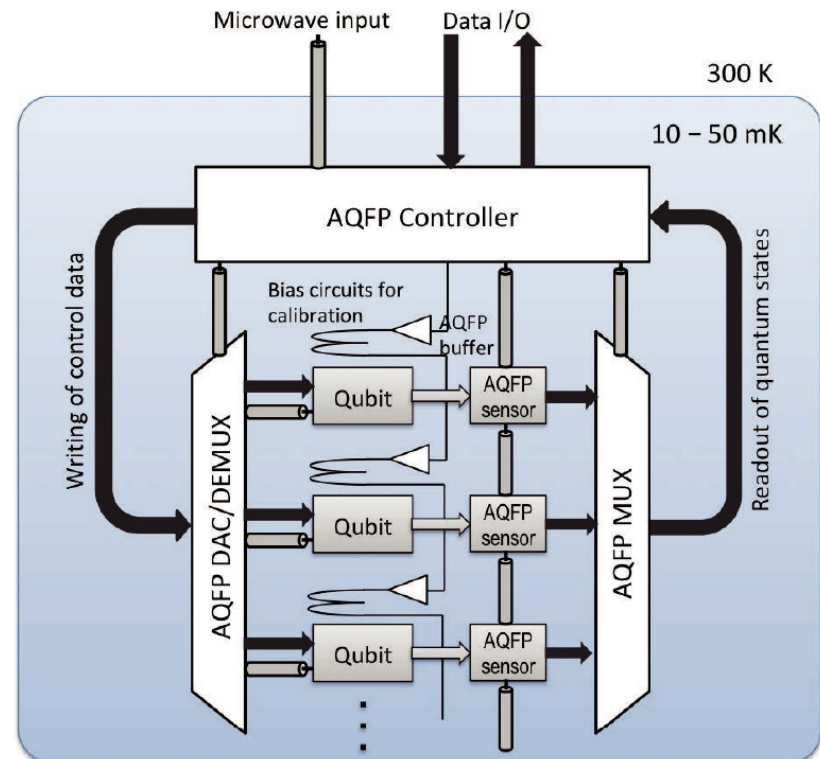
# Superconducting control circuitry for qubits

- JJ-based vector modulator for generating microwave pulses for qubit gates
- Minimal on-chip power dissipation, potential for integrating near qubits



\*O. Naaman et al., *J. Appl. Phys.* (2017)

- AQFP for integrated qubit control and readout at mK stage
- MUX and DEMUX of dc and microwave signals for qubit control/readout
- Potential for low power dissipation of AQFP circuitry

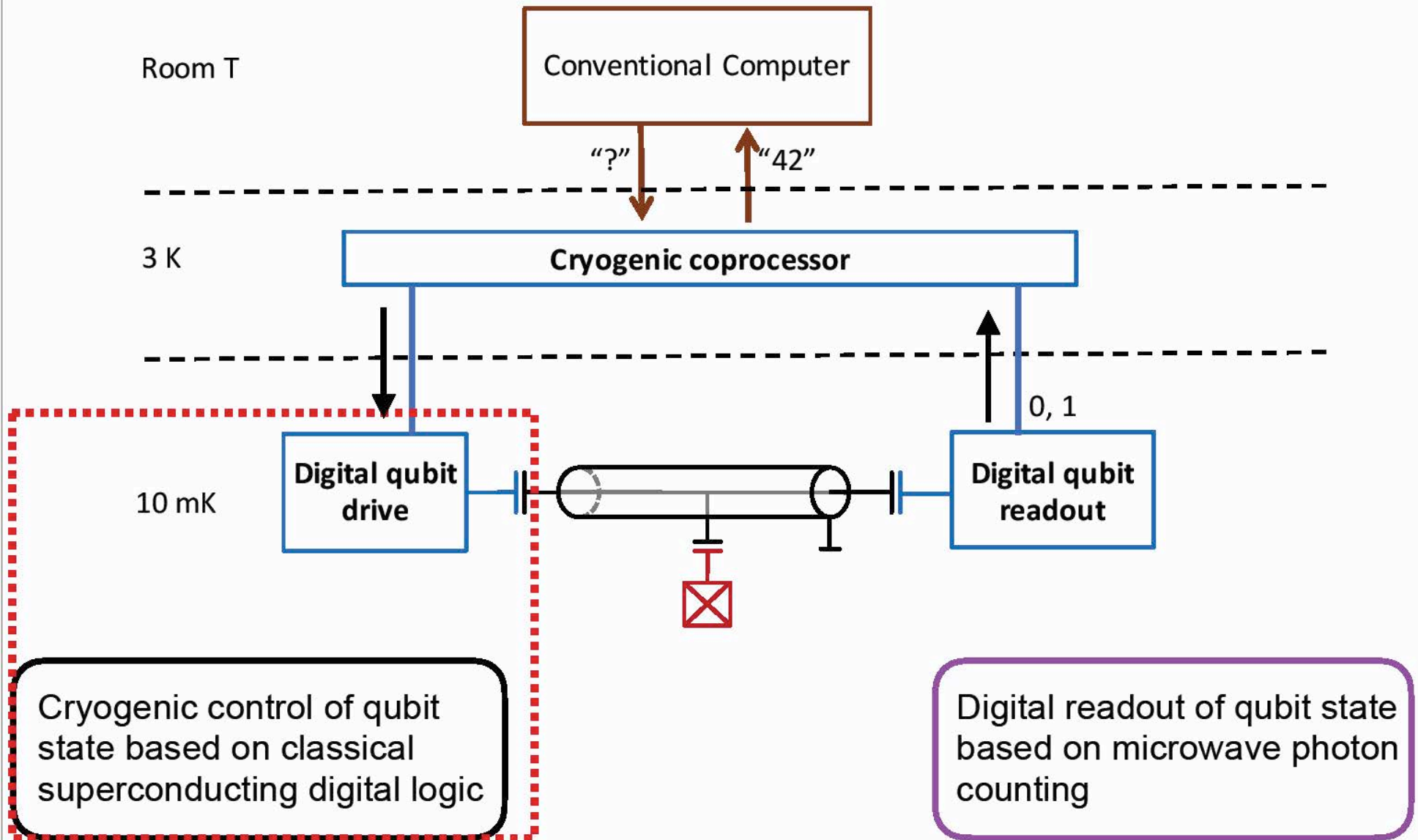


\*N. Yoshikawa, *IEICE Trans. Electron.* (2019)



# Reducing room-temperature hardware overhead

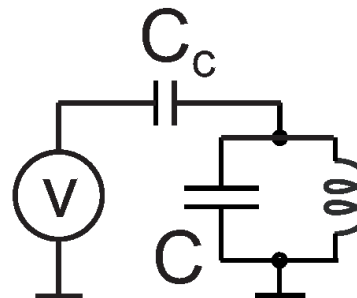
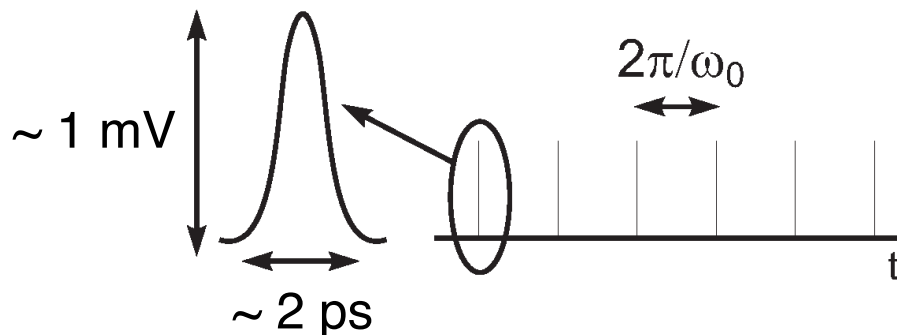
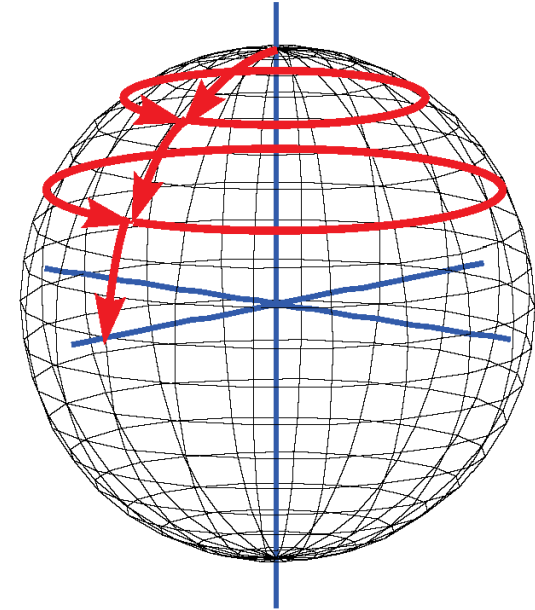
\*McDermott *et al.*, Quant. Sci. Tech. 3, 024004 (2018)



# On-chip digital control of qubits

- SFQ circuitry on same chip as qubits or flip-chip coupling
- Capacitively couple resonant train of narrow SFQ pulses to drive qubit rotations without microwaves
- Important to mitigate heating/quasiparticles produced on-chip from operation of SFQ circuitry

\*McDermott and Vavilov,  
*Phys. Rev. Applied* 2014



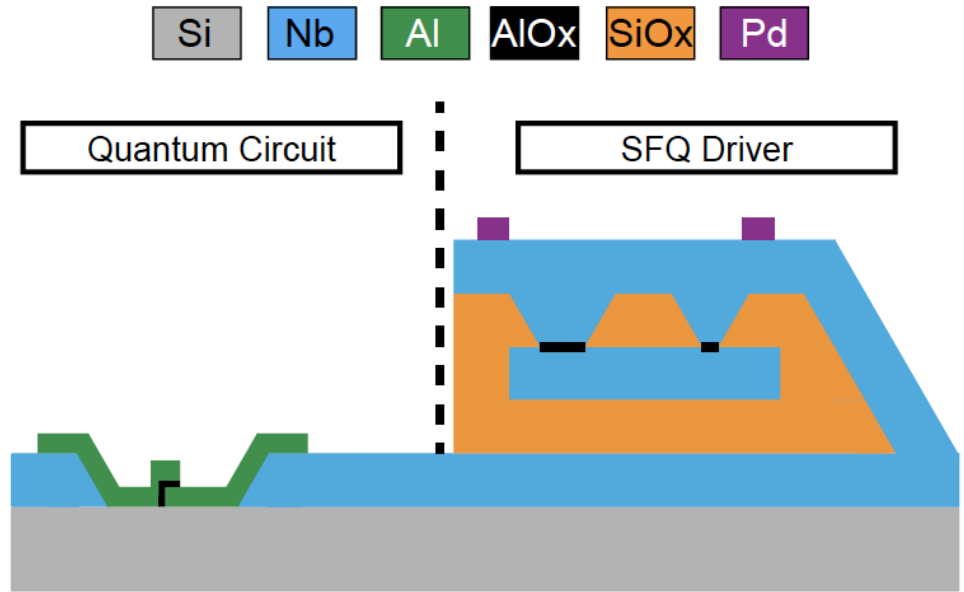
$$\delta\theta = C_c \Phi_0 \sqrt{\frac{2\omega_{01}}{\hbar C}}$$

$\pi$  rotation with  $\sim 100$  pulses

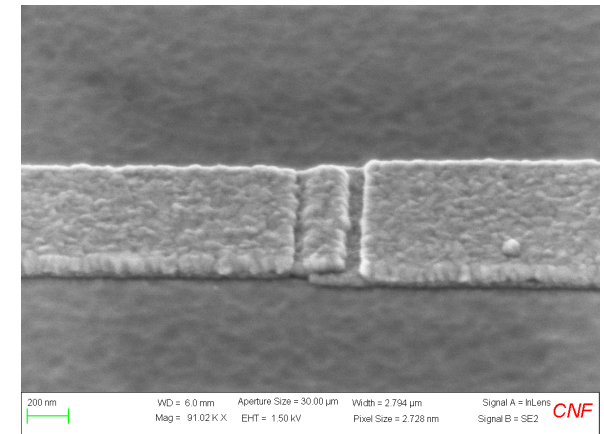
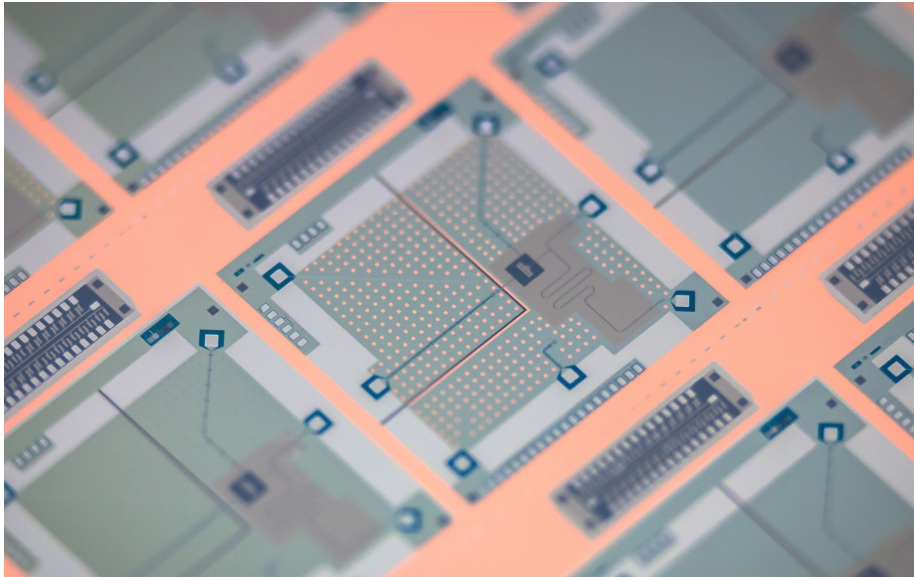
$\sim 14 \text{ ns}$  for 7 GHz qubit

# Implementation of SFQ driver and qubits

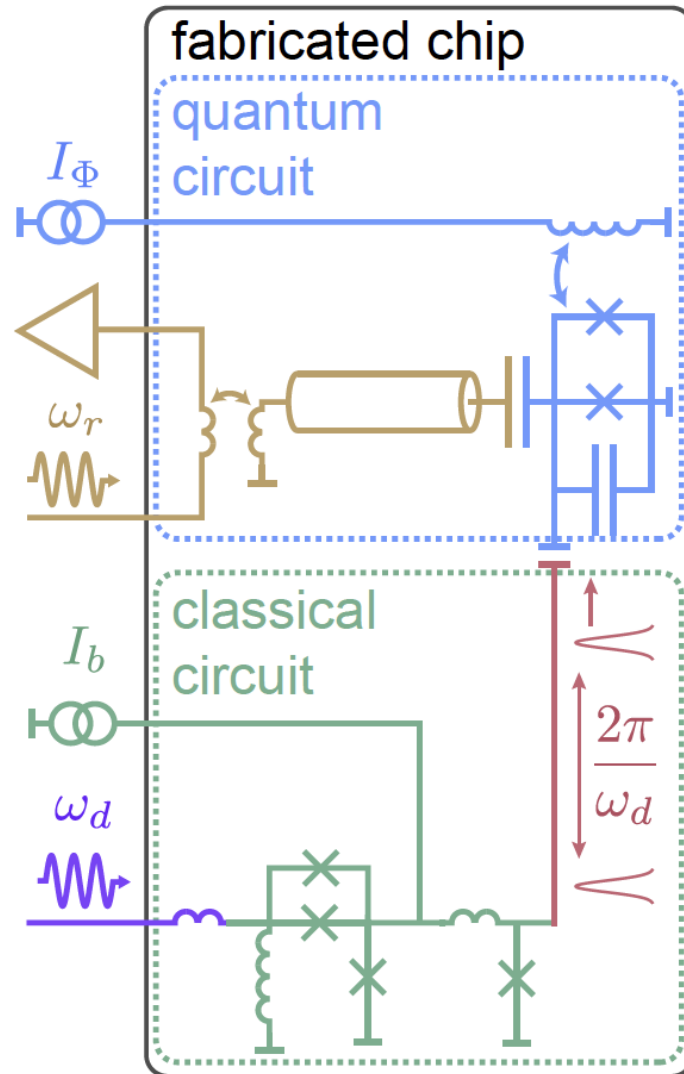
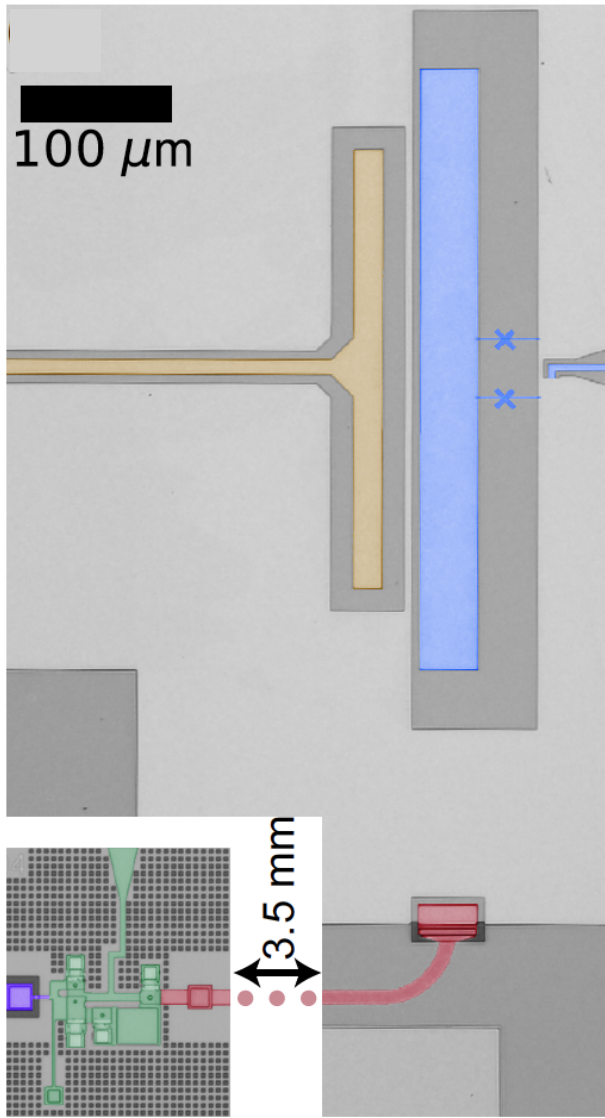
- Collaborative hybrid fabrication
- High-Jc Nb/AIOx/Nb junctions from Wisconsin
- Low-Jc Al/AIOx/Al junctions from Syracuse



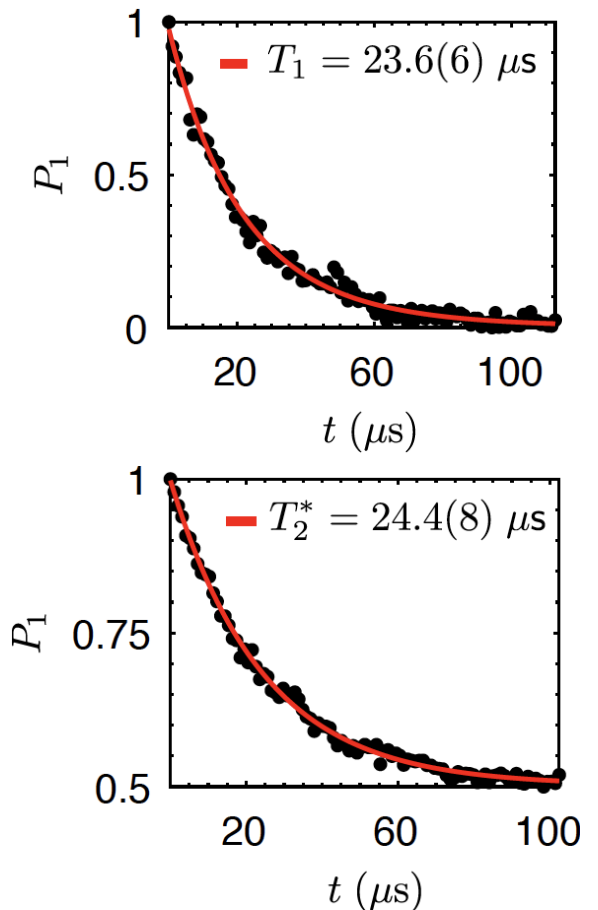
\*Leonard *et al.*, Phys. Rev. Applied 11, 014009 (2019)



# Layout of SFQ driver and qubit

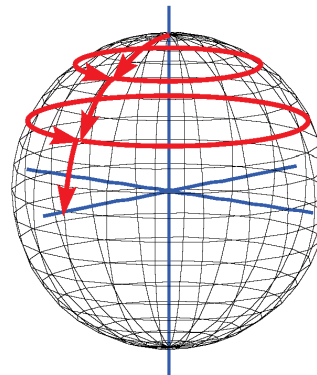
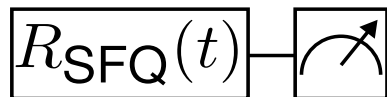
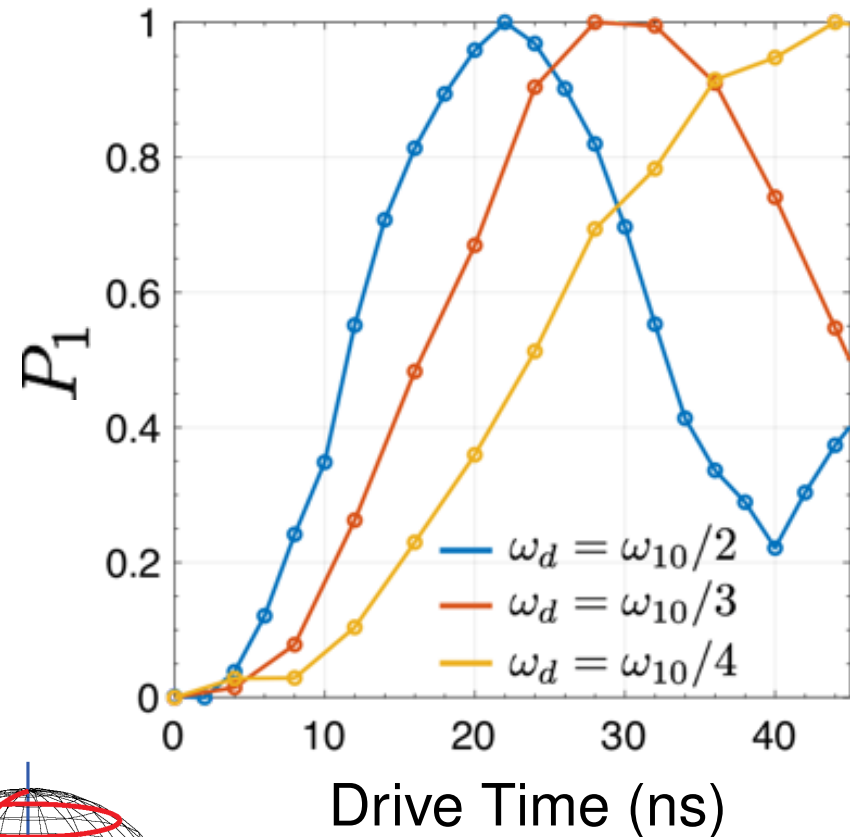
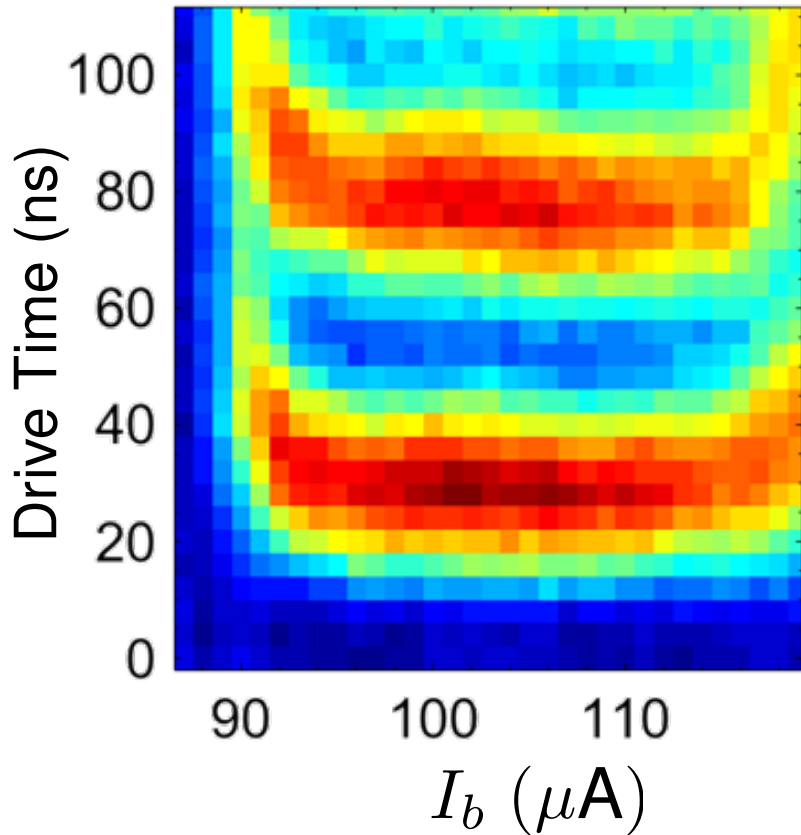


- Conventional heterodyne qubit readout
- Decent coherence



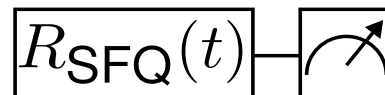
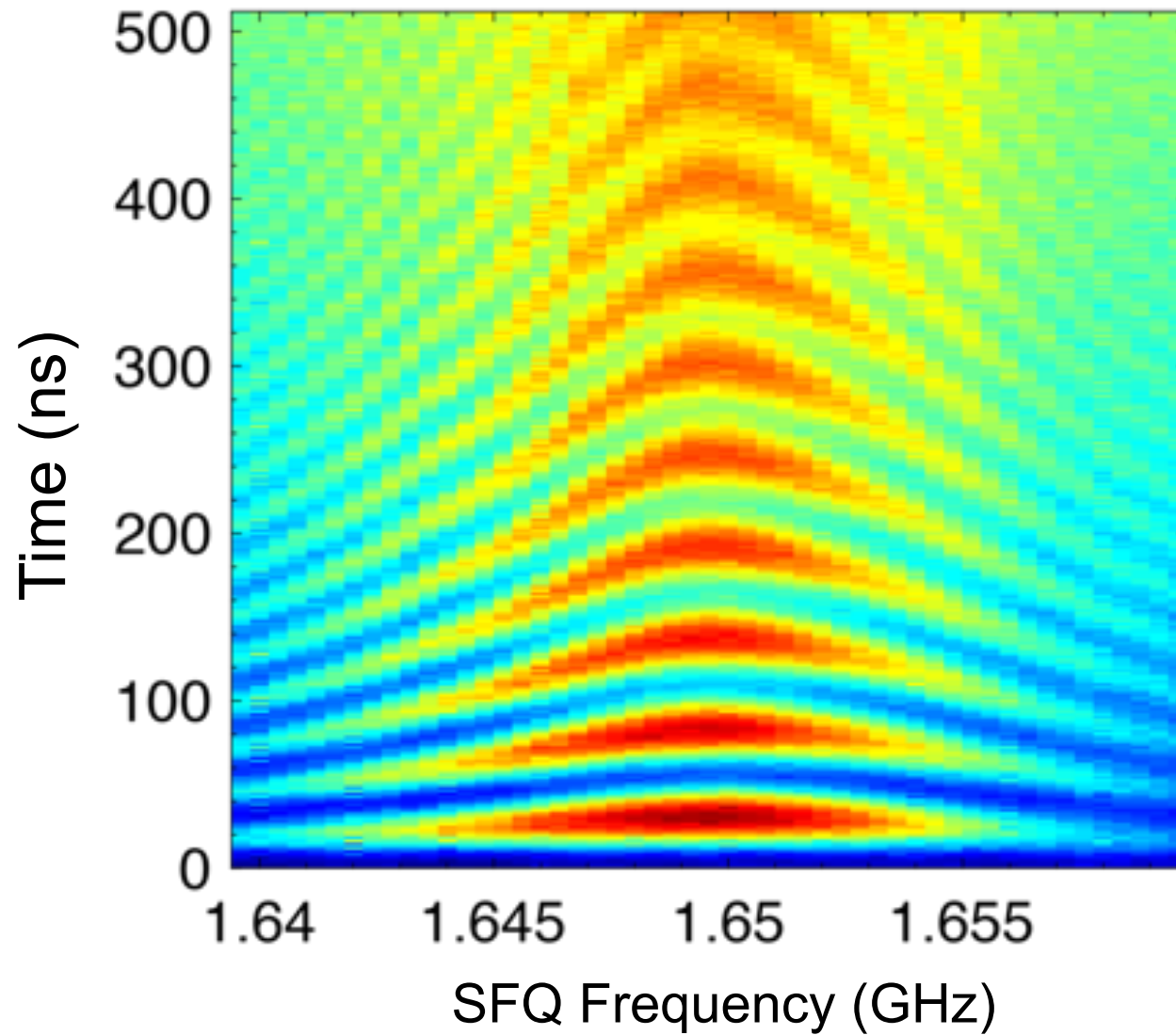
# Qubit Rabi oscillations with SFQ pulses

- Bias qubit at upper sweet spot:  $\omega_{10}/2\pi = 4.958$  GHz
- Send microwave pulses to trigger input of SFQ driver



Drive SFQ circuit on subharmonic to avoid direct drive of qubit

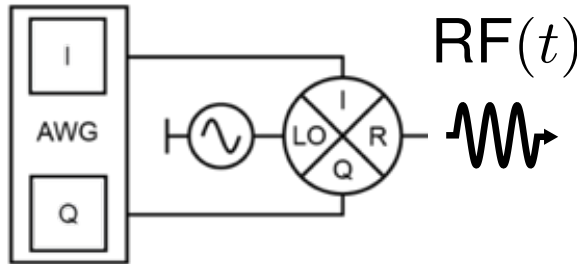
# Qubit Rabi oscillations at $\omega_{10}/3$



# Orthogonal gates with SFQ pulses

$$RF(t) = \cos\left[\underbrace{(\omega_{LO} - \omega_{IF})}_{\omega_d} t + \phi_d\right]$$

DC/SFQ Trigger



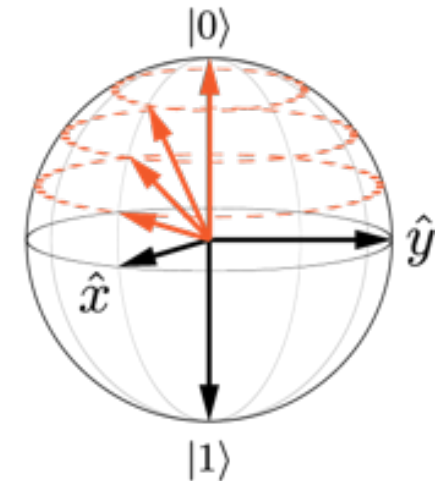
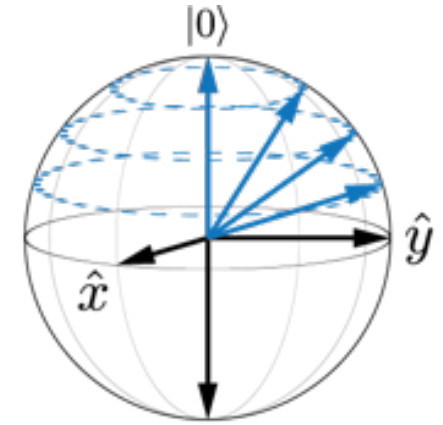
$$X_{SFQ}$$

$$\phi_d = 0$$

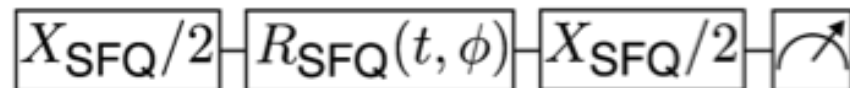
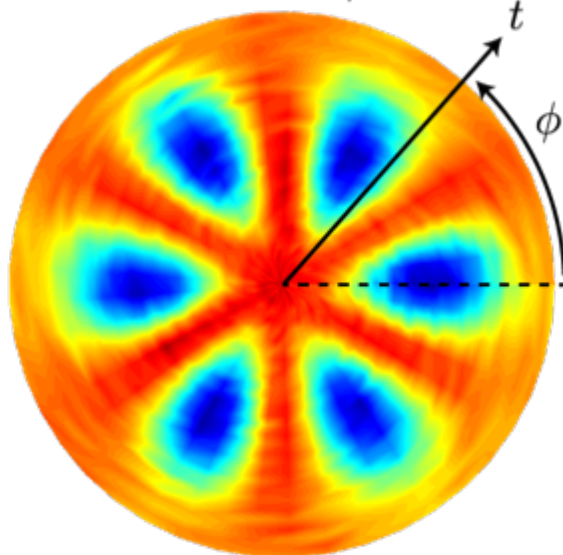


$$Y_{SFQ}$$

$$\phi_d = \frac{\pi}{2n}$$

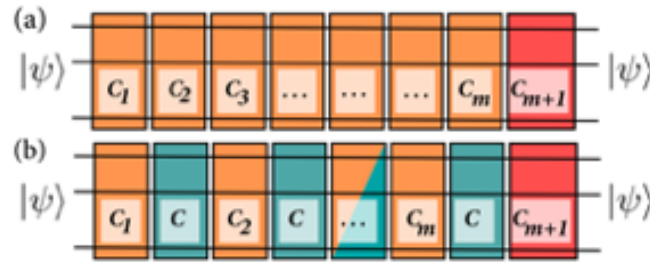


$$\omega_d = \omega_{10}/3$$



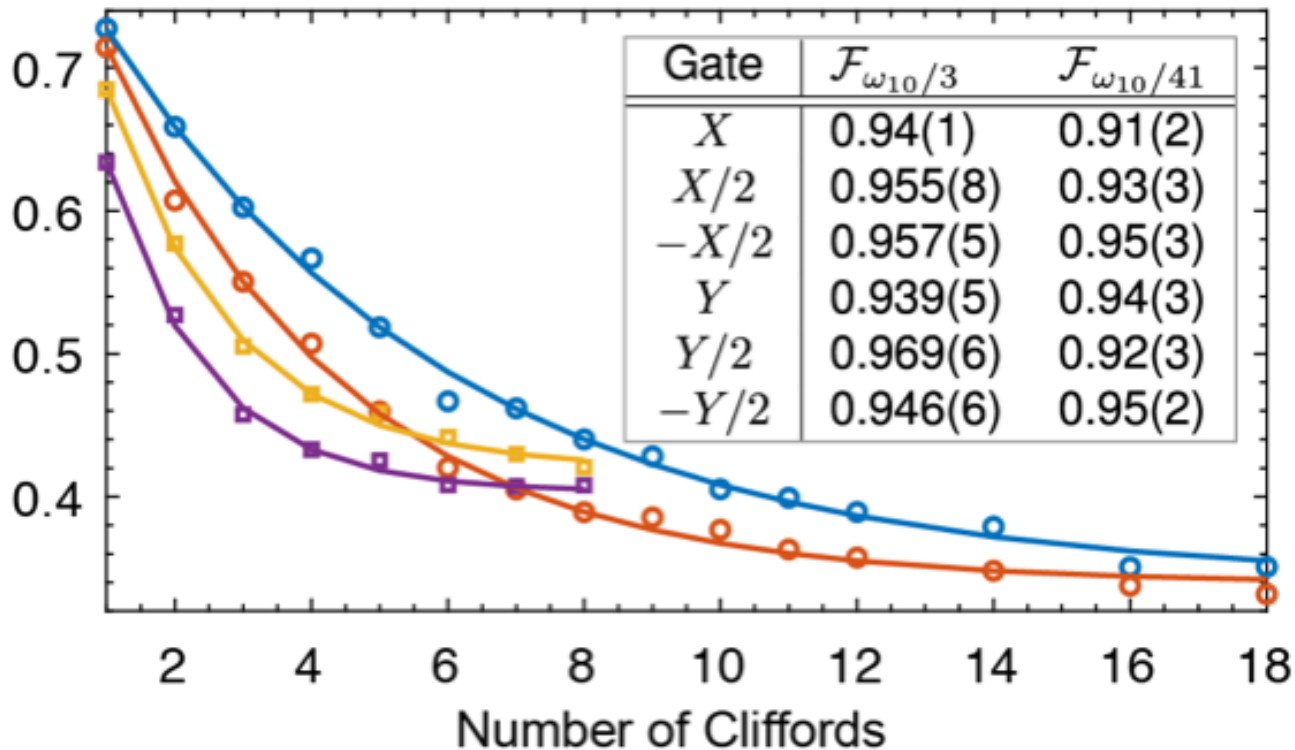
# Characterizing SFQ-based gates

Randomized  
benchmarking



\*Magesan *et al.*, PRL 109, 080505 (2012)

$\omega_{10}/3$  :    ● standard RB    ○ interleaved  $X_{\text{SFQ}}/2$   
 $\omega_{10}/41$  :    ■ standard RB    ■ interleaved  $X_{\text{SFQ}}/2$

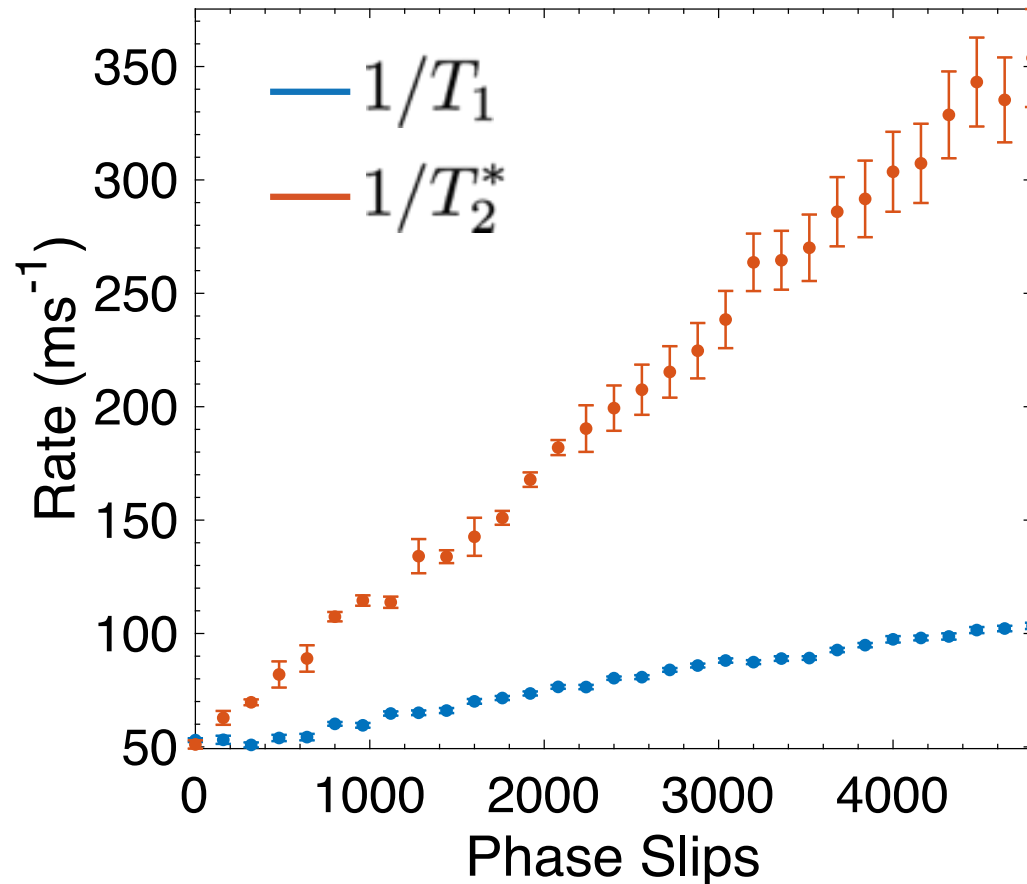
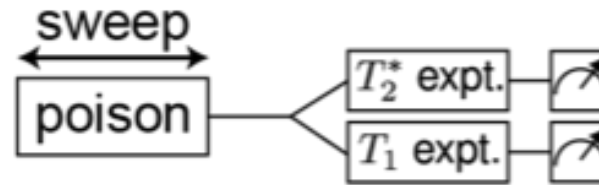


\*Gate fidelities limited by on-chip quasiparticle generation\*



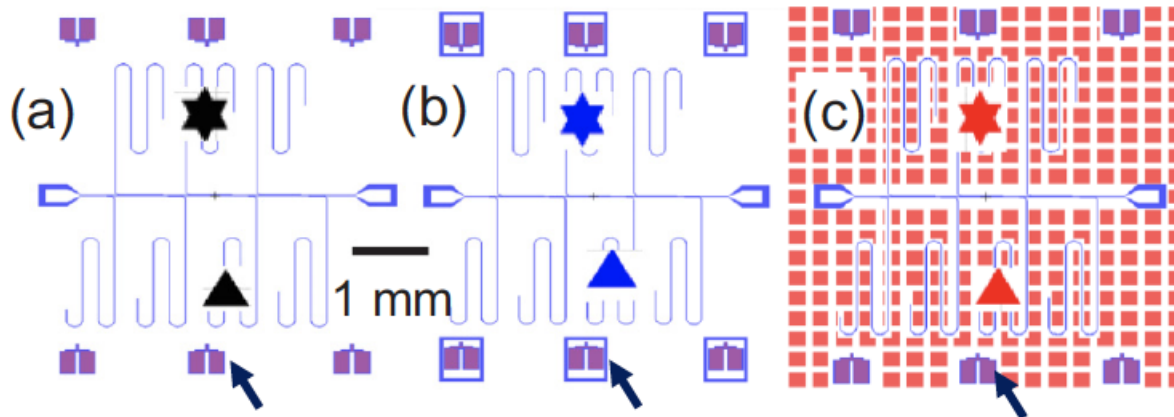
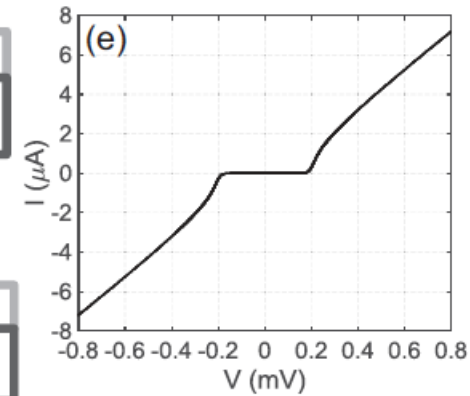
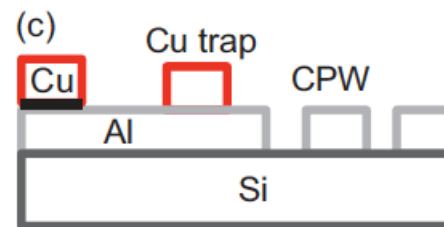
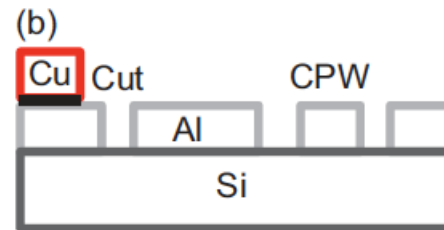
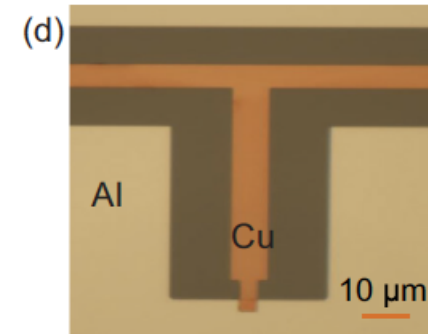
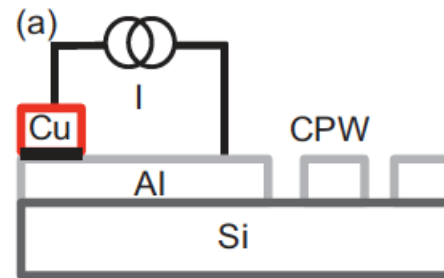
# Quasiparticle poisoning

- Trigger SFQ driver off-resonant from qubit subharmonics
- Phase slips of SFQ junctions generate quasiparticles that poison qubit



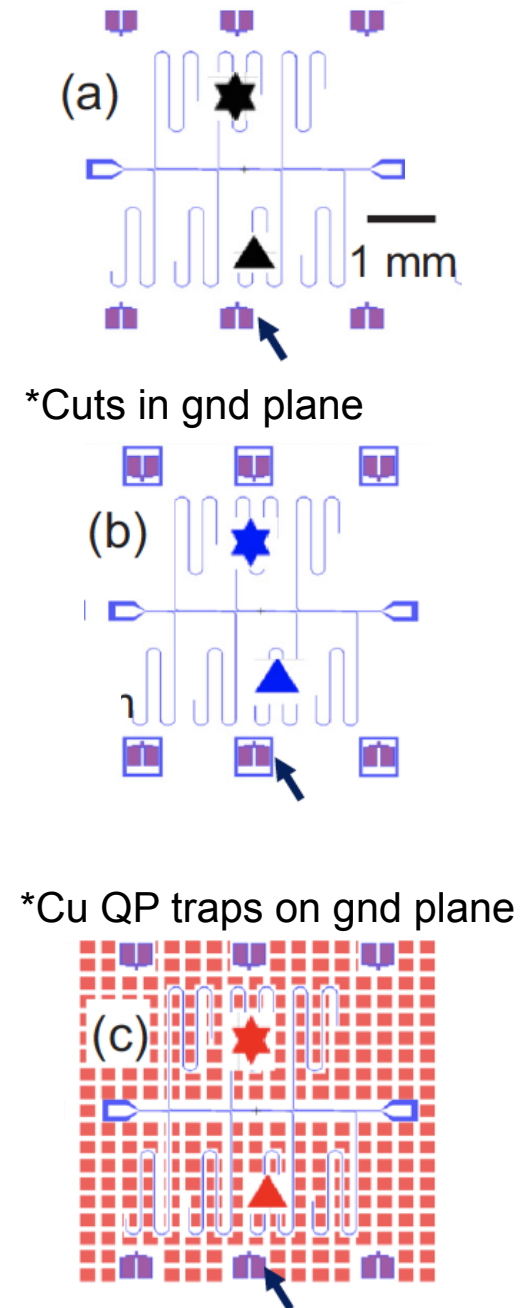
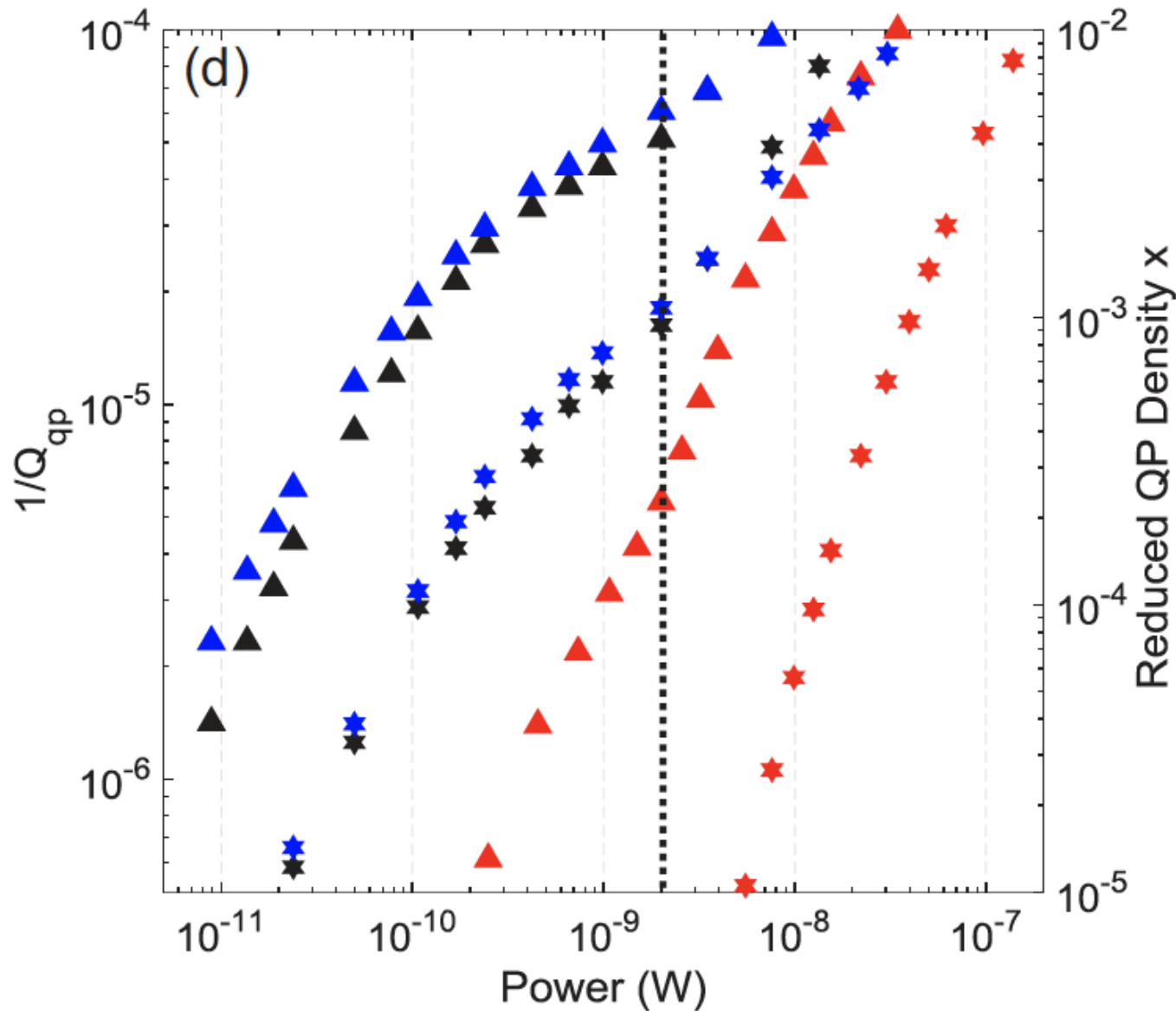
# Loss due to quasiparticle injection

- Aluminum CPW resonators
- NIS junctions along perimeter of ground plane
- Bias junctions beyond gap to inject quasiparticles into ground plane



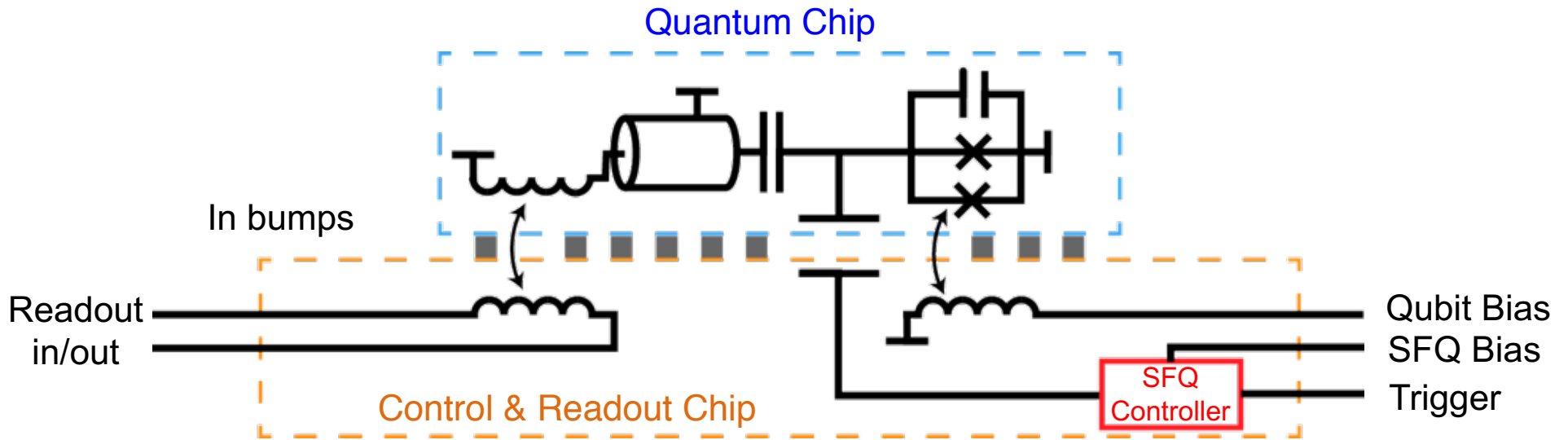
\*Patel et al., *PRB* 96, 220501 (R) (2017)

# Loss due to quasiparticle injection

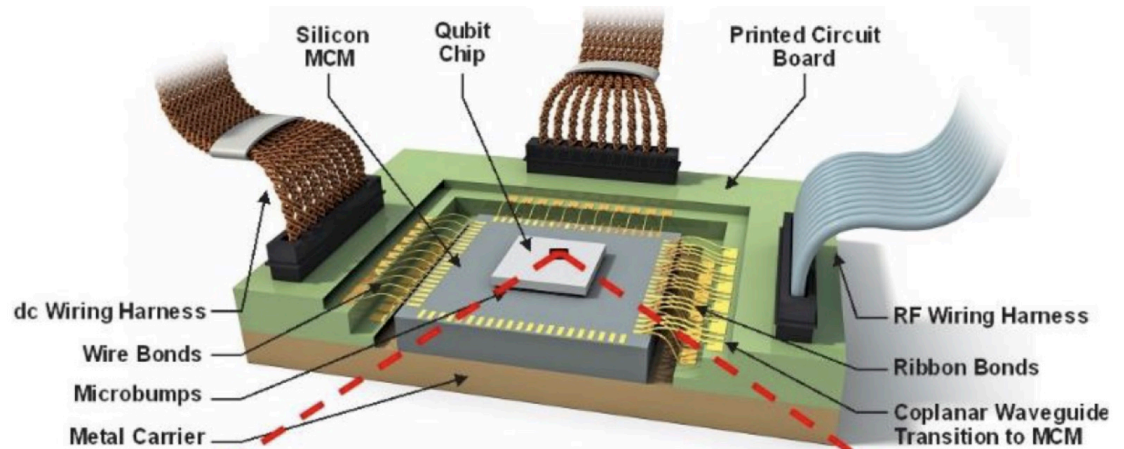


\*Patel et al., *PRB* 96, 220501 (R) (2017)

# Mitigating quasiparticle poisoning



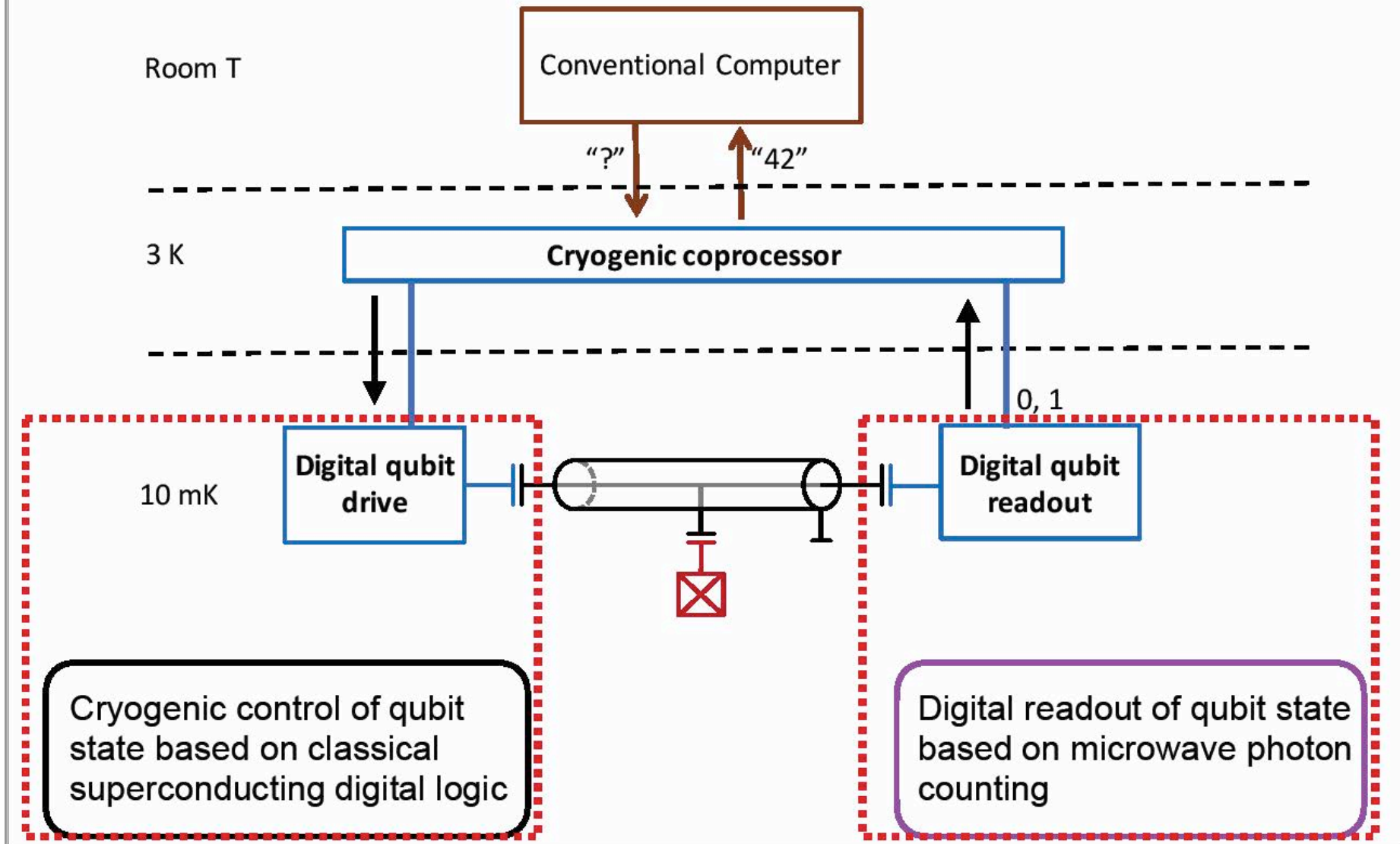
- Multi-chip module (MCM) configuration
- Separate high-coherence qubits and resonators from dissipative classical control/readout circuitry



\*R. Das et al., IEEE 68th ECTC (2018)

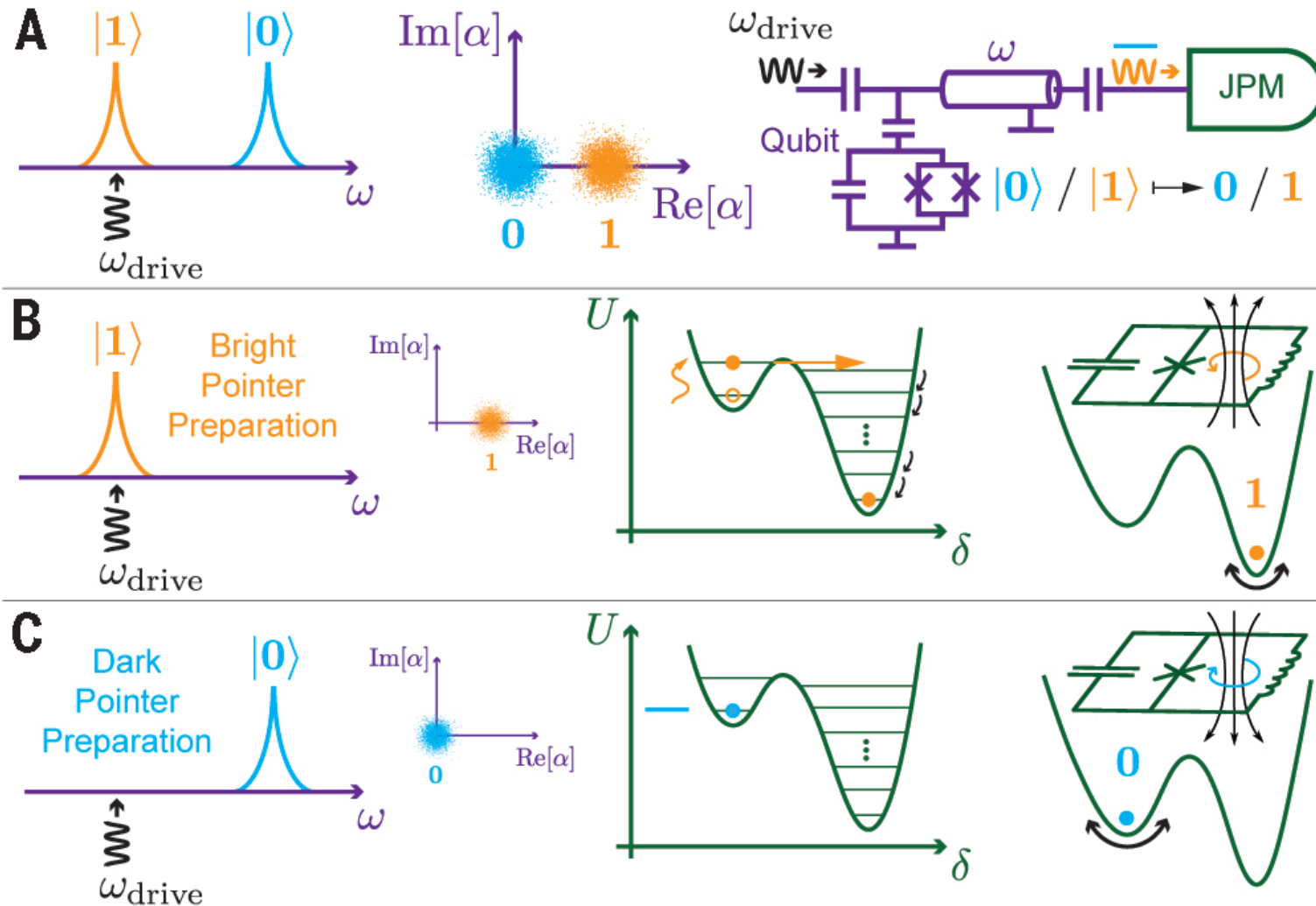
# Reducing room-temperature hardware overhead

\*McDermott *et al.*, Quant. Sci. Tech. 3, 024004 (2018)



# Digital Readout of Qubit with Josephson Photomultiplier

\*Opremcak *et al.*, Science 361, 1239 (2018)

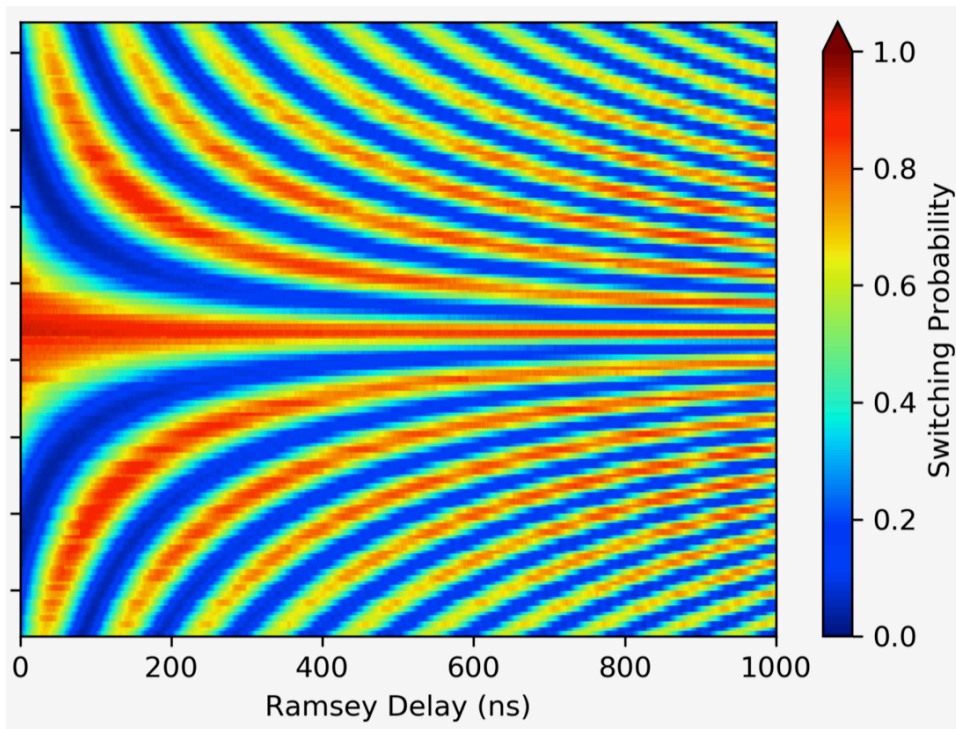


\*Chen *et al.*, Phys. Rev. Lett. (2011)

\*Govia *et al.*, Phys. Rev. A (2014)

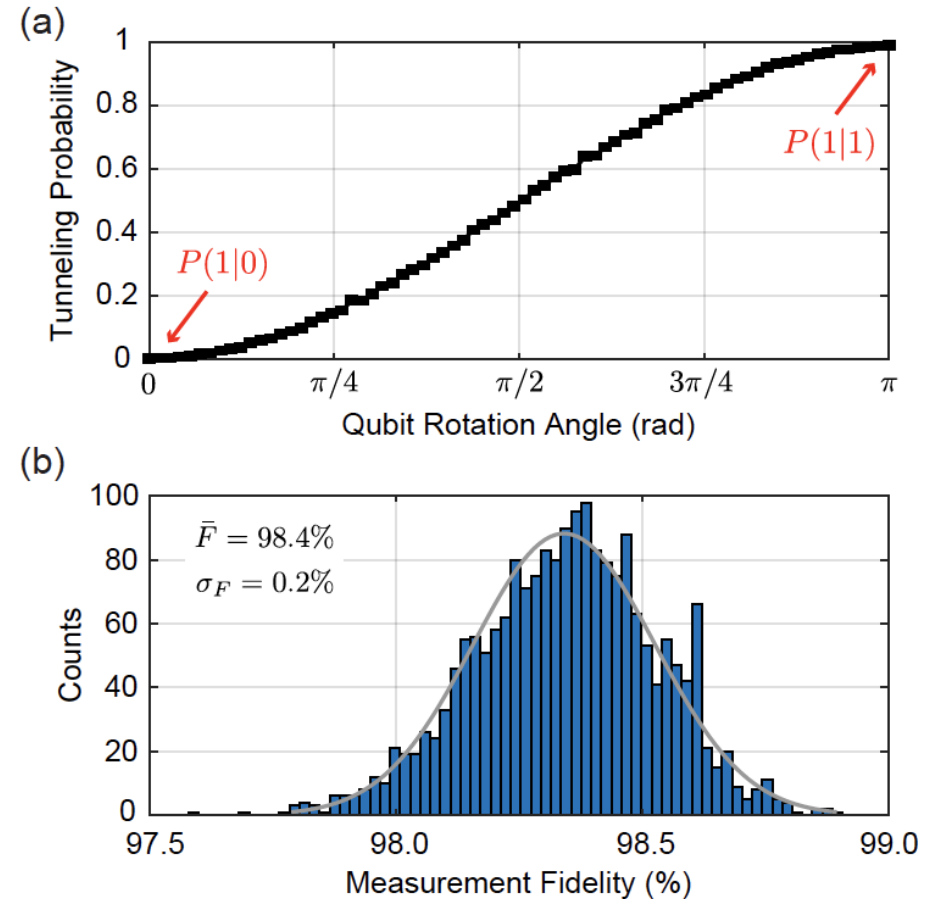
# Digital Readout of Qubit with Josephson Photomultiplier

\*Opremcak *et al.*, Science 361, 1239 (2018)



Raw measurement fidelity  $\approx 92\%$

\*Opremcak *et al.*, arXiv:2008.02346 (2020)

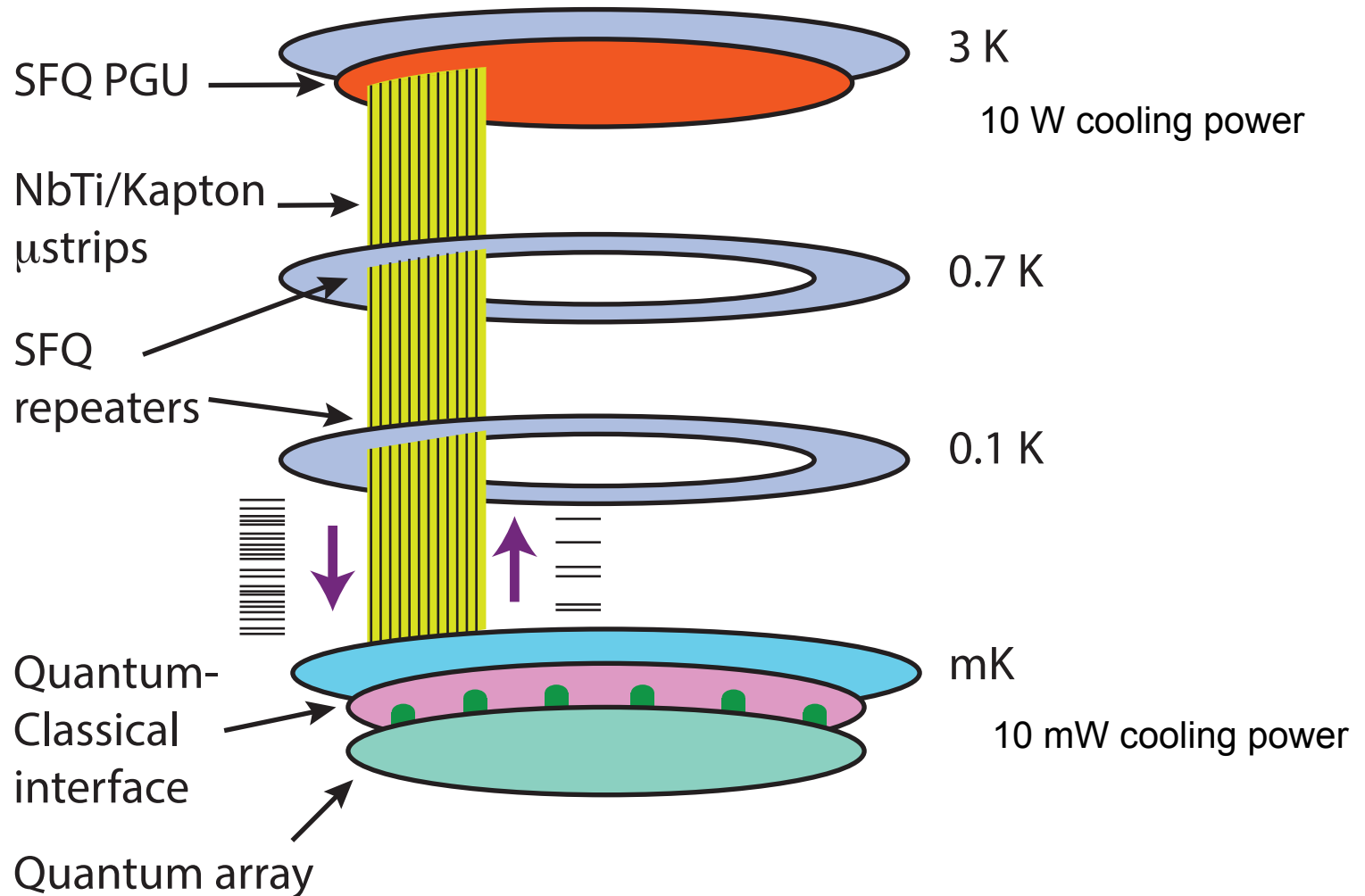


- Fast, high-fidelity qubit readout with no need for microwave isolators
- Measurement result accessible at mK; possibility of converting to SFQ signal for cryogenic processing



\*Howington *et al.*, IEEE Trans. Appl. SC (2019)

# Quantum-Classical Interface



Quantum layer = qubits and readout resonators only; minimal fab processing

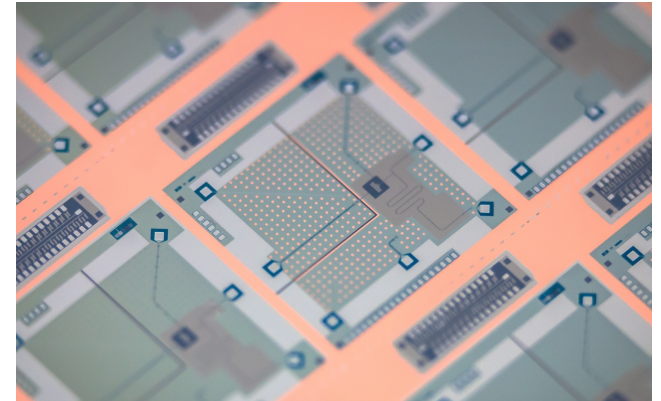
Quantum-Classical interface layer = SFQ drivers; JPMs and SFQ output; flux bias lines



# Summary

- Hardware challenges for scaling to large qubit arrays with conventional microwave-based control and readout

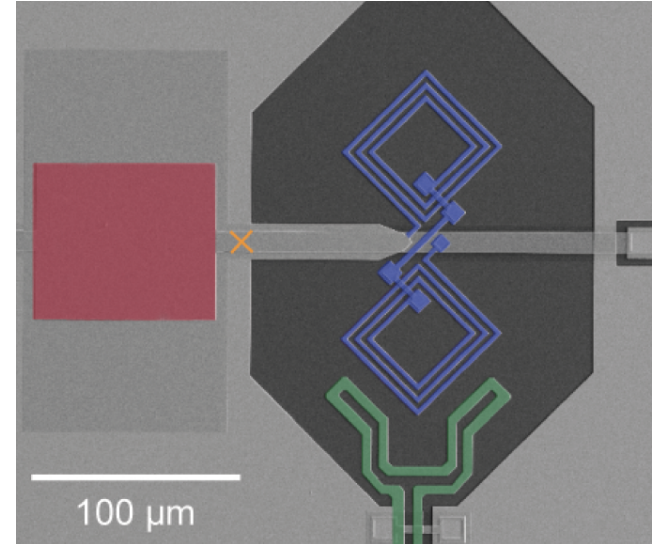
\*McDermott *et al.*, Quant. Sci. Tech. 3, 024004 (2018)



- Cryogenic control offers a pathway to overcome scaling challenges

- SFQ-based qubit control without microwave pulses

\*Leonard *et al.*, Phys. Rev. Applied 11, 014009 (2019)



- Microwave photon counter JPMs for digital readout of qubit state

\*Opremcak *et al.*, Science 361, 1239 (2018)

