IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), No. 49, March 2021.
Invited presentation Wk1EOr3B-01 given at the virtual ASC 2020, October 29, 2020.

A 150-nm Node of an Eight-Nb-layer Fully Planarized Process for Superconductor Electronics

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LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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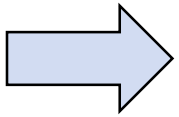
Outline



- Introduction and Motivation
- Scaling of Superconductor Electronics (SCE)
- MIT LL Research Foundry and fabrication processes for SCE
  - SFQ4ee and SFQ5ee, and SFQ6ee
  - SC1 process
- 150-nm SC2 process and its characterization
  - Wiring
  - Inductors
  - Josephson junctions
  - Benchmark circuits
- Conclusion

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Abstract

- At the last ASC2018 we introduced a new fabrication process for superconductor electronics, SC1, with 250 nm minimum linewidth. This process differs from our standard 350-nm SFQ5ee process by the placement of Josephson junctions and shunt resistors near the bottom of the layer stack, while similar in all other respects, utilizing 248-nm photolithography and high density plasma (HDP) etching for layer patterning, and chemical-mechanical polishing (CMP) of interlayer dielectric for layer planarization.
- This time, we present the next node, 150-nm node, of the SC process, titled SC2. It is an eight-Nb-layer process with layer structure and planarization scheme similar to the SC1 node. We use a 193-nm photolithography to define circuit features down to 150 nm on a few critical layers, including inductors and Josephson junctions, and 248-nm photolithography for all other (non-critical) layers. We present process characterization including data on critical currents and inductance of Nb lines in the 120 nm to 250 nm range, on-chip linewidth statistics and on-wafer uniformity.
- The process offers two types of Nb/Al-AlO_x/Nb junctions: resistively shunted with Josephson critical current density J_c = 100 and 200 μA/μm^2, and self-shunted junctions with J_c = 600 μA/μm^2. We present data on electrical properties and statistics of Josephson junctions (JJs) defined by 193-nm photolithography and their comparison with those defined by 248-nm photolithography.
- To benchmark the SC2 node, we designed test circuits using self-shunted junctions and 150-nm linewidth for inductors, and fabricated and tested them, e.g., DC-SFQ and SFQ-DC converters, balanced comparators, SFQ and QFP logic gates, ac-biased shift registers, etc. We demonstrate a ~2x increase in the circuit density in comparison with SC1 process by implementing a single layer of 150-nm linewidth inductors on the Nb layer closest to the JJ layer in the stack. For the shift registers with 600-μA/μm^2 self-shunted Josephson junctions, we achieved the circuit density of $1.3 \cdot 10^7$ JJs per cm^2, thus crossing over the threshold of 10M JJs per 1-cm^2 chip, the integration scale required for applications in large-scale superconductor electronic systems.

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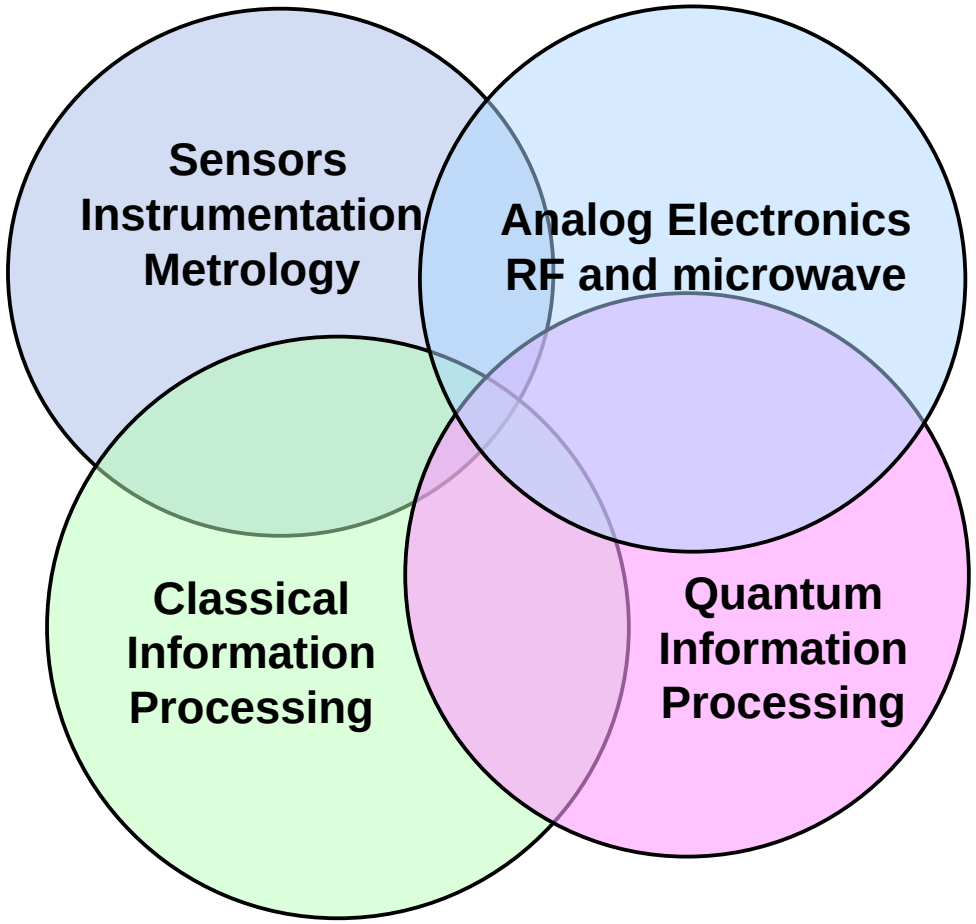
Superconductor Electronics

- **Sensors, Instrumentation, Metrology**
  - SQUIDs, SQIFs,…
  - TES, MKID, SNSPD, …
  - DC and AC Voltage Standards, etc.
- **Analog Electronics**
  - RF and Microwave transmission
  - Resonators, antennas, filters, mixers,…
  - Parametric amplifiers
- **Classical Information Processing**
  - Digital electronics and computations
    - (R)SFQ, RQL, (A)QFP digital circuits
  - Mixed Signal
    - Digital Signal Processing: ADC, TDC, FFT, etc.
- **Quantum Information Processing**
  - Quantum annealers, analog processors
  - Gate-based quantum computing



Progress in all areas requires increasing the scale of integration

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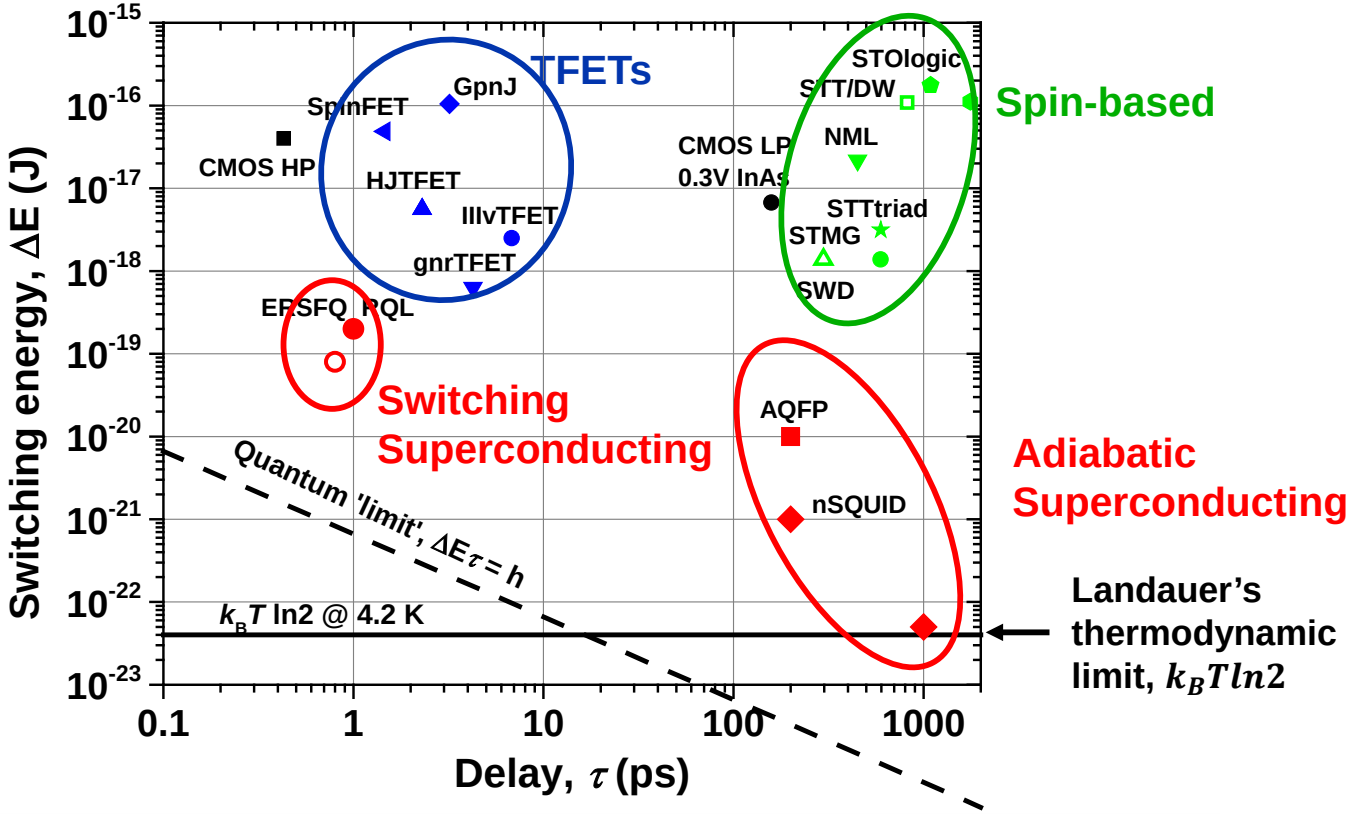
Superconductor Digital Electronics Development Drivers

- **Historically** − High-clock-speed computing and DSP due to possibilities of near-THz clock frequencies and low latency
- **More recently** − Energy efficient computing, adiabatic and reversible computing, quantum computing
- Appears to be more mature than other "disruptive" beyond-CMOS technologies
- Ideal for applications in systems requiring cryogenic temperatures
- Several different types of digital logic available

Switching Energy for Emerging Devices



Superconducting electronics has demonstrated the lowest energy per operation (~ 10^{-22} J at 4.2 K), the highest clock speeds (up to 770 GHz), and is more mature than other beyond-CMOS technologies

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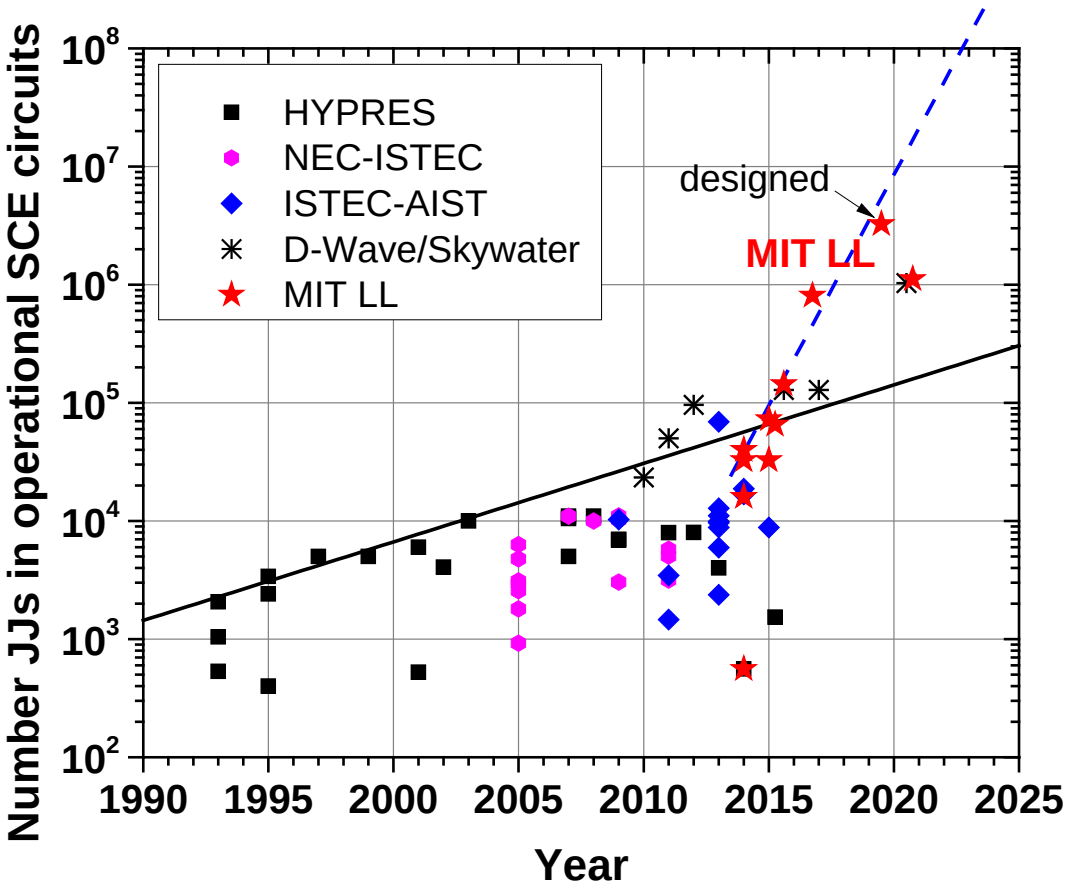
Superconductor Electronics Scaling

- Superconductor electronics (SCE) can provide advantages in speed and energy consumption for
  - Classical and quantum information processing
  - Digital signal processing
  - Advanced sensor arrays and imagers, etc.
- However, to become useful and competitive in functionality, SCE must increase integration scale
- Modern CMOS processors have ~ 20B transistors per chip
  - Density: ~ 17B transistors/cm^2 (5-nm FinFET, TSMC)
  - Chip sizes: up to ~ 8 cm^2
- The largest demonstrated SCE circuits have ~ 1M JJs and density of 1.3M JJs per cm^2, a factor of 10^4 less than in CMOS
- Assuming SCE could grow according to the Moore's law, double JJ count every 2 years, it would take more than 28 years to reach the current CMOS level
- SCE needs a path for increasing integration scale



MIT LL technology enables very large scale integration (VLSI) of superconducting circuits

SCE Scaling Relations

- **SCE scaling is very different from CMOS**
  - **SCE circuits include Josephson junctions (JJs) and inductors in about 1:1 ratio, usually competing for the same area**
  - **Hence, the circuit density is optimized when density of JJs, n_J is approximately equal to density of inductors, n_L**
- **The minimum critical current of JJs, $I_{c\,min}$ ~ 50 μA, is set by the circuit bit error rate requirements**
- **This sets the minimum JJ area (size) and the maximum JJ density at a given Josephson critical current density, J_c:**

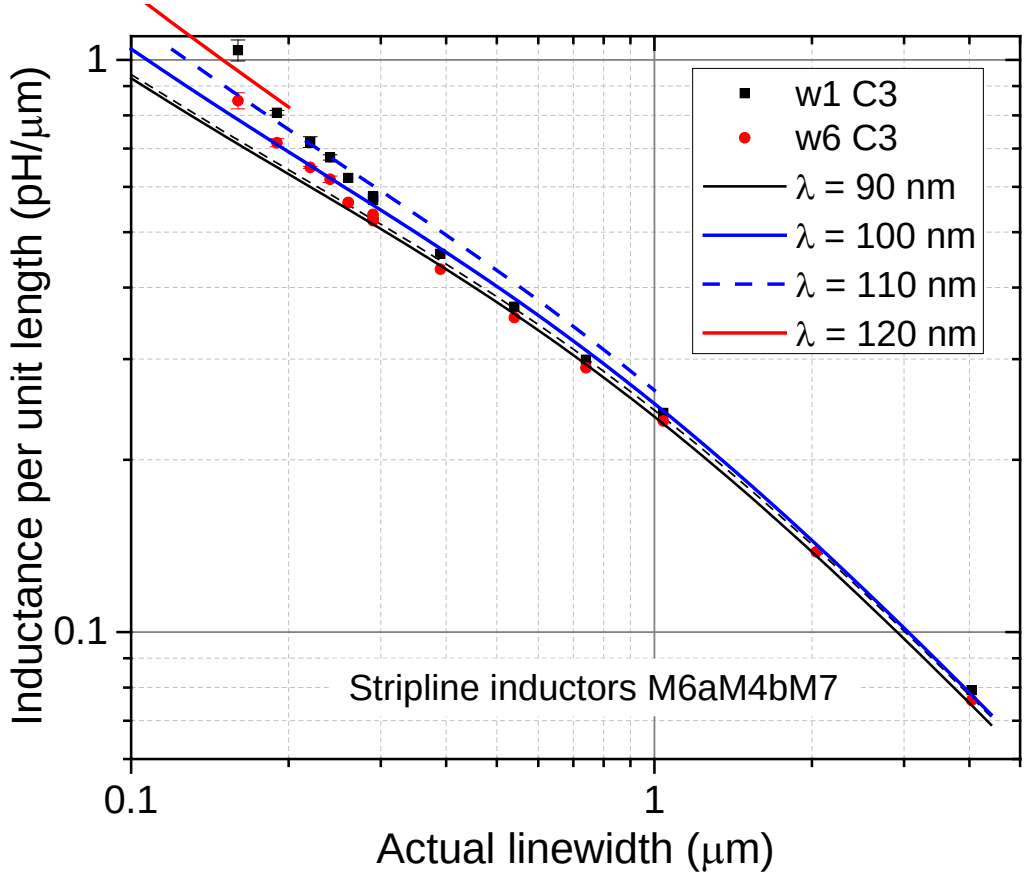
$$n_J < J_c/I_{c\,min} \text{ and } d_{min}\,(\text{in } \mu\text{m}) \approx 8/J_c^{1/2},$$

where J_c is in μA/μm²

  - d_{min} = 0.8 and 0.33 μm at J_c =100 and 600 μA/μm², respectively
- **Because information is encoded by presence/absence or location of a single flux quantum in logic cells, LI_c is nearly constant, the order of Φ_0, where L - the typical inductance**
- **Hence, the selected I_c (JJ size) determines the typical value and area (and density) of inductors**

$$A_L \sim (L/\ell)p,$$

$\ell = \ell(w)$ is linewidth-dependent inductance per unit length and p is the inductor pitch (linewidth + spacing)

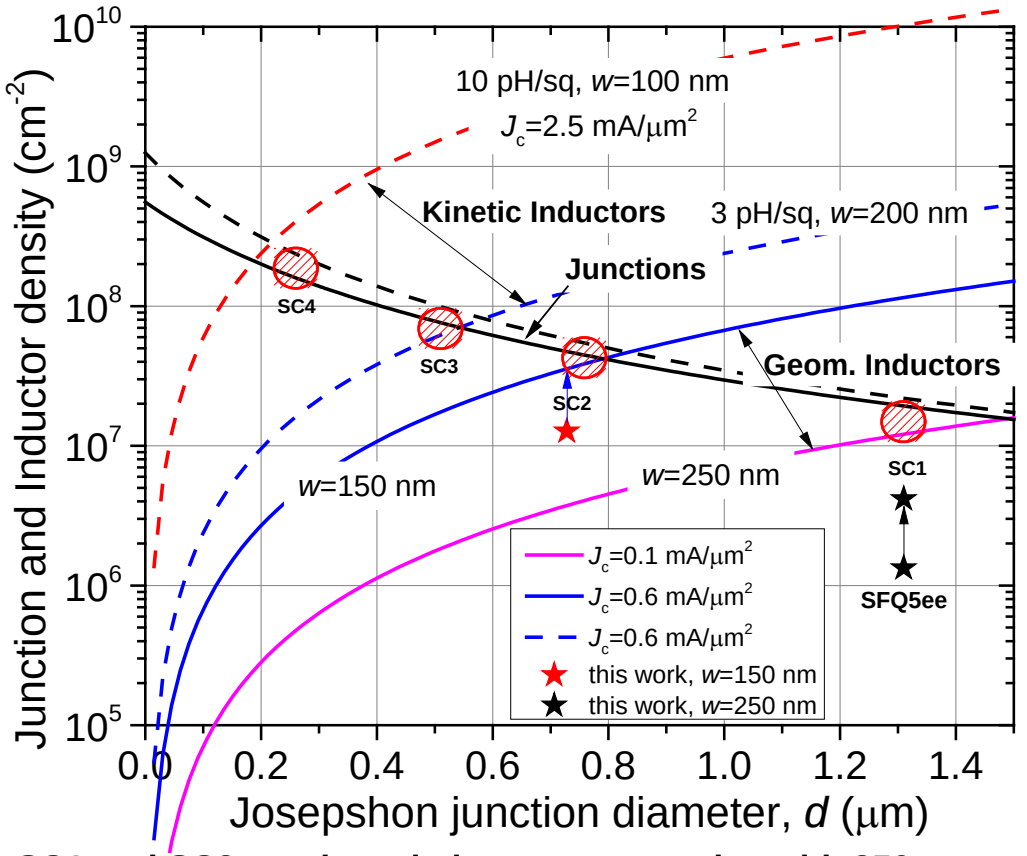


See Poster Wk2EPo2A "Inductance of superconductor circuit features with sizes down to 120 nm fabricated in a eight-Nb-layer planarized process" for details

https://asc2020.ipostersessions.com/default.aspx?s=FA-AE-82-7F-BE-19-7D-F5-51-B4-35-86-E8-CF-E8-47&guestview=true

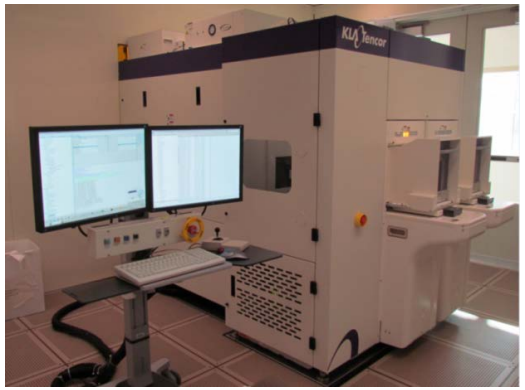
SCE Scaling Relations

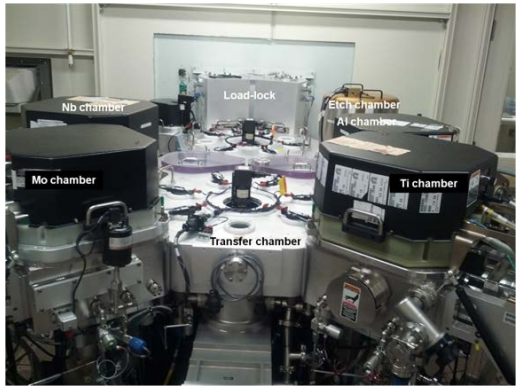
- **There are three process parameters which we need to decrease, and two materials parameters which we need to increase in order to increase the overall circuit density:**
  - **JJ min size, *d; we want to decrease it***
  - **Inductor linewidth, *w* and pitch, *p; want to decrease them***
  - **Interlayer contact (via) size; *also want to decrease***
  - **JJ critical current density, J_c *should increase as* $1/d_{min}^2$**
  - **Inductance per unit length, ℓ or sheet inductance L_{sq}**
- **JJ density is proportional to $1/(d+sr)^2$ and *decreases with increasing d,* where *sr* is the required surround**
- **Geom. inductor maximum density increases with *d* as $\ell d^2/p$ *because larger JJs need smaller inductors***
- **Similarly, kinetic inductor maximum density would also increase with *d* as $L_{sq}d^2/pw$, where L_{sq} – the sheet inductance**
- **Replacing geometrical inductors by kinetic inductors can dramatically increase inductor density if $L_{sq}/w >> \ell$ ~ 1 pH/μm**
- **Design optimization is required for each node**



SC1 and SC2 are the existing process nodes with 250 nm and 150 nm min linewidth, respectively
SC3 and SC4 are Roadmap nodes requiring kinetic inductors

MIT LL Microelectronics Laboratory Trusted Foundry





SCE Fab at MIT LL Leverages Facilities and Toolset of 90-nm CMOS Foundry in ML

- Photolithography
  - 248-nm Cannon stepper for standard process nodes
  - 193-nm ASML 5500 scanner for critical layers in advanced nodes
- Photoresist processing and wafer cleaning tools
- Chemical-mechanical polishing tools for dielectric and metal CMP
- Metrology tools: SEMs, stress and resistance mappers, ellipsometers,…

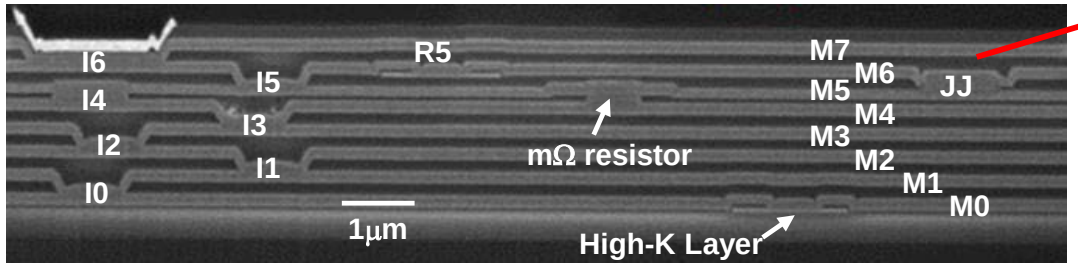
Dedicated Tools Enhance SCE Processing Capabilities

- Sputter deposition cluster tools for superconducting thin films: Nb, Al, Mo_2N, $NbTiN_x$
- Low-temperature dielectric deposition tools
  - HDP gap fill and interlayer dielectric deposition
  - PECVD dielectric
- High-density plasma metal and dielectric etchers
- KLA-Tencor Altair 8920 Defect Inspection tool

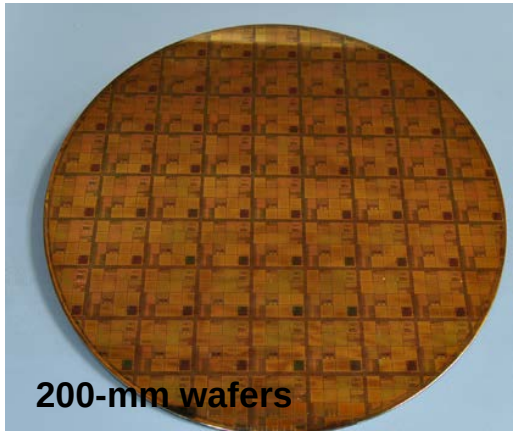
MIT Lincoln Lab SCE Research Foundry

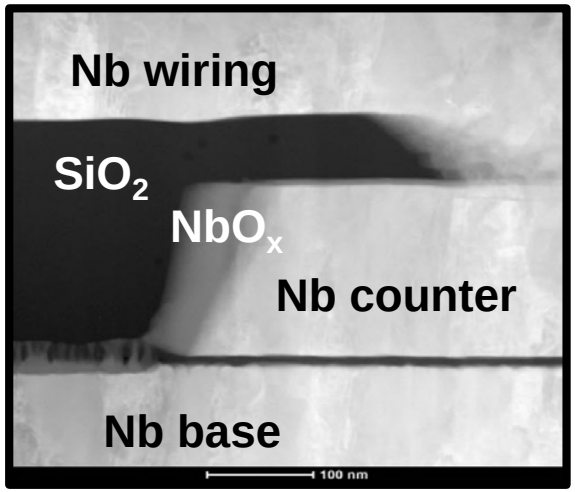
- **Microelectronics Laboratory (ML)**
  - **Total: 6,400 m^2 (Class-10: 740 m^2; Class-100: 910 m^2)**
  - **Production-class 90-nm, 200-mm wafer tool set**
  - **3-shift, 5-day (24/5) operation**
- **~ 1,000 SCE wafer starts per year**
  - **22 mm x 22 mm die size**
  - **45 dies per wafer**
  - **5 mm x 5 mm chips (16 chips per die, 675 chips per wafer)**
  - **Also 5 mm x 10 mm and 10 mm x 10 mm chips**
  - **Multi-project runs**
- **Government Furnished Foundry**

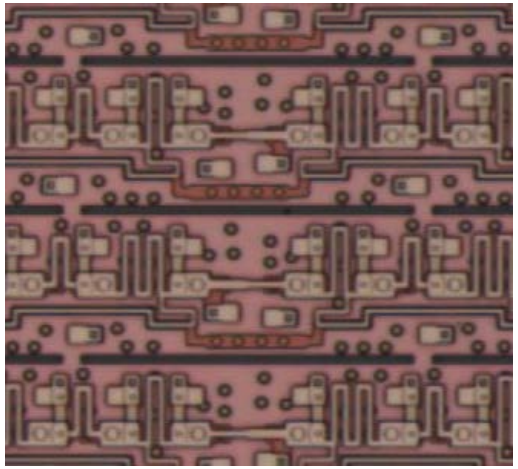
SFQ-5ee (9-Metal-Layers) Process



Microelectronics Laboratory







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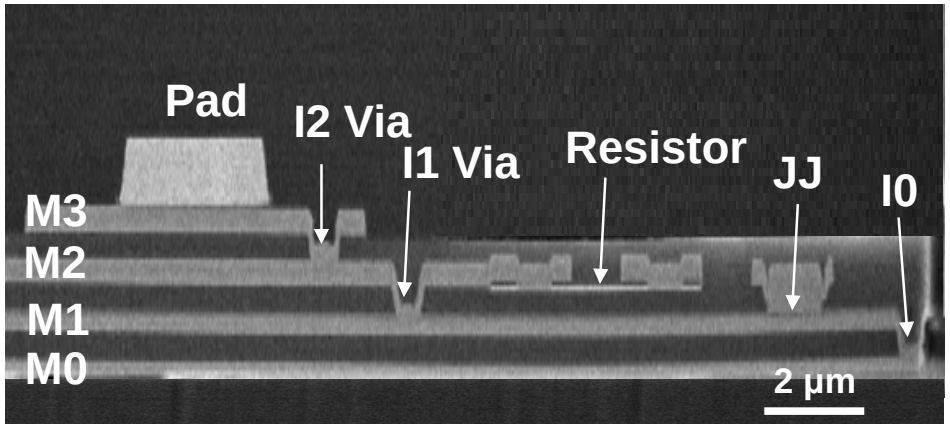
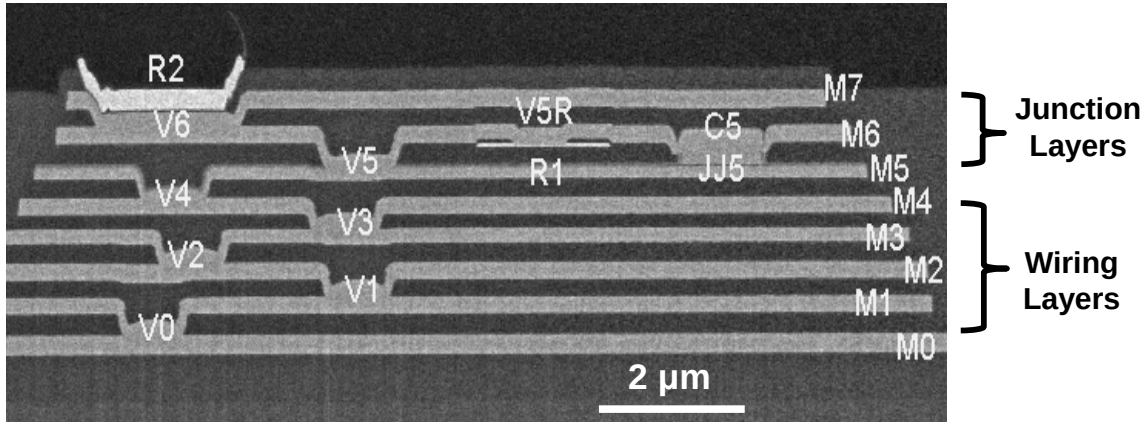
MIT LL Superconducting Electronics Fabrication

4-layer node SFQ3ee, 2012



- Wafer size: 200 mm
- Number of Nb layers: 4
- Resistors: Pt, 2 Ω/sq, lift-off
- Min JJ size: 700 nm
- Min wiring size: 700 nm
- Min spacing: 1000 nm

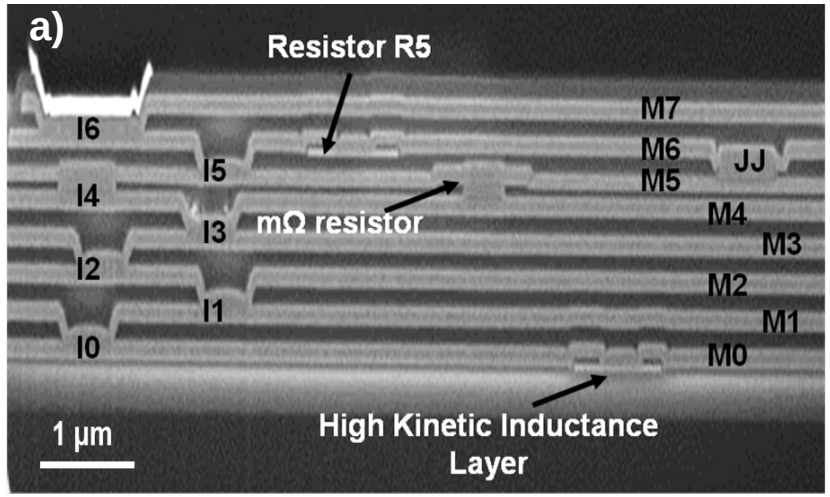
8-layer node SFQ4ee, 2014



- Wafer size: 200 mm
- Number of Nb layers: 8
- Resistors: Mo, 2 Ω/sq, etched
- Min JJ size: 700 nm
- Min wiring size: 500 nm
- Min spacing: 700 nm

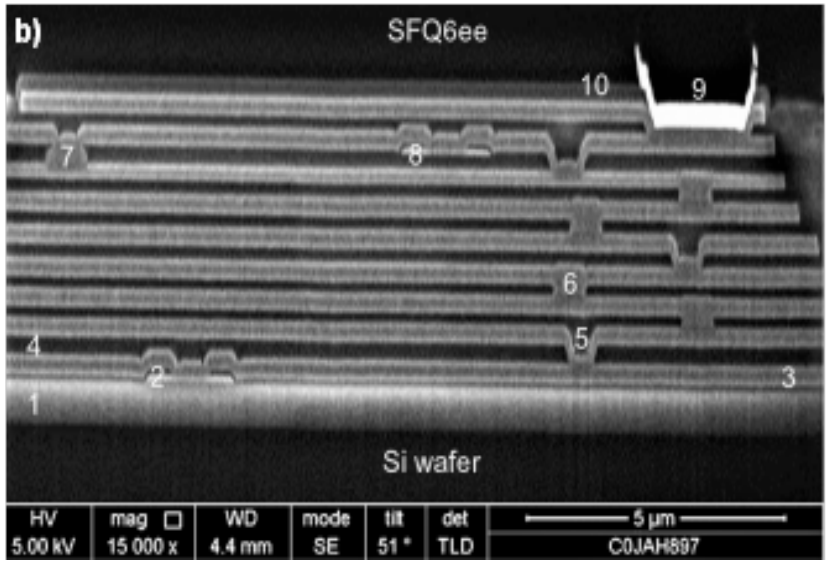
MIT-LL Fabrication Process: Nodes SFQ5ee and SFQ6ee

9-layer node SFQ5ee, 2015



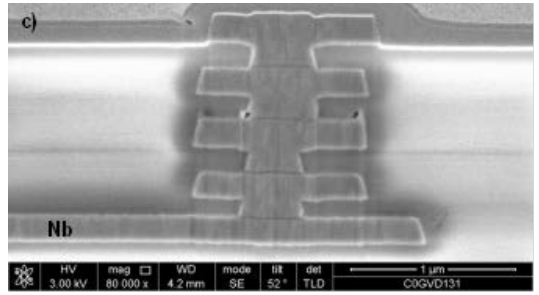
- No. of superconducting layers: 9
- Nb wiring layers: 8
- Kinetic inductors: 1 (Mo_2N)
- Resistors: 2 Ω/sq or 6 Ω/sq
- Min wiring linewidth: 350 nm
- Etched vias: 500 nm

10-layer node SFQ6ee, 2016



- No. of superconducting layers: 10
- Nb wiring layers: 9
- Kinetic inductors: 1 (Mo_2N)
- Resistors: 2 Ω/sq or 6 Ω/sq
- Min wiring linewidth: 350 nm
- Etched vias: 350 nm

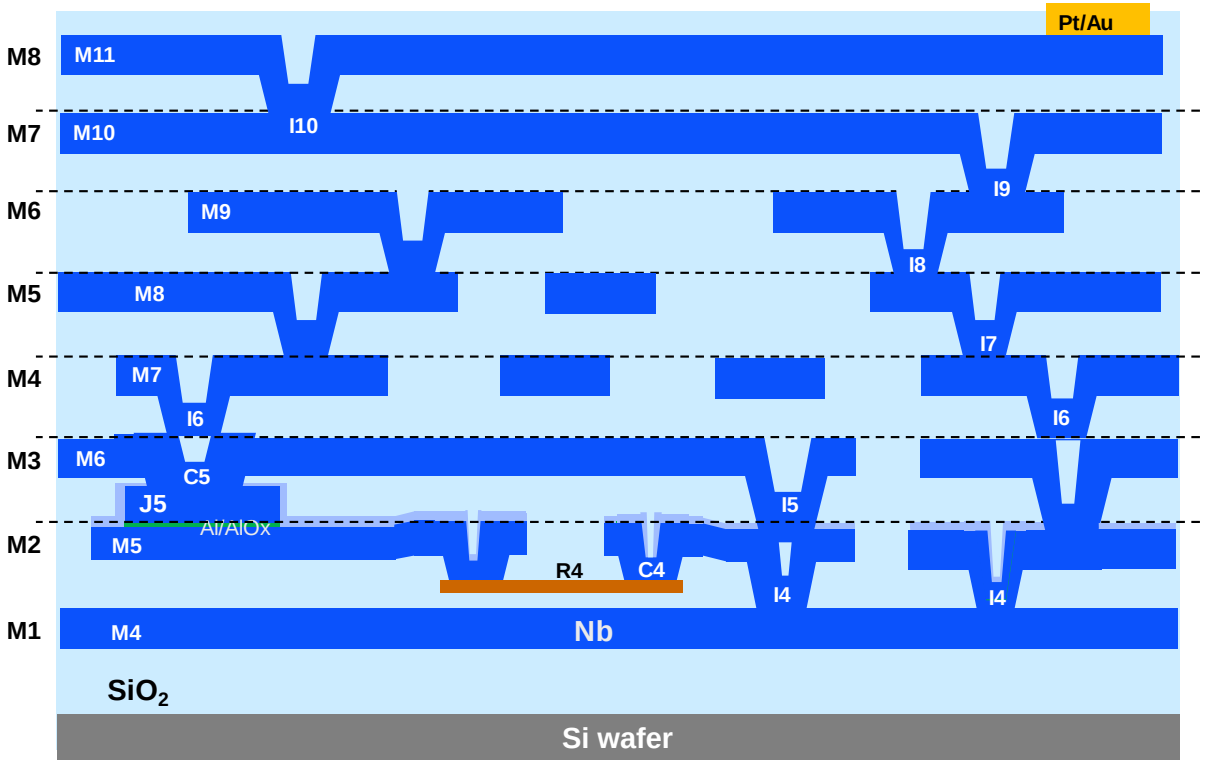
350-nm stacked stud vias in SFQ6ee



SC2 Process Features and Cross Section

- **Process salient features:**
  - 8 niobium layers, 1 JJ layer
  - JJ layer at the bottom above one solid ground plane
  - Resistor layer is interconnected by trilayer base electrode
  - Resistor options: 2 (Mo), 6 (MoN_x), and 10 Ω/sq (MoN_x)
- **Minimum feature sizes:**
  - 0.60 μm min JJ
  - 0.15 μm for Nb wires
  - 0.25 μm min spacing
  - 0.40 μm for R4 resistor
  - 0.35 μm for etched vias
  - 0.2 μm via surround
  - Etched vias with two-high stacking allowed

Our newest process for addressing challenges at and below 250-nm linewidth

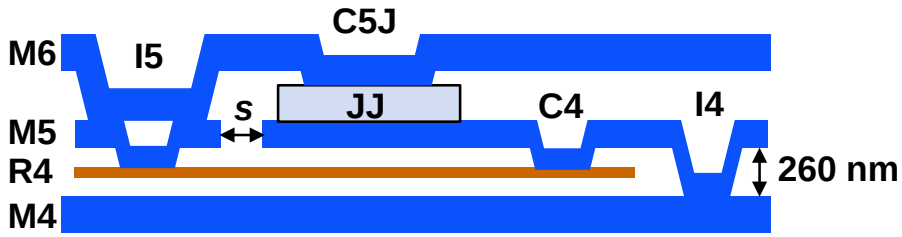


- Thickness of all niobium layers, but M5: 200 nm
- Junction base electrode, M5, after anodization: 135 nm
- Thickness of all dielectric layers, but I4 and I5: 200 nm
- Thickness of I4 and I5 dielectric: 260 nm
- Resistor R4 (Mo or MoN_x): 40 nm

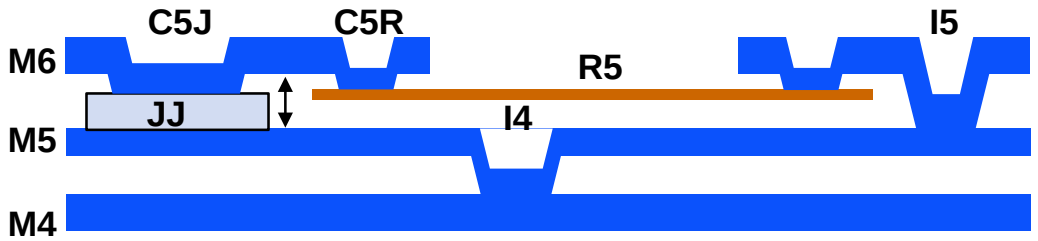
Shunted Junctions in SC2 and SFQ*ee Processes

- The SC2 process and the 'standard' SFQ*ee processes are similar but have several differences
- Resistor layer placement
  - At JJ counter electrode level in SFQ*ee process
  - Below the base electrode in SC2 process
  - In SC2, resistor can be directly under the JJ
- Resistor layer topography is removed
  - Planarized by CMP in SC1 and SC2
  - Not planarized in SFQ*ee
- Total area of a resistively shunted junction
  - In SC2: Shunt with two vias + I5 via
  - In SFQ*ee: Shunt with two vias + JJ + I5 via
- RSJ area in the SC2 process can be 30% smaller than in the SFQ6ee process with the same feature sizes

Shunted Junction in SC2 Process



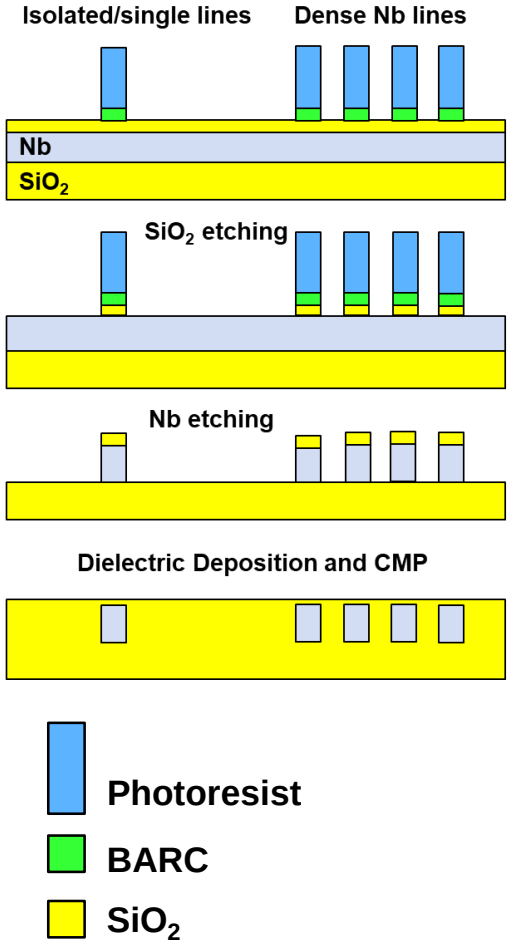
Shunted Junction in SFQ*ee Process

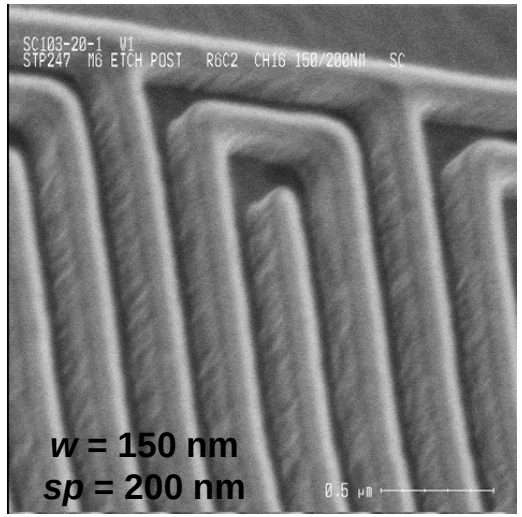


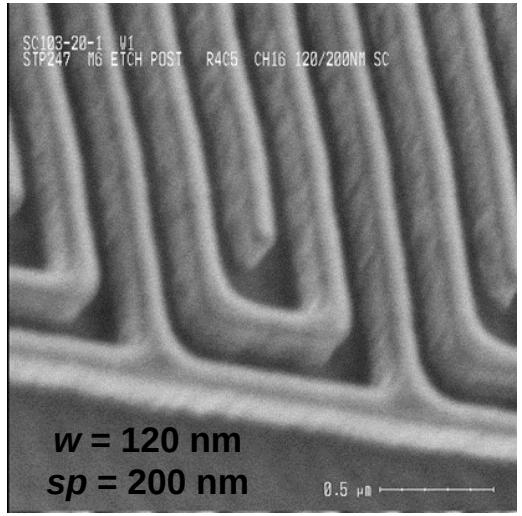
1-μm critically damped JJ; all dimensions are to scale

Fabrication Process and Details

- The fabrication process is very similar to MIT LL standard process SFQ5ee utilizing 248-nm photolithography and high-density plasma (HDP) etching for definition of all features down to 250 nm, and dielectric CMP for layer planarization
- In the SC2 process, a 193-nm 4x reduction photolithography (ASML PAS 5500 -1100 scanner) is used on critical inductance layers to define all features down to 120 nm
- Because of a high etch rate of a 193-nm photoresist (low selectivity to Nb) in HDP, the image was firstly transferred onto a thin SiO_2 layer deposited on Nb surface to form a 'hard' etch mask
- Thus formed tri-layer etch mask (SiO_2+BARC+photoresists) was used to etch Nb in chlorine-based HDP
- Small dimensions and hard mask process may create a difference in the linewidth of single and dense line due to a difference in the rates even if the photoresist linewidths are the same







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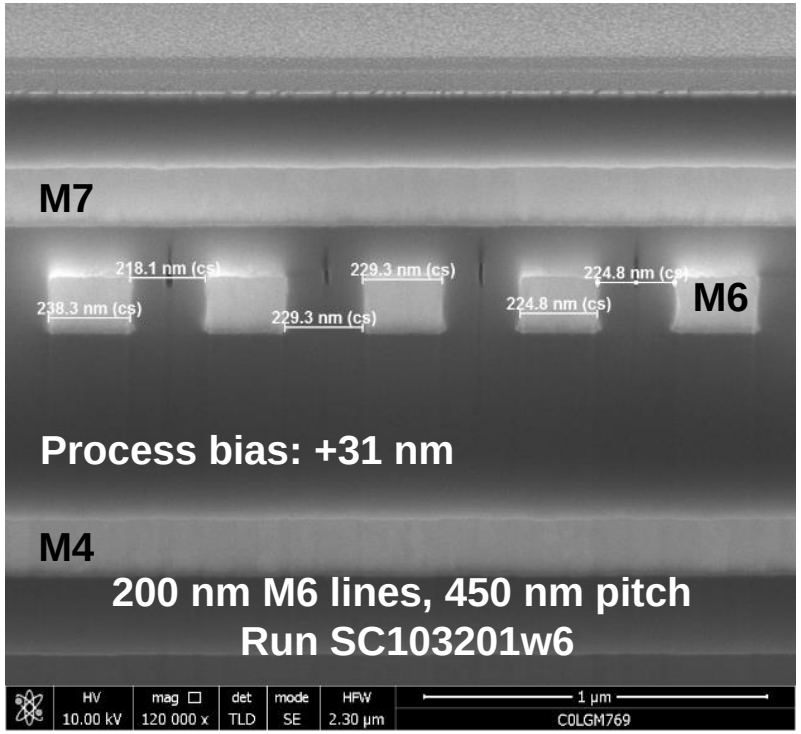
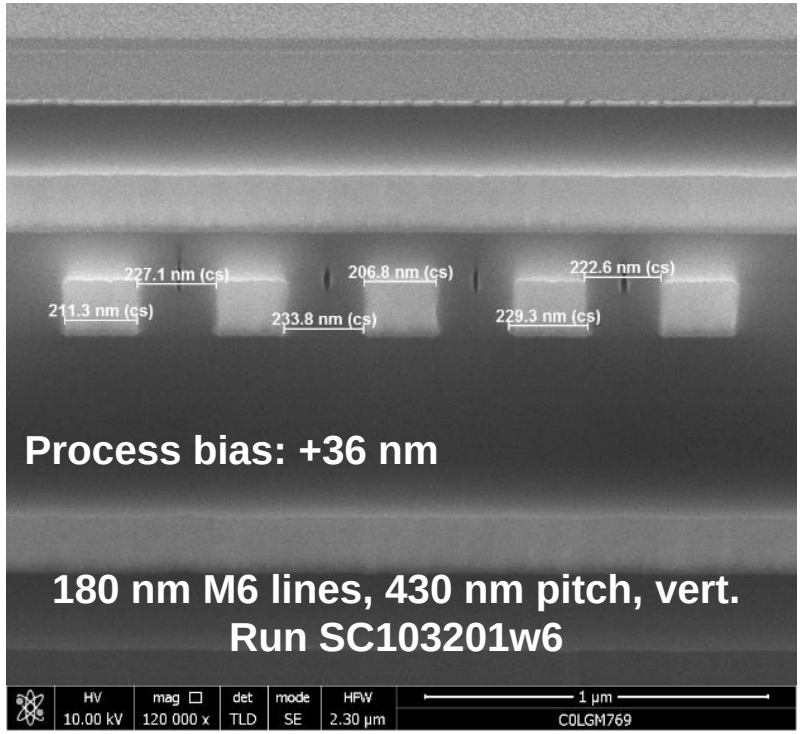
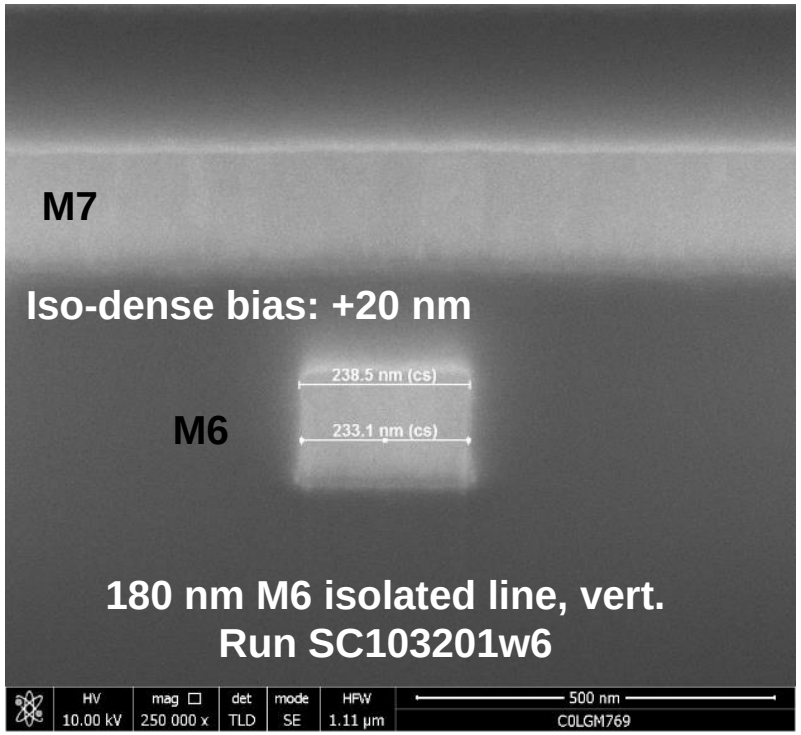
Characterization of Critical Layers of Inductors

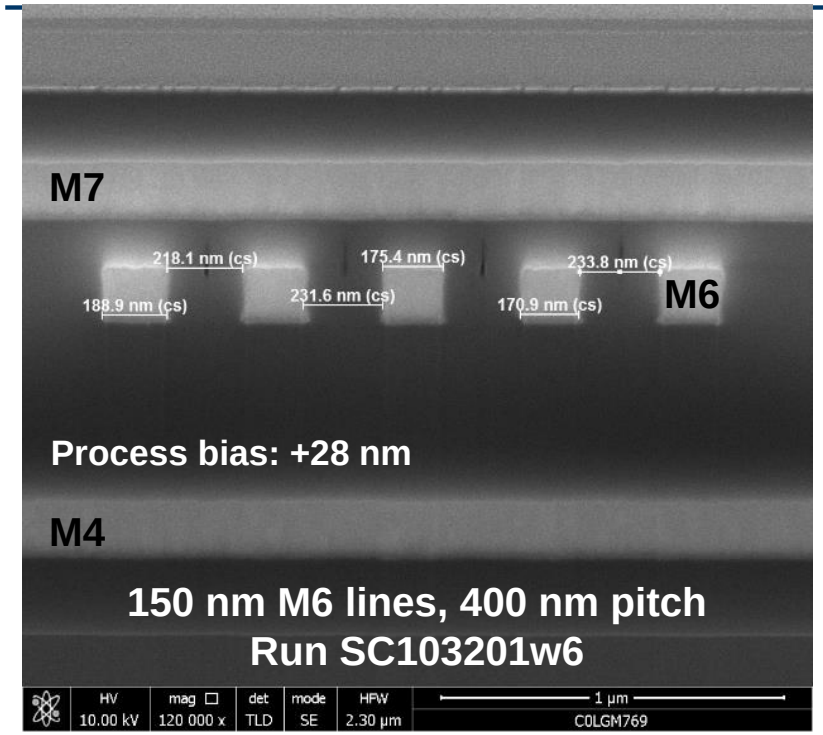


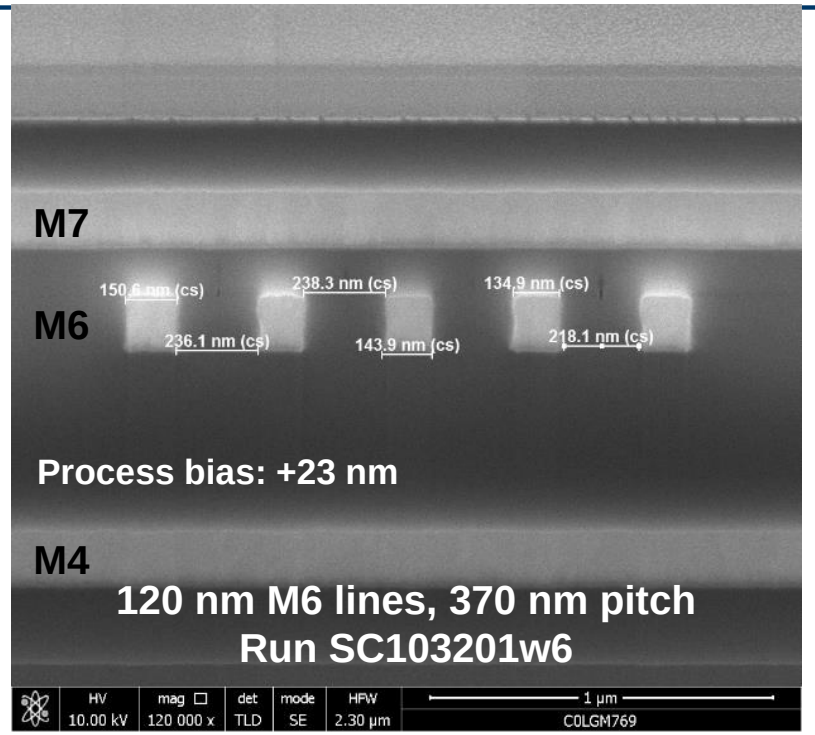


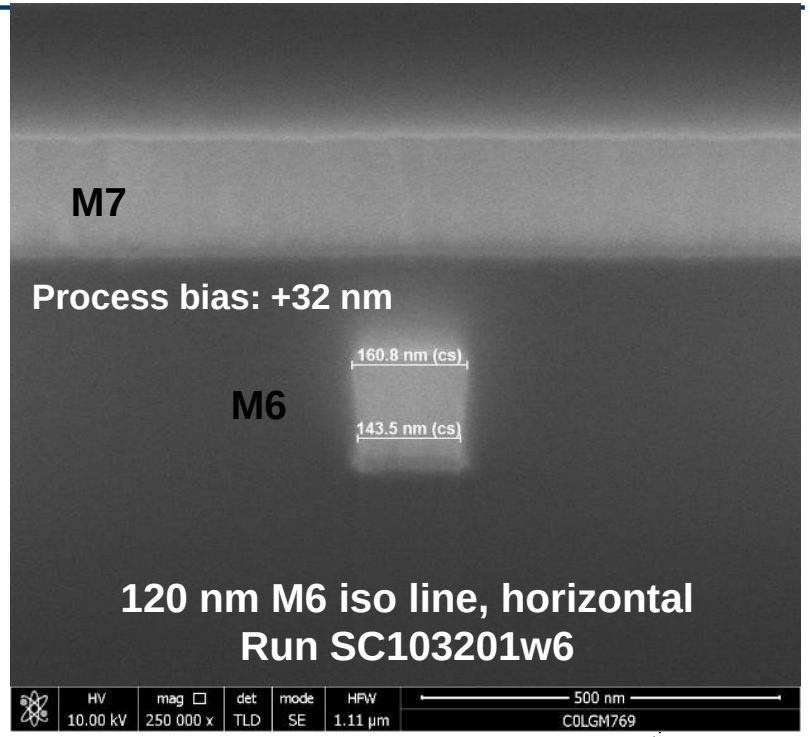


- **Hard mask process gives vertical profile of etched Nb features and a positive process bias: $b = w_w - w_{mask} \sim 30$ nm**
- **HDP SiO_2 CVD process fills narrow gaps (down to 250 nm) between metal lines**

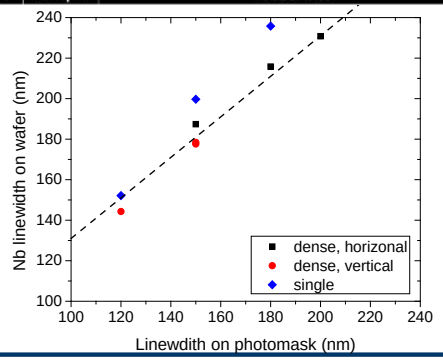
Characterization of Critical Layers of Inductors





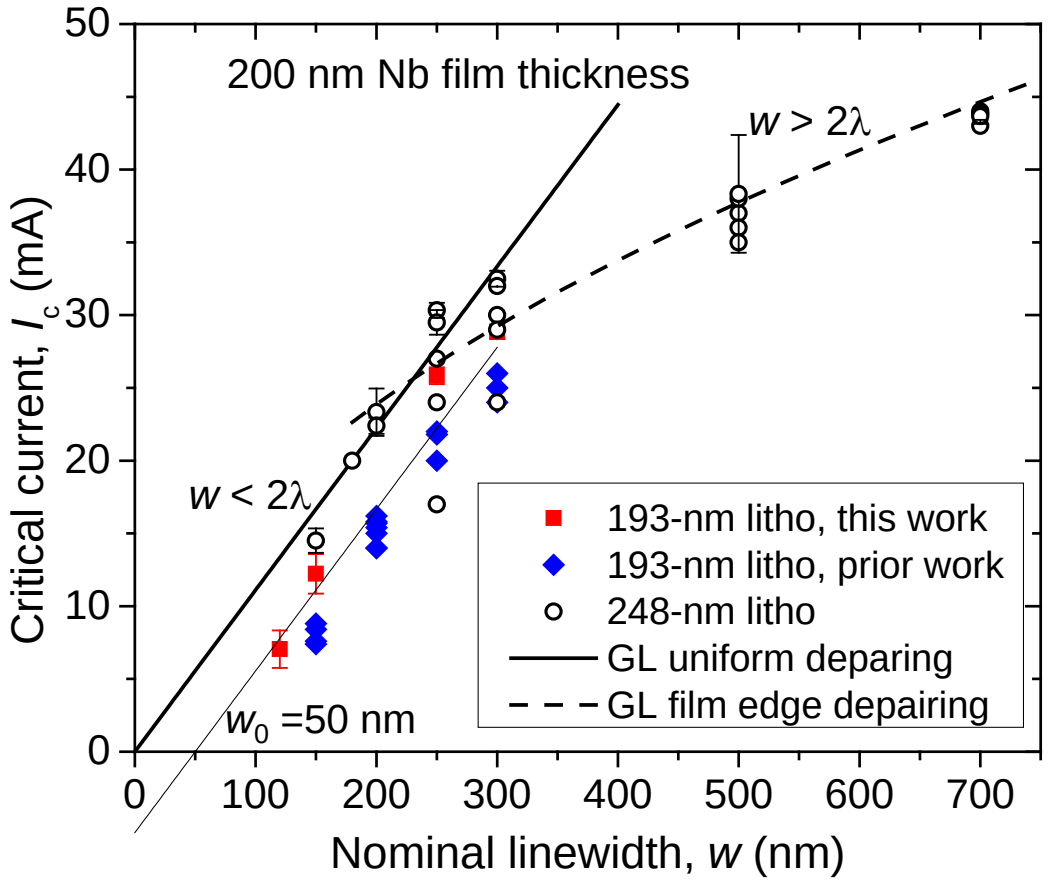


- **The process target linewidth of 150 nm was obtained at 120 nm linewidth on the photomask (design linewidth)**
- **Isolated−Dense linewidth bias is also minimized at this linewidth, decreasing to ~ 9 nm (6%)**
- **This difference is expected to result in a 3.3% larger linear inductance of dense stripline inductors than of the isolated stripline inductors**



Critical Current of Processed Nb Lines

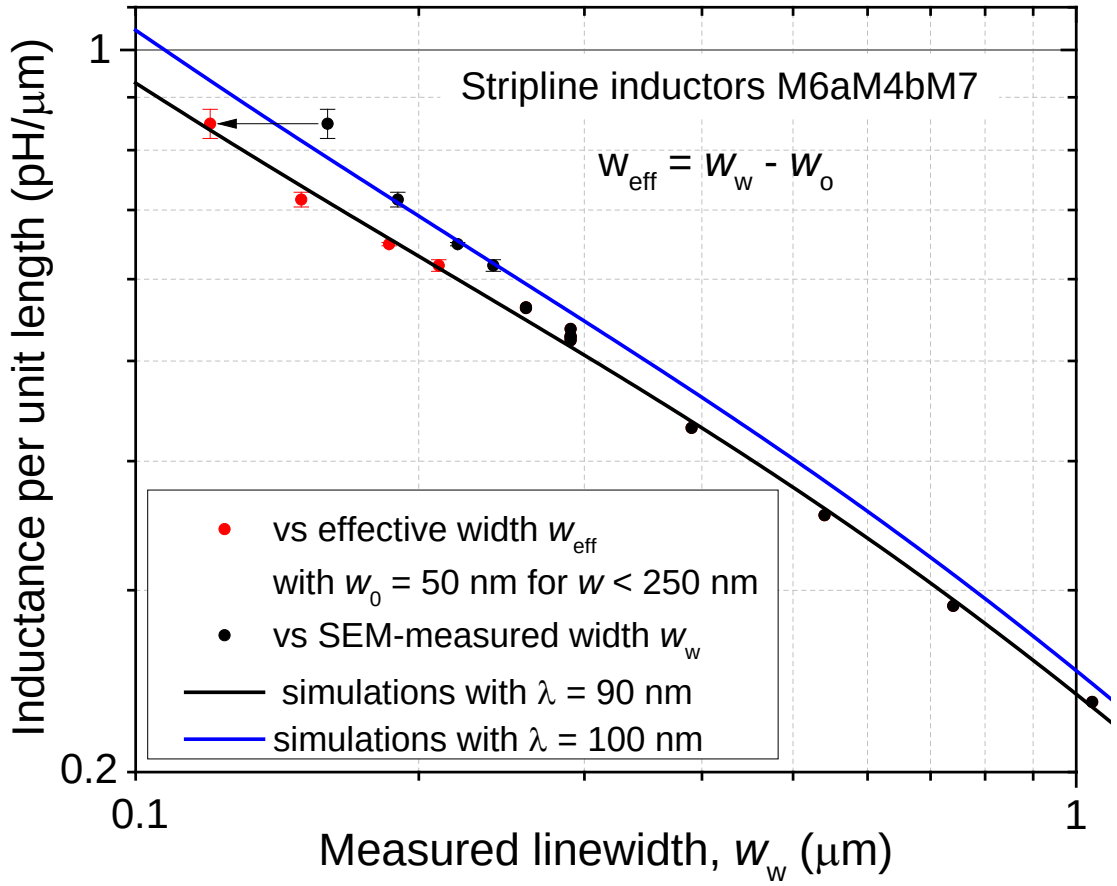
- **Critical currents of all patterned Nb layers were measured using ~ 1 cm long 'snakes' with different linewidths and spacings**
  - **$w \geq 120$ nm for 193-nm photolithography**
  - **$w \geq 150$ nm for 248-nm photolithography**
- **I_c of wide ($w >> 2\lambda$) Nb lines agrees with the value following from the current density reaching Ginzburg-Landau departing density within coherence length ξ distance from the line edges and accounting for current crowding near the line edges, giving $w^{1/2}$ dependence**
- **I_c of narrow lines ($w < 2\lambda$) Nb lines appears to follow the GL departing current with effective linewidth ($w-w_0$), with $w_0 \approx 50$ nm. This suggests existence of a narrow "dead" layer with suppressed superconductivity along line edges.**
- **Superconductivity in narrow Nb lines may weaken as a result of contamination through their side surfaces by hydrogen, consequence of growing as $1/w$ surface to volume ratio. The thickness of this contaminated surface layer appears to be ~ 25 nm.**
- **I_c values are sufficient for applications in VLSI digital circuits with the SC2 process target linewidths - well over 5 mA in 150-nm lines and with low spreads**



Critical currents of long snakes on M6 layer at 4.2 K

Inductance of Deep-Submicron Nb Lines

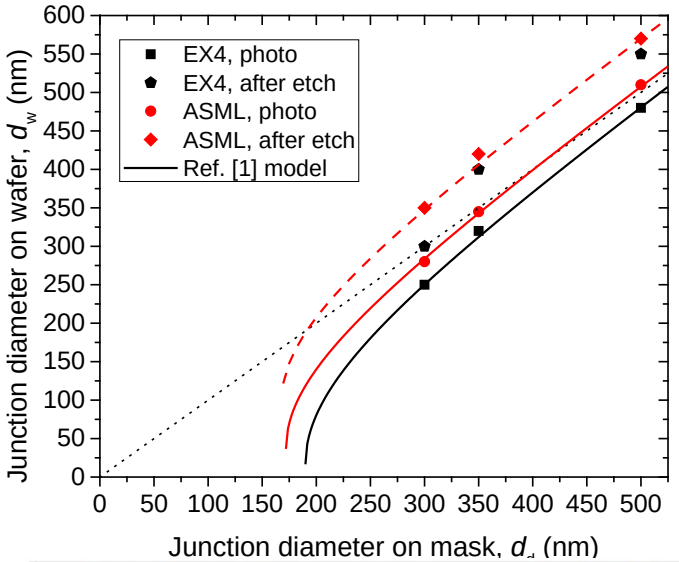
- **The notion of a 'dead' layer along the sidewall of the narrowest Nb lines, making their electrical width smaller than the physical width by $w_0 \approx 50$ nm, does not contradict other measurements, e.g., line inductance**
- **The chart shows the inductance per unit length of straight M6 striplines (between M4 and M7 ground planes) as a function of their physical width on the wafer, w_w measured in SEM using FIB cross sections**
- **The solid black line shows the simulated inductance, which agrees nicely with the measurements in a very wide range of widths studied, up to 4 μm, using the standard value of magnetic field penetration depth, λ = 90 nm**
- **A noticeable deviation from the simulated inductance starts at linewidths below ~ 250 nm, with inductance growing stronger with decreasing the linewidth than in the theory, indicating a smaller electric (magnetic) linewidth or a larger value of magnetic field penetration depth (shown by the blue line) in narrow Nb lines**
- **However, if we use the effective width $w_{eff} = w_w - w_0$ with $w_0 = 50$ nm for the electrical linewidth, a perfect agreement with the simulations is completely restored**

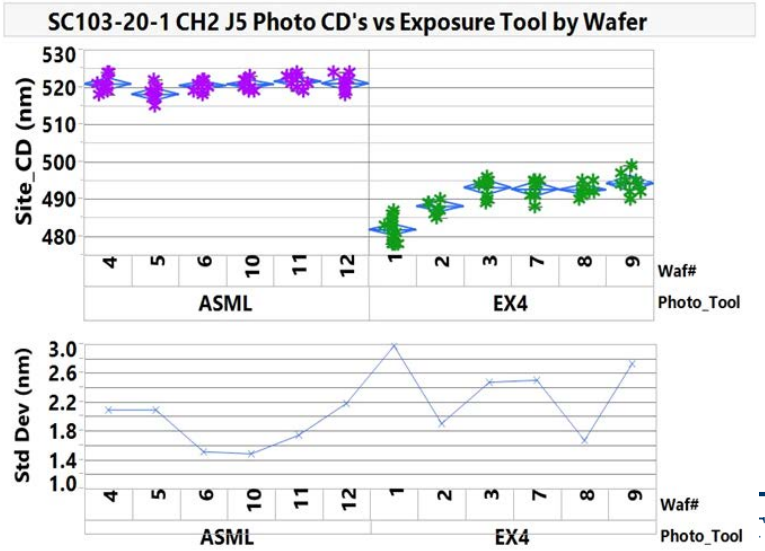


https://asc2020.ipostersessions.com/default.aspx?s=FA-AE-82-7F-BE-19-7D-F5-51-B4-35-86-E8-CF-E8-47&guestview=true

Josephson Junction Phtolithography

- **Photolithography processes with exposure using 248-nm wavelength (Canon FPA-3000 EX4 5x-reduction stepper) and 193-nm wavelength (ASML 5500-1100 4x-reduction scanner) were optimized for printing circular junctions with 500 nm design (on mask) diameter**
- **Size rollover on approaching the minimum printable size (cut-off) d_c, is a well-known photoresist-related effect studied in detail in [1] for the EX4 exposure**
- **193-nm lithography, theoretically, has almost a factor of two smaller cut-off size and should allow for printing smaller junctions**
- **Unfortunately, the etch rate of a 193-nm photoresist used (JSR AR1682J) is much higher than of the 248-nm photoresists. Therefore, almost 2x thicker resist (540 nm vs 395 nm) and a hard SiO_2 mask need to be used to withstand Nb counter electrode (JJ) etching in HDP, compromising resolution**
- **Nevertheless, wafer-scale critical dimension (CD) uniformity ($1\sigma_{wafer} \approx 1.4 – 2.0$ nm) and wafer-to-wafer repeatability of the 193-nm photolithography was somewhat better than for the 248-nm photolithography ($1\sigma_{wafer} \approx 1.6 – 3$ nm) due to more advanced features of the ASML tool (e.g., dynamic focusing)**

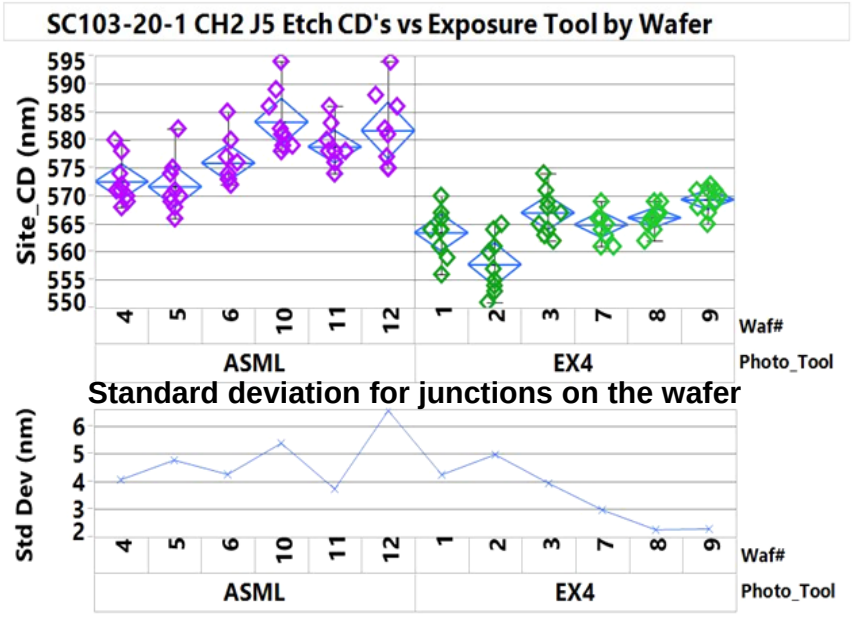




[1]. S.K. Tolpygo et al. IEEE TAS 25, 1101312 (2015)
https://ieeexplore.ieee.org/abstract/document/6967749

Josephson Junction Etching

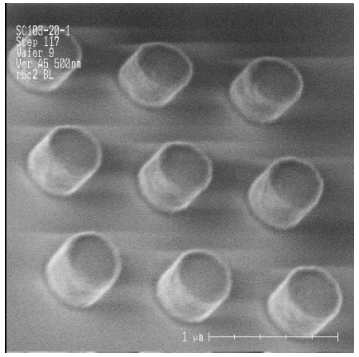
- After junction etching, JJ diameter spreads (1σ) typically increase by ~ 2x in comparison with the post photolithography CD spreads
- However, the increase in etched Nb counter electrode CD spreads is smaller for 248-nm resist process than for 193-nm resist, compensating the initially larger 248-nm photoresist CD spreads
- This may be explained by faster ASML resist erosion during the etch and heavier formation of 'veils-fencing' on ASML wafers due to a thicker resist
- As a result, JJ area spreads for etched 500-nm junctions are about the same for both tools. However, ASML has lower spreads for smaller JJs



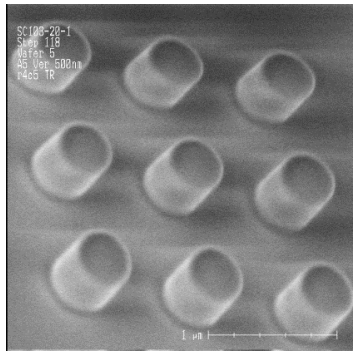
Photoresist mask before etching

JJs after etching

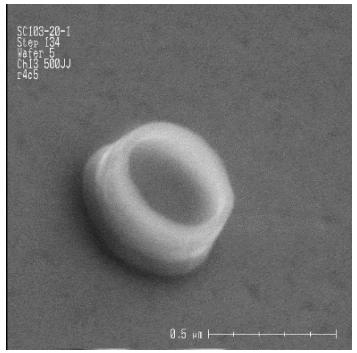
500-nm JJs w9 EX4



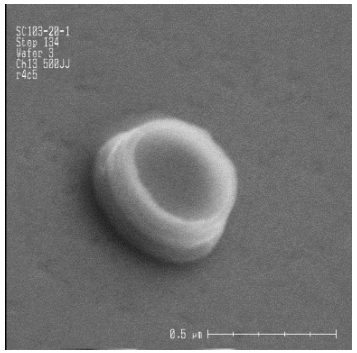
500-nm JJs w5 ASML



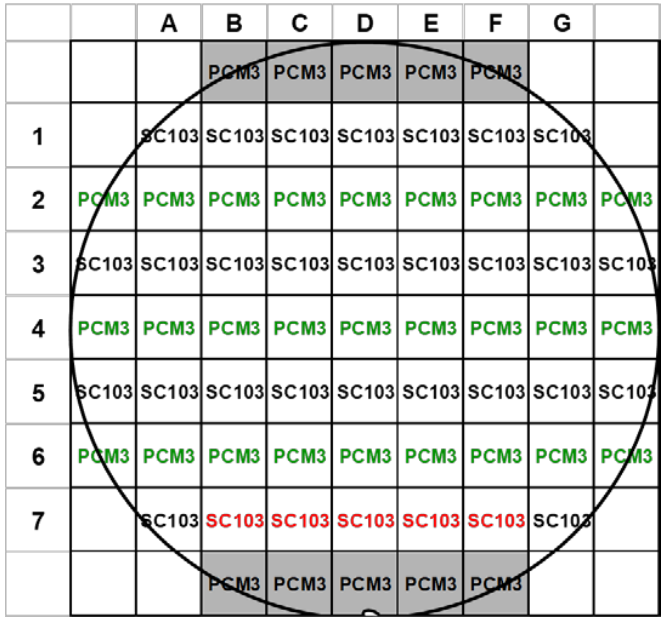
500-nm JJ w5 ASML



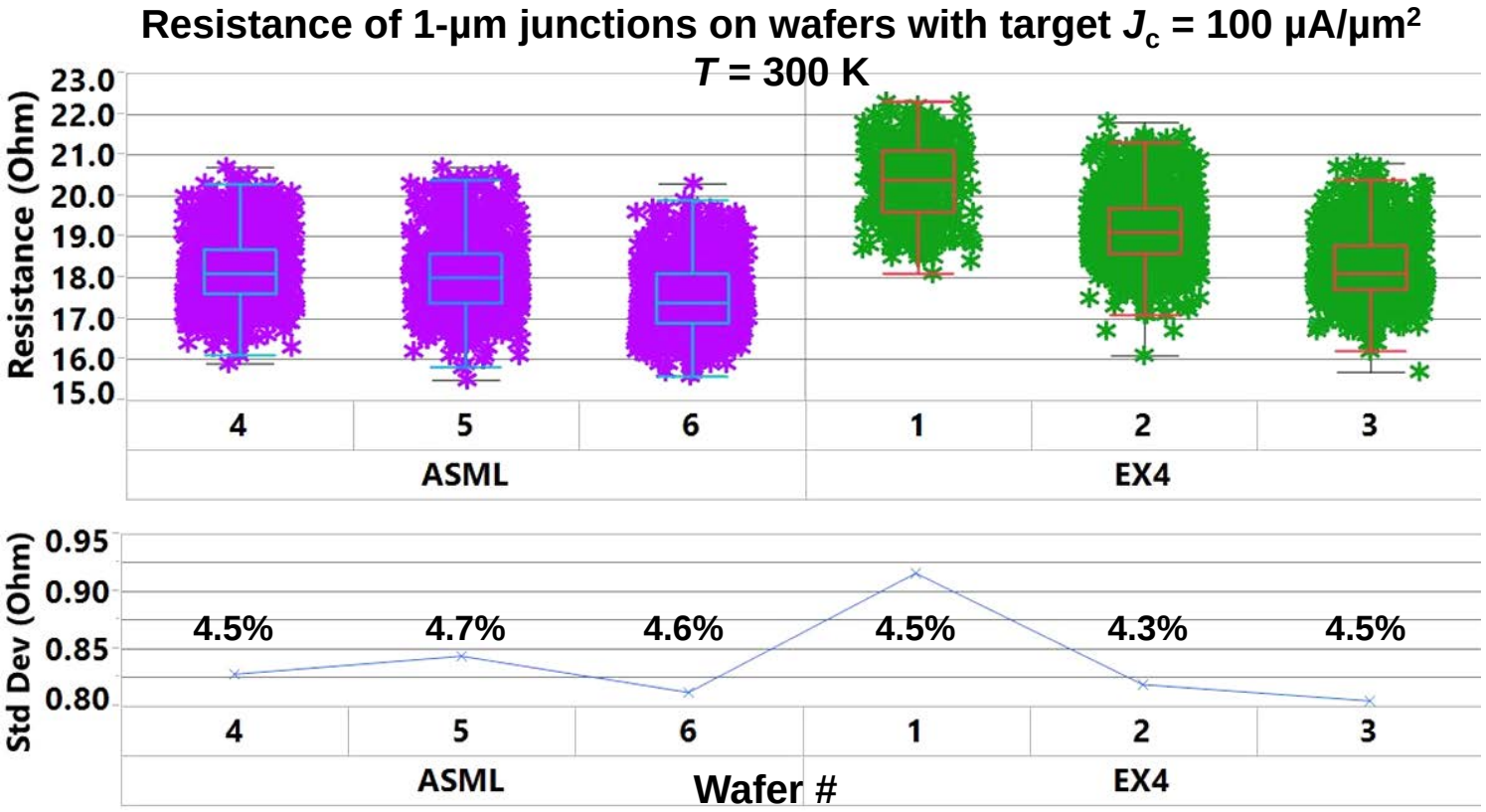
500-nm JJ w9 EX4



Josephson Junction Testing Results



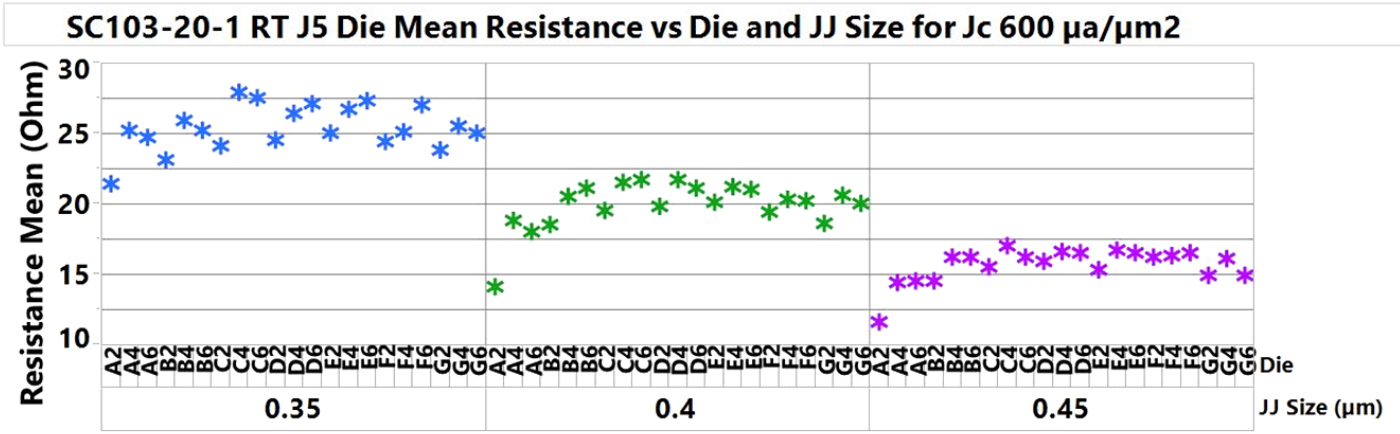
PCM and test circuits die locations

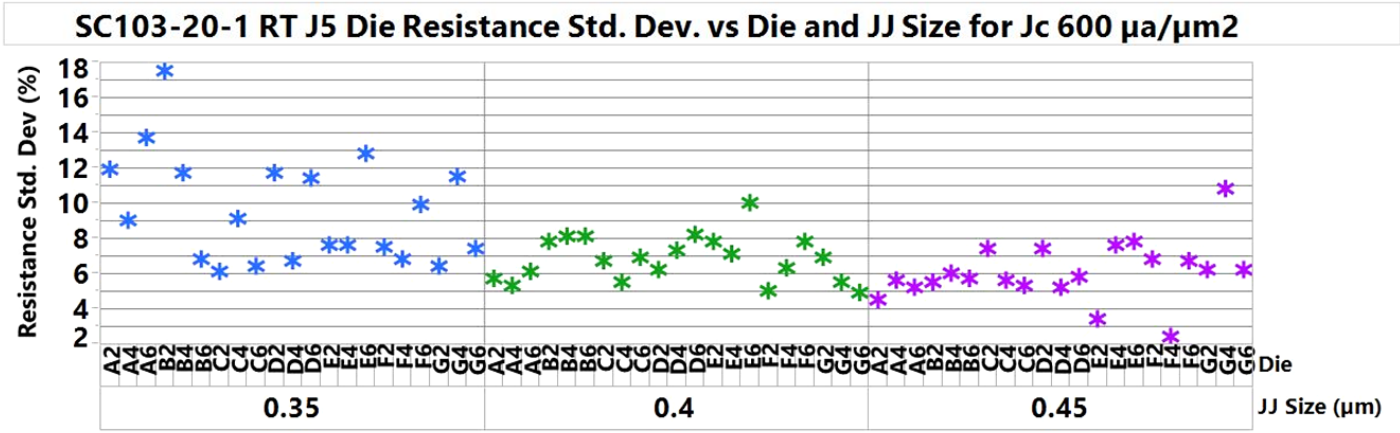


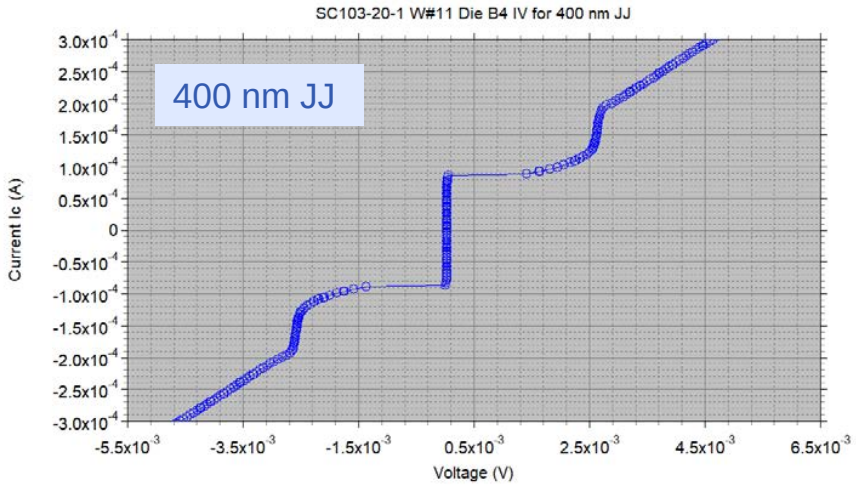
- Resistance of junctions with sizes from 0.30 μm to 4.0 μm was measured at 300 K on all PCM3 and SC103 die, 45 die total, using a semi-automated wafer prober
- For large JJs, resistance distribution characterizes mainly J_c (tunnel conductance) distribution on the wafers and is clearly independent of the photolithography tool used for junction definition

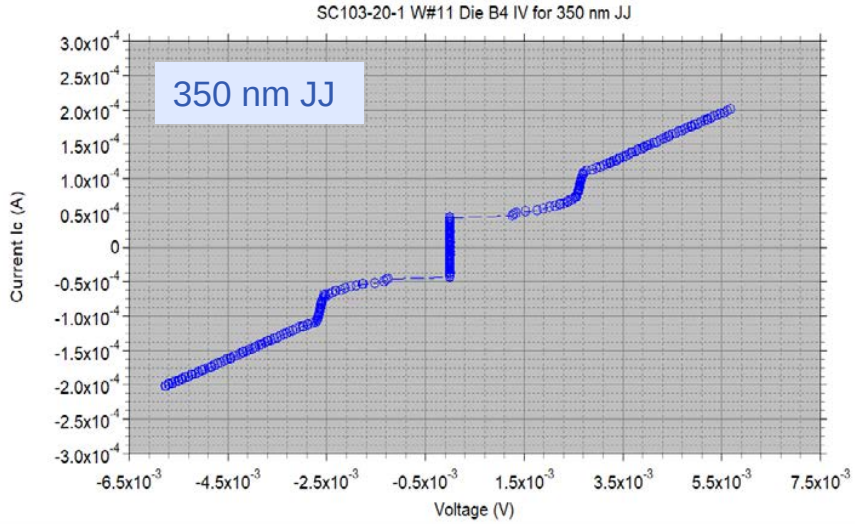
Characteristics of Self-Shunted 600-μA/μm² Junctions

- **The use of 193-nm photolithography (ASML) allows us to better define JJs with sizes below 500 nm, which is essential for the process with self-shunted high-J_c junctions**





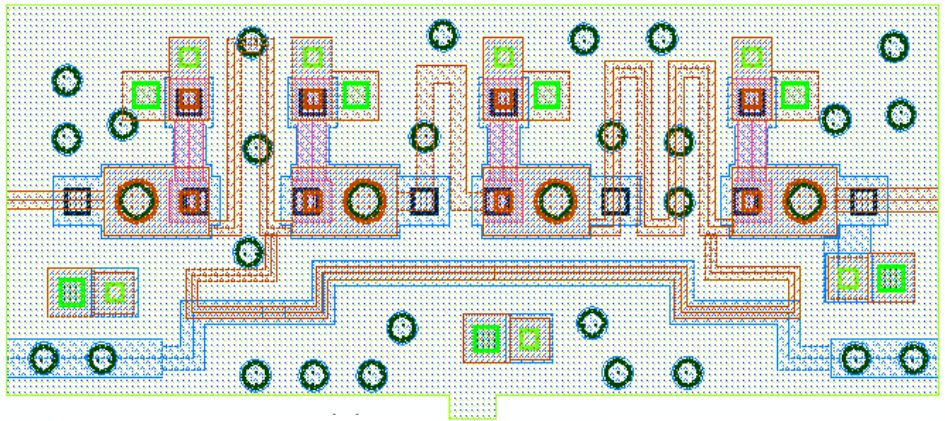




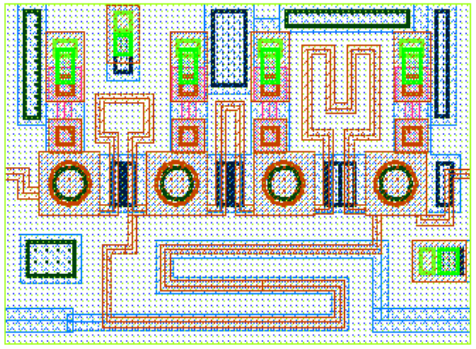
IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), No. 49, March 2021.
Invited presentation Wk1EOr3B-01 given at the virtual ASC 2020, October 29, 2020.

SCE Scaling From Benchmark Circuits

Sh. Reg. cell in 500-nm node: 40 μm x 17 μm = 680 μm²

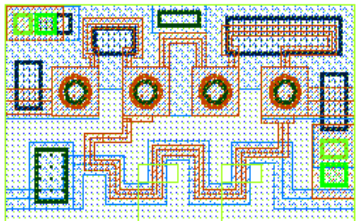


350-nm node



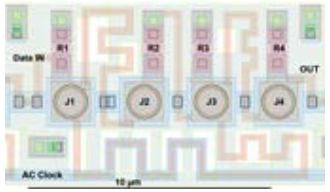
20 μm x 15 μm = 300 μm²
Density: 1.33×10⁶ JJ/cm²

350-nm node



Self-shunted JJs: J_c = 500 μA/μm²
15 μm x 10 μm = 150 μm²
Linewidth: 350 nm
Density: 2.67×10⁶ JJ/cm²

250-nm node



Shown in the same scale

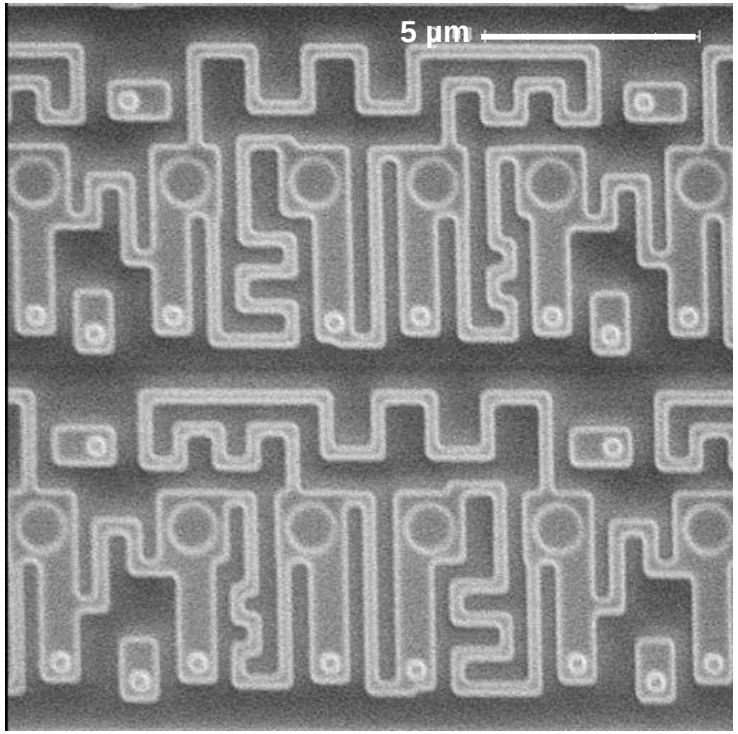
This work:

- **Cell: 12 μm x 8 μm = 96 μm²**
- **Devices: J_c = 100 μA/μm² (resistively shunted JJs)**
- **Linewidth: 250 nm**
- **Density: 4.16×10⁶ JJ/cm²**

- **We use ac-biased shift registers as benchmark circuits to characterize technology nodes: circuit density, defect density, parameter spreads, yield**
- **Linewidth reduction clearly helps increasing circuit density**
- **Implementing self-shunted (high-J_c) JJs instead of RSJs increased JJ density by ~ 2x in the SFQ5ee 350-nm technology node**
- **Another 1.6x increase has been obtained by transitioning to 250-nm SC1 node. Fully operational 91180-bit (~365,000 JJs) shift registers have been demonstrated**

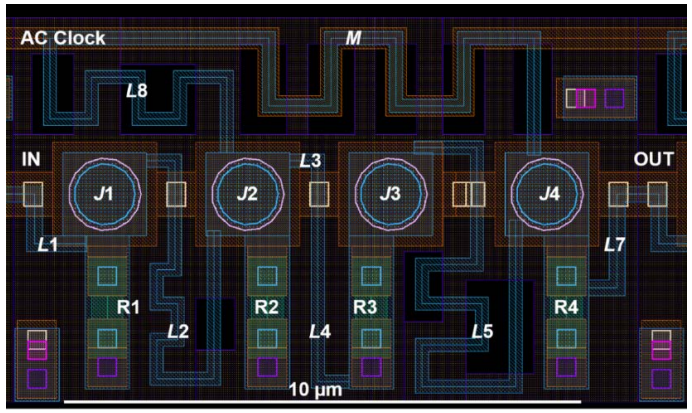
AC-Clocked Shift Register With RSJs and 250-nm Inductors

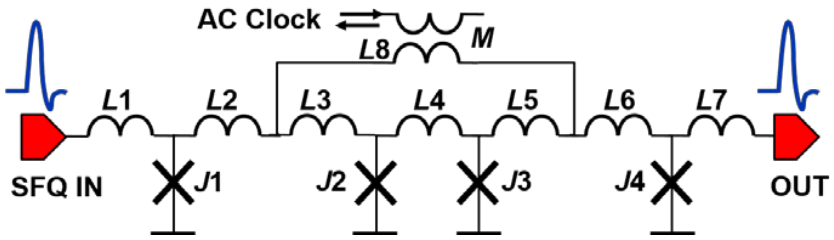
SEM image of fabricated circuit



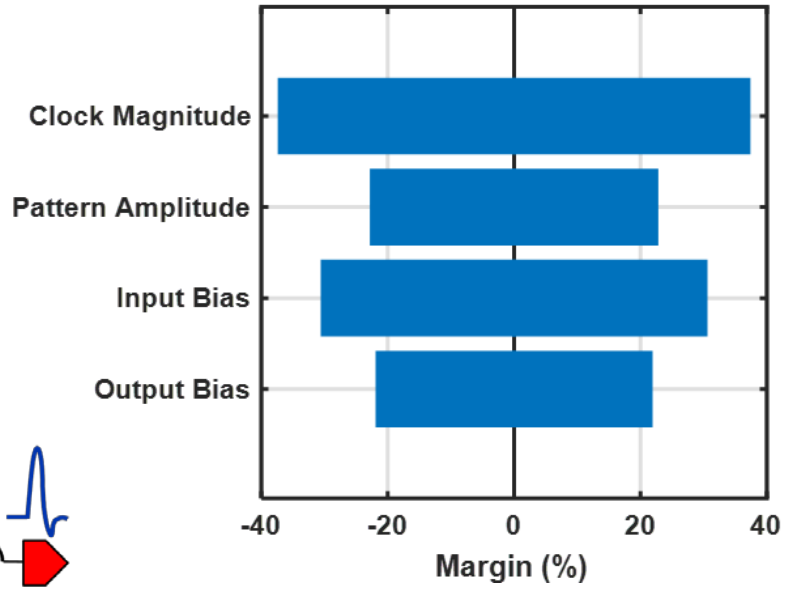
- Process J_c: 100 μA/μm²
- Cell size: 12 μm x 8 μm
- Resistively shunted junctions
- Number of cells: 91180

Shift register unit cell and circuit diagram





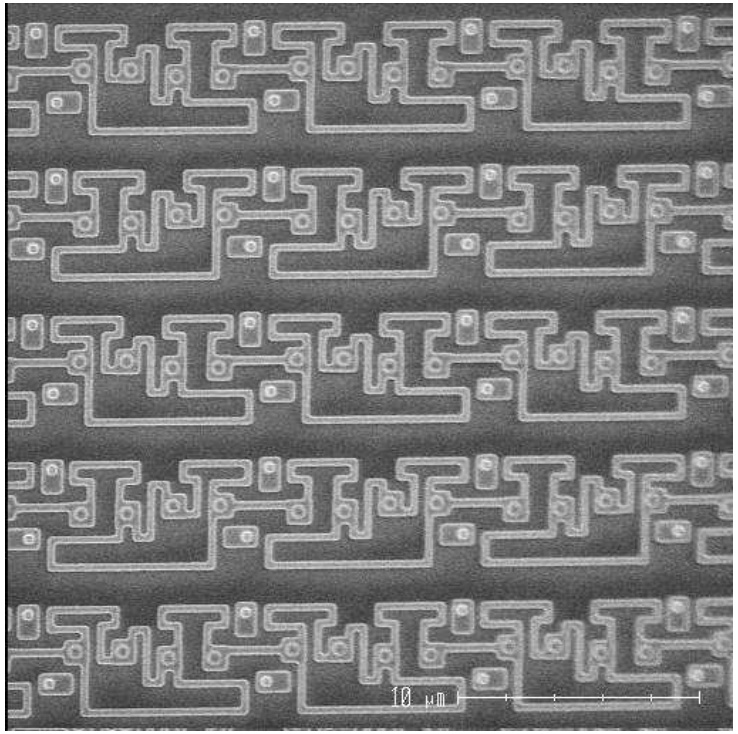
- Number of junctions: 365,000
- JJ density: 4.16·10⁶ JJ/cm², >3x increase over the SFQ5ee
- Circuit area: 8.68 mm² (~ 2.9 mm x 3 mm)

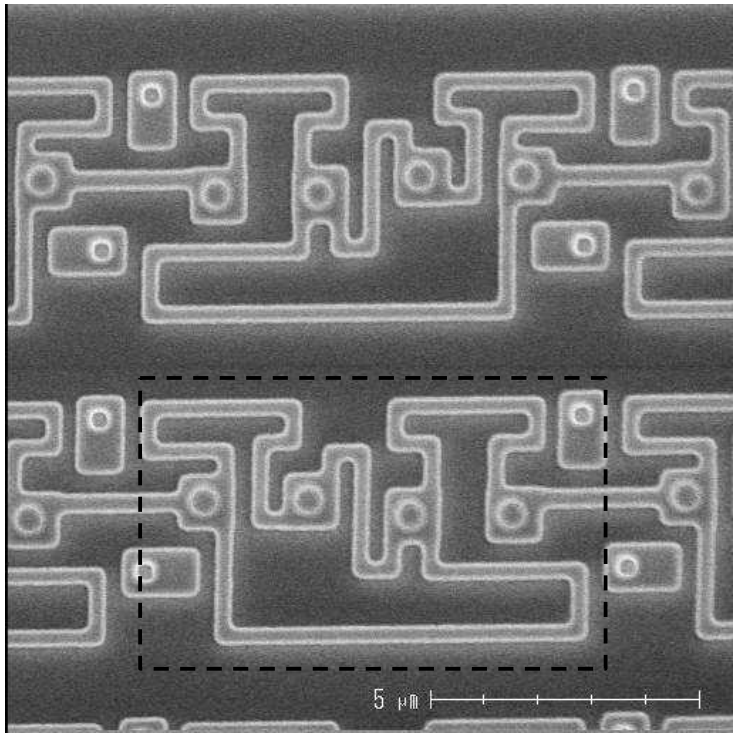


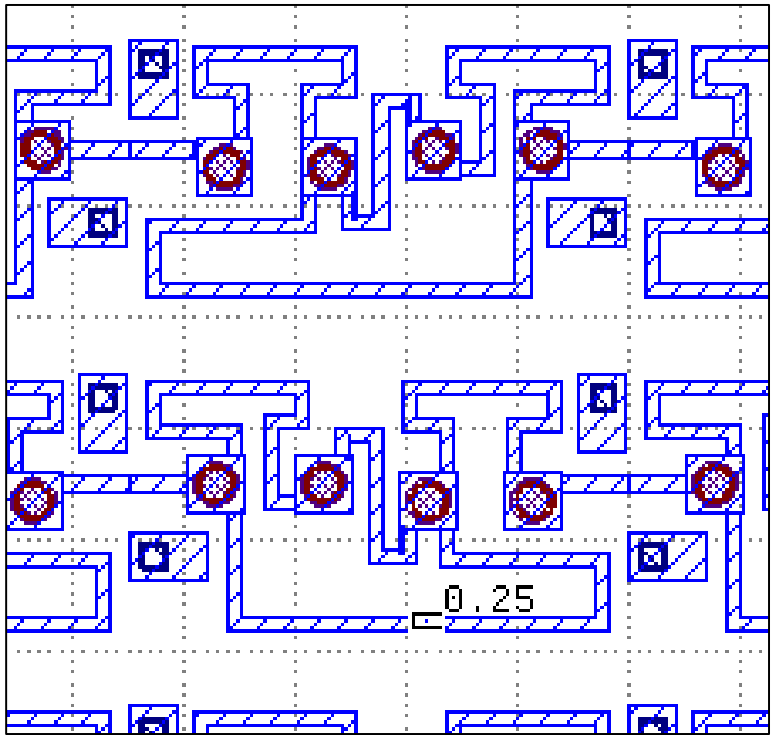
Operating margins measured on a 936-bit section of the register

Shift Registers With Self-Shunted (600 μA/μm²) JJs

SEM images of the fabricated ShReg (run SC103201 ch11) with 250-nm inductors





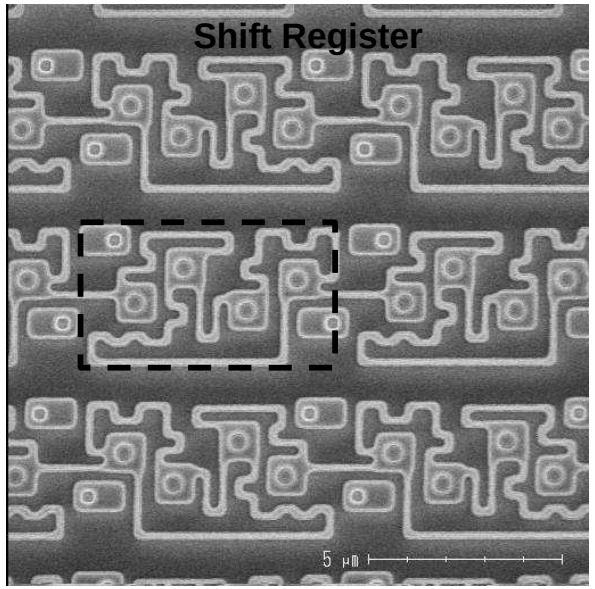


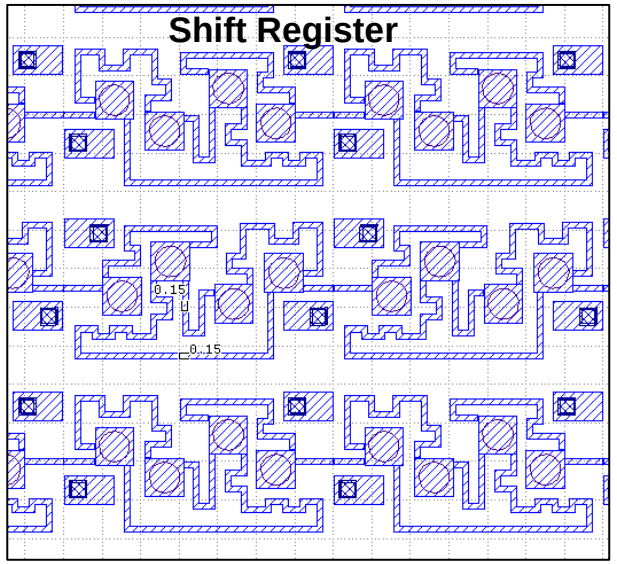
- J_c = 600 μA/μm² (self-shunted JJs)
- Cell dimensions: 9 μm x 6 μm = 54 μm²
- ~2x reduction in area with respect to the cell with resistively shunted junctions (RSJ)
- JJ density: 7.4·10⁶ JJ/cm²

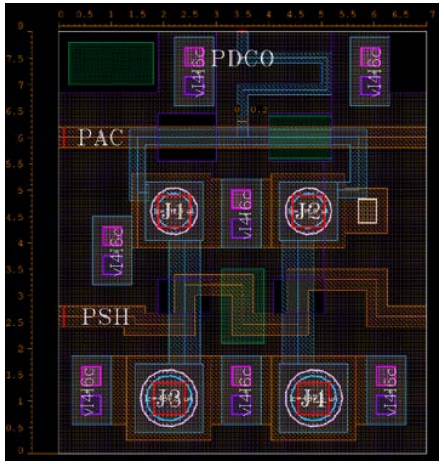
Circuits With Self-Shunted JJs and 150-nm Inductors

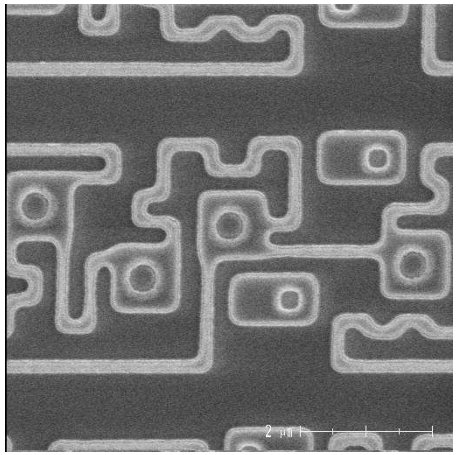
- SC2 Process: 150-nm min linewidth, 250-nm min spacing
- J_c = 600 μA/μm^2
- AC-clocked shift registers
  - Cell dimensions: 7 μm x 4 μm
  - Circuit density: 1.3·10^7 JJ/cm^2
  - 2x increase over 250-nm process
- SFQ basic circuits and cell library
  - DC-SFQ and SFQ-DC converters and JTL
  - Balanced comparators
  - AC-DC bias converters and circuits biased by single flux quanta*
  - QFP cell library
  - Etc.

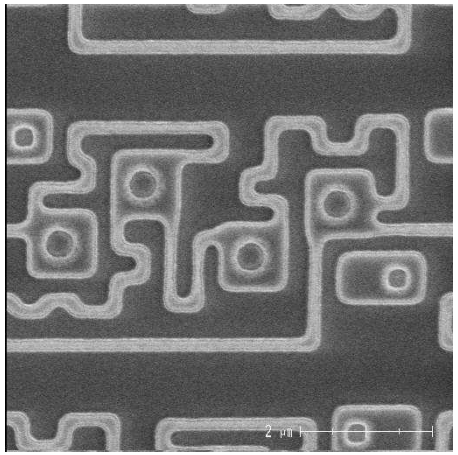
* See V.K. Semenov et al. presentation Wk1EPo2B01 “SFQ Bias for SFQ Digital Circuits” at this ASC2020











Conclusion

- We developed a new 150-nm node of MIT LL process SC2 for superconductor electronics
- Using 250-nm linewidth and J_c = 100 μA/μm^2, we have demonstrated benchmark circuits with 365,000 junctions and density of 4.2·10^6 JJs per cm^2
- Implementation of the self-shunted JJs in this 250-nm node increases circuit density and JJ count by a factor of ~2x to 7.4M JJs per cm^2
- Using 150-nm linewidth and self-shunted junctions with J_c = 600 μA/μm^2 we demonstrated shift registers and other SFQ circuits with density of 1.3·10^7 JJ/cm^2
- Superconductor electronics is on a solid “Moore’s-law-like” path into VLSI
- Main improvements in circuit density came from
  - Reduction of the linewidth of inductors and transformers
  - Reduction of shunt resistor linewidth or elimination of shunt resistors
  - Better circuit optimization which accounts for mutual inductances of all components and allows to minimize the “dark space” between components
- Further progress in the circuit density should come from transitioning to kinetic inductors and to damascene processing for interlayer vias and inductors
- This technology coupled with large superconducting MCM technology should enable complex superconductor electronics systems

Thank You Very Much!

Questions?