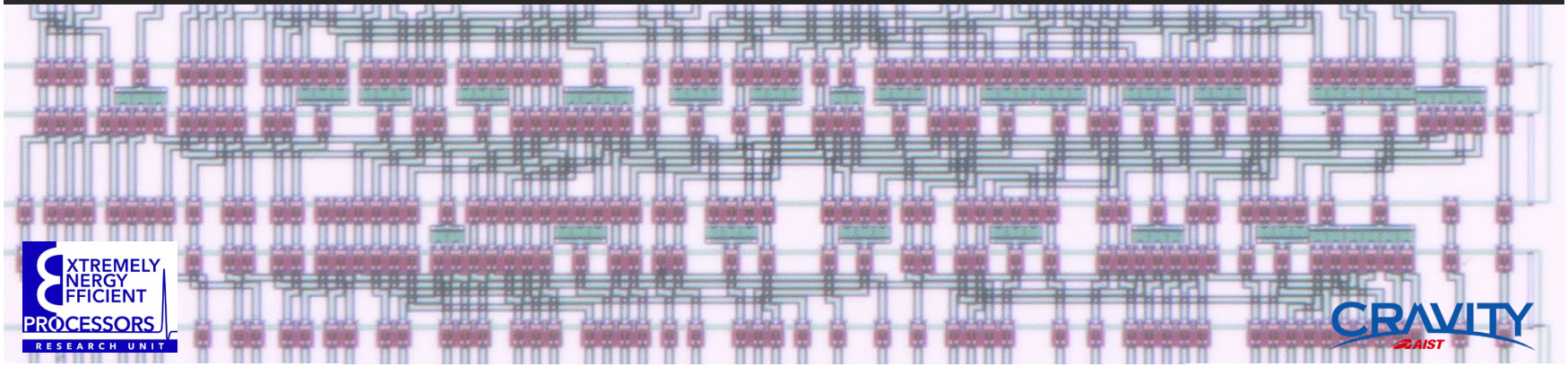
IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), No. 49, March 2021.
Invited presentation Wk1EOr1B-01 given at the virtual ASC 2020, October 27, 2020.

A 4-bit RISC-Dataflow AQFP MANA Microprocessor: Architecture, Design Challenges, and Demonstration

Christopher L. Ayala*
Ro Saito, Tomoyuki Tanaka, Tomohiro Tamura, Naoki Takeuchi, and Nobuyuki Yoshikawa

Yokohama National University, Yokohama, Kanagawa, Japan
**email: ayala-christopher-pz@ynu.ac.jp • chris.ayala@ieee.org*



YOKOHAMA National University
Institute of Advanced Sciences

YNU 横浜国立大学
YOKOHAMA National University

Outline

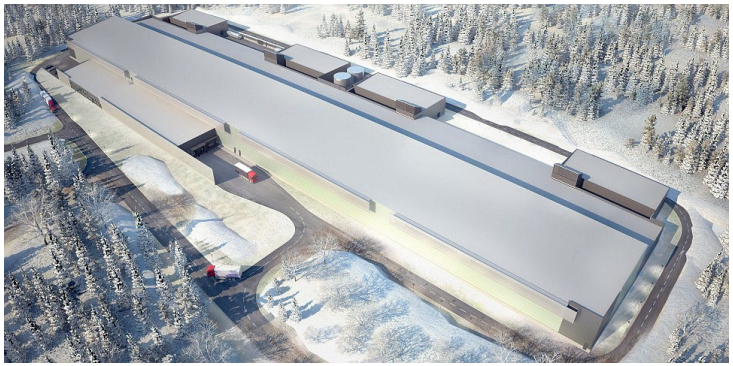
- Motivation and background
- MANA processor
  - Design goals
  - Microarchitecture and ISA
- Tested breakout chips
- MANA prototype chip
- Outlook
- Summary

Motivation

Trend of rising electricity demand of information and communications technology (ICT).

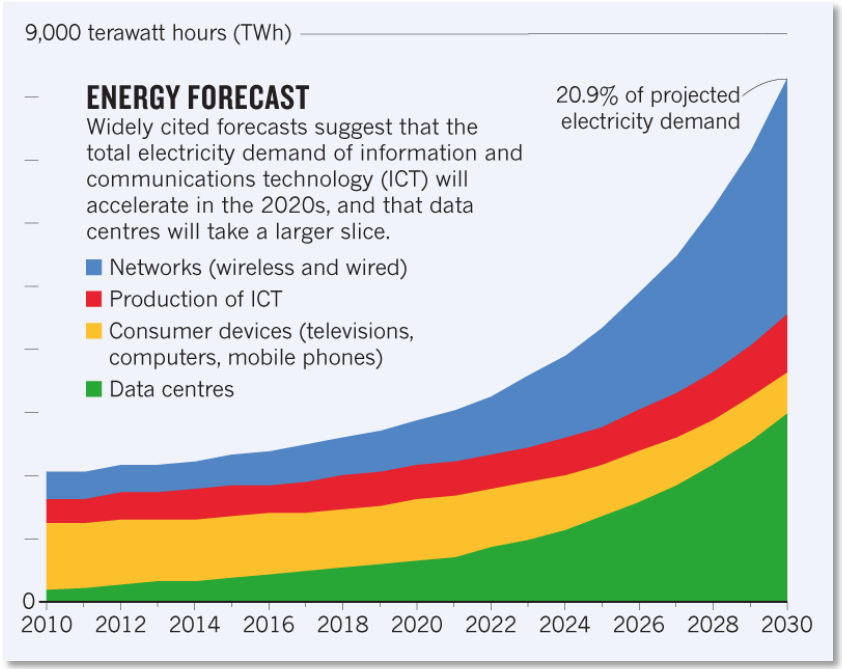
Approaching 10% of the total electric power worldwide in 2020.

Facebook Data Center, Lulea, Sweden



Performance: 27-51 PFLOP/s
Power 84 MW avg* (120 MW max)

D.S. Holmes, ISS 2013, Tokyo, Japan.
http://worldstopdatacenters.com/renewable-energy-output-rankings/



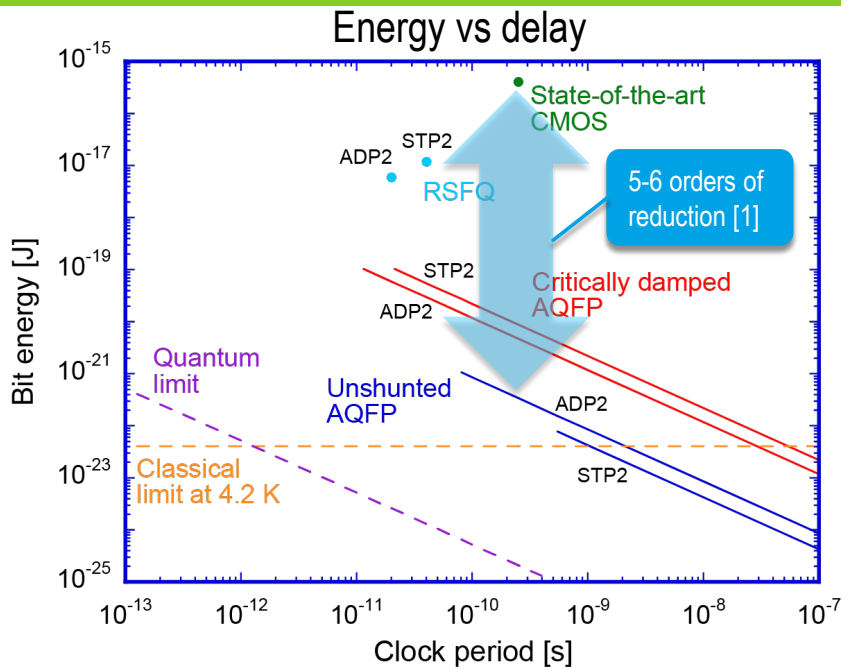
N. Jones, *Nature*, vol. 561, no. 7722, pp. 163–166, Sep. 2018.

Worst-case scenario: ICT could use as much as 50% of global electricity by 2030.

A. S. G. Andrae and T. Edler, *Challenges*, vol. 6, no. 1, pp. 117–157, Jun. 2015.

AQFP logic for computing

- **A**diabatic **q**uantum-**f**lux-**p**arametron (AQFP) logic
  - Extremely small bit energy << $I_c\Phi_0$
    - Very small switching energy due to adiabatic operation
    - 1.4 zJ at 4.2 K in experiment [2]
  - High gain
    - 10-50x gain from μA's of input current
  - High robustness
  - Clock speeds on par with state-of-the-art CMOS logic (5-10GHz)



[1] N. Takeuchi et al., Supercond. Sci. Technol. 26, 035010 (2013).
[2] N. Takeuchi et al., *Appl. Phys. Lett.*, vol. 114, no. 4, p. 042602, Jan. 2019.

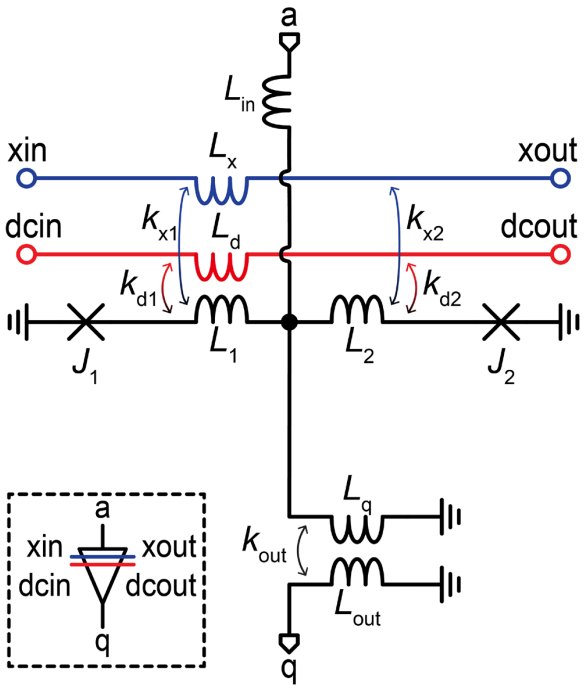
After cooling overhead [2], **~80x more efficient** than 7nm FinFET with V_{DD} = 0.8V [3]

[2] D.S. Holmes et al., IEEE TAS, 23, no.3, (2013)
[3] A. Stillmaker et al., Integration. 58, pp. 74-81 (2017)

AQFP logic a promising candidate for energy-efficient computing.

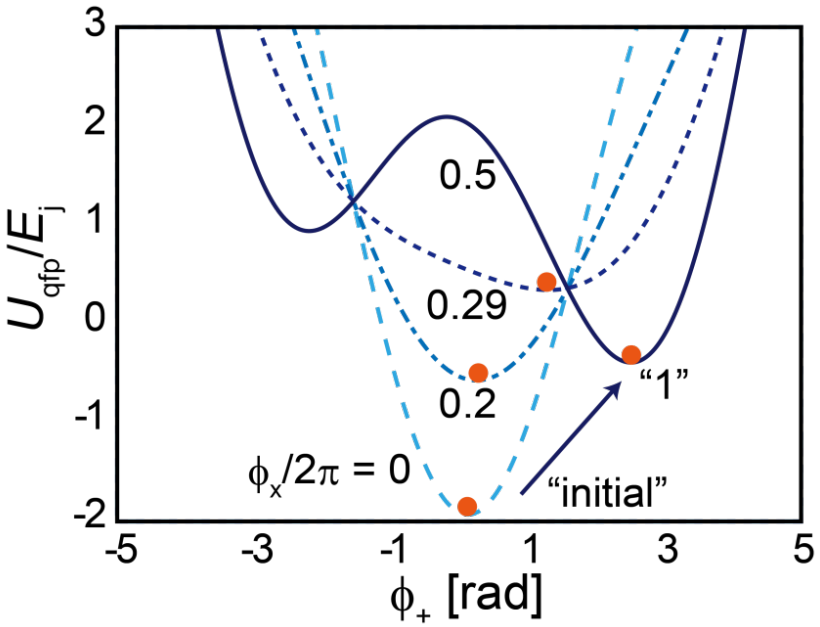
Adiabatic quantum-flux-parametron (AQFP)

AQFP (buffer) schematic



$+I_{in} \rightarrow$ SFQ stored in left loop, logic '1'.
$-I_{in} \rightarrow$ SFQ stored in right loop, logic '0'.

Potential energy of the AQFP



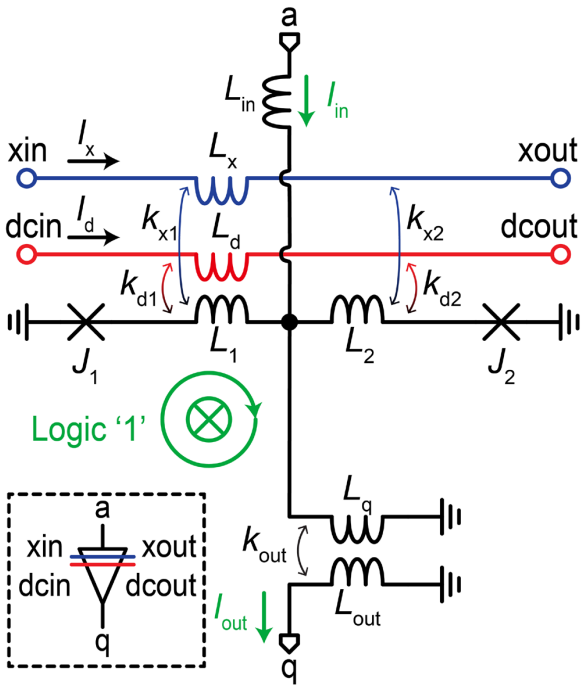
Potential energy changes adiabatically during a switching event.

Operation is based on conventional QFP gates [1].
Switching energy can be reduced below $I_c\Phi_0$
by using AC excitation currents, I_x.

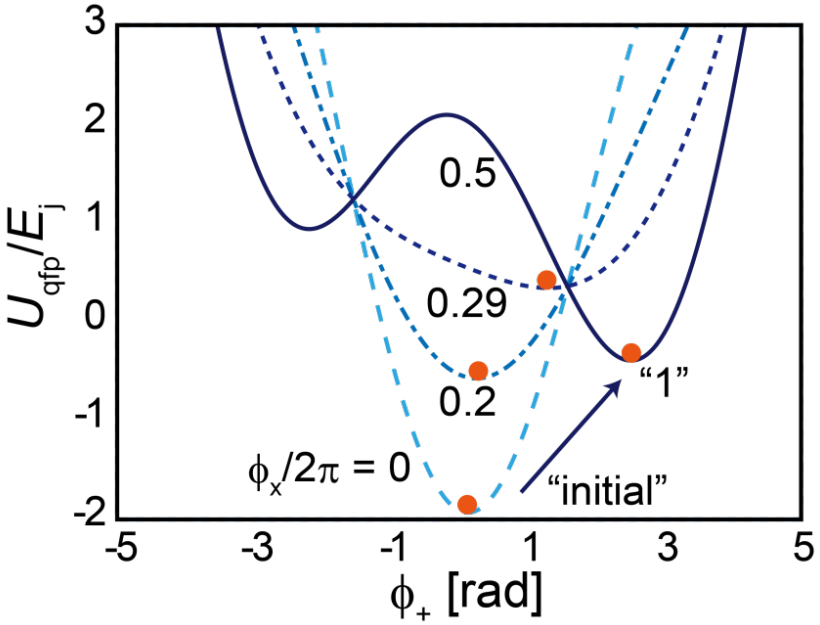
[1] M. Hosoya et al., IEEE Trans. Appl. Supercond. 1, 77–89 (1991).

Adiabatic quantum-flux-parametron (AQFP)

AQFP (buffer) schematic



Potential energy of the AQFP



$+I_{in} \rightarrow$ SFQ stored in left loop, logic '1'.
$-I_{in} \rightarrow$ SFQ stored in right loop, logic '0'.

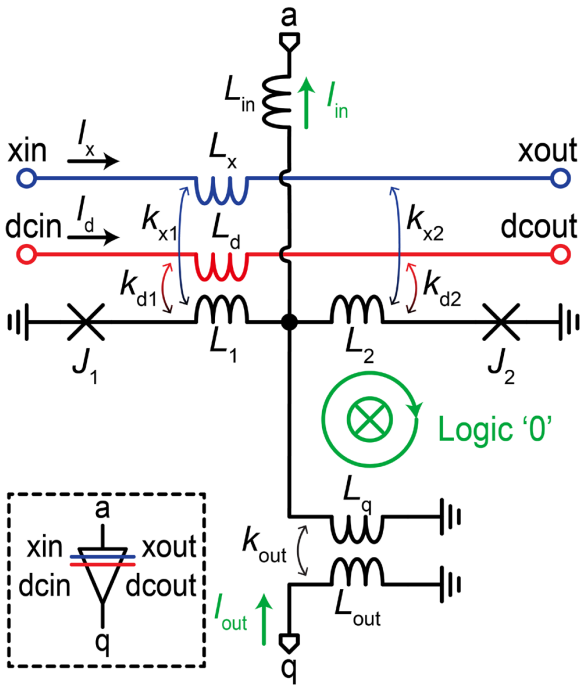
Potential energy changes adiabatically during a switching event.

Operation is based on conventional QFP gates [1].
Switching energy can be reduced below $I_c\Phi_0$
by using AC excitation currents, I_x.

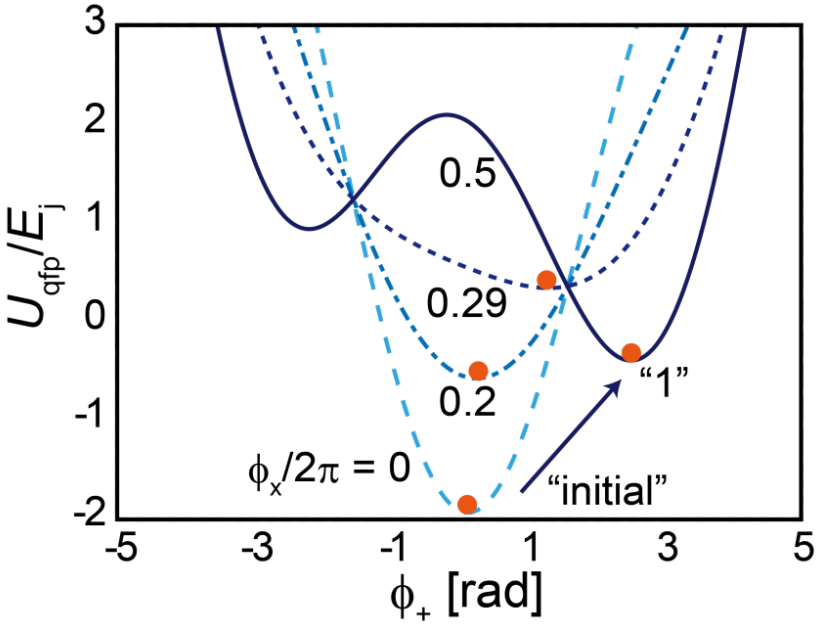
[1] M. Hosoya et al., IEEE Trans. Appl. Supercond. 1, 77–89 (1991).

Adiabatic quantum-flux-parametron (AQFP)

AQFP (buffer) schematic



Potential energy of the AQFP



$+I_{in} \rightarrow$ SFQ stored in left loop, logic '1'.
$-I_{in} \rightarrow$ SFQ stored in right loop, logic '0'.

Potential energy changes adiabatically during a switching event.

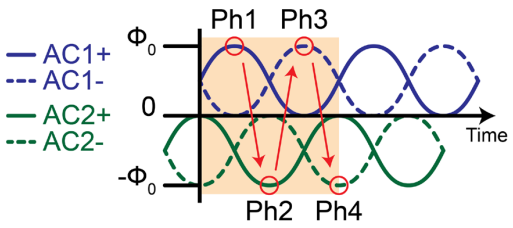
Operation is based on conventional QFP gates [1].
Switching energy can be reduced below $I_c\Phi_0$
by using AC excitation currents, I_x.

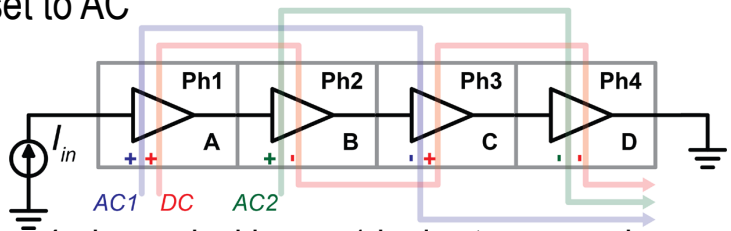
[1] M. Hosoya et al., IEEE Trans. Appl. Supercond. 1, 77–89 (1991).

Data propagation in AQFP logic

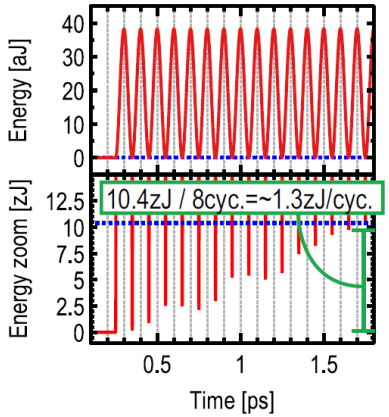
90° phase shift btw **AC1** & **AC2**

DC provides +/- offset to AC

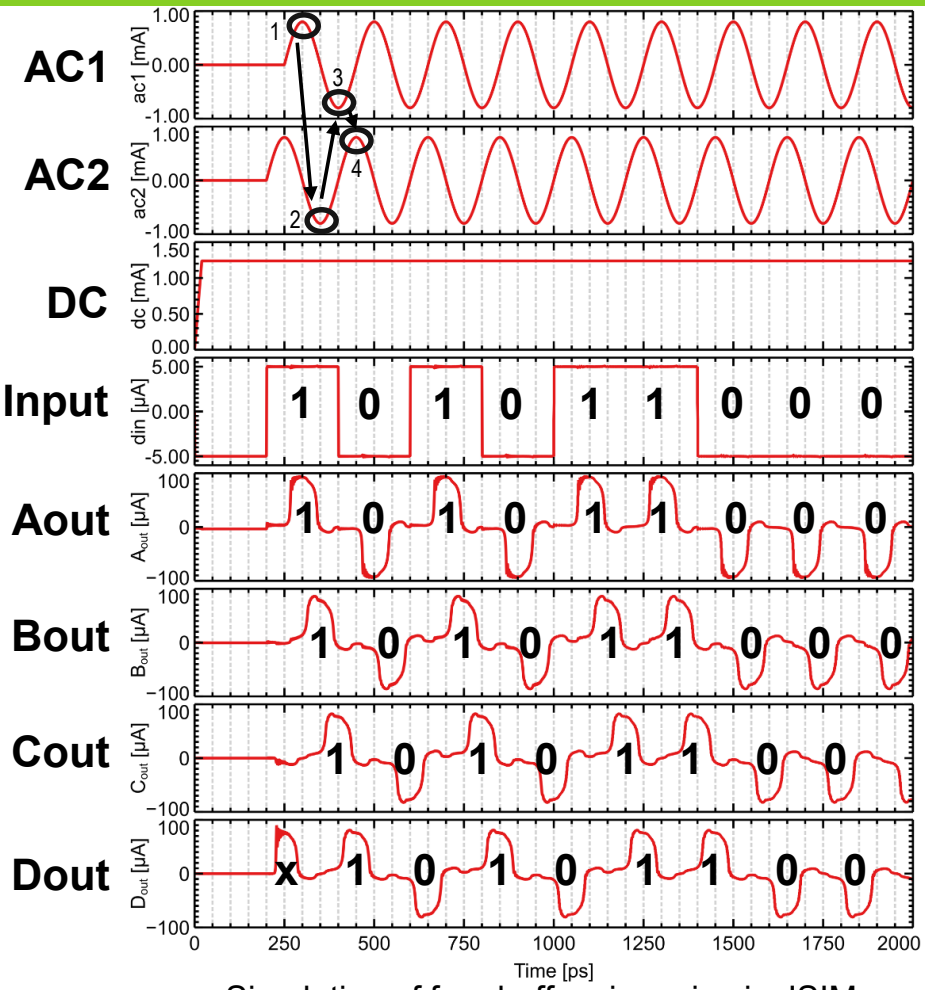




4-phase clocking → 1 logic stage per phase



Adiabatic switching in JSIM. Measured to be 1.4zJ/cyc. at 5 GHz [1].

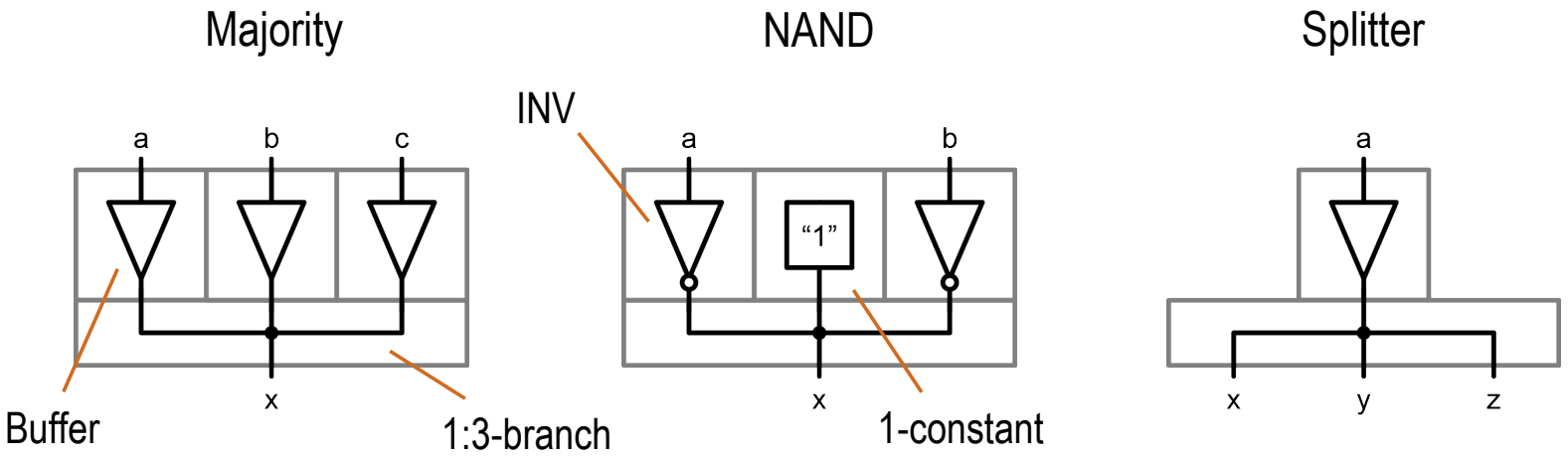


Simulation of four buffers in series in JSIM.

http://www0.sun.ac.za/ix/?q=tools_jsim

[1] N. Takeuchi et al., *Appl. Phys. Lett.*, vol. 114, no. 4, p. 042602, Jan. 2019.

Cell library: minimalist design



$$x = \mathrm{MAJ}(a,b,c) = a\cdot b + b\cdot c + c\cdot a$$

$$x = \mathrm{MAJ}(\overline{a},1,\overline{b}) = \overline{a} + \overline{b} = \overline{ab}$$

$$x = y = z = a$$

Any combinational logic gates can be designed by arraying the four building blocks.

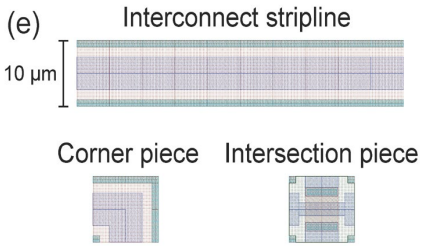
N. Takeuchi et al., *J. Appl. Phys.*, vol. 117, no. 17, p. 173912, May 2015.

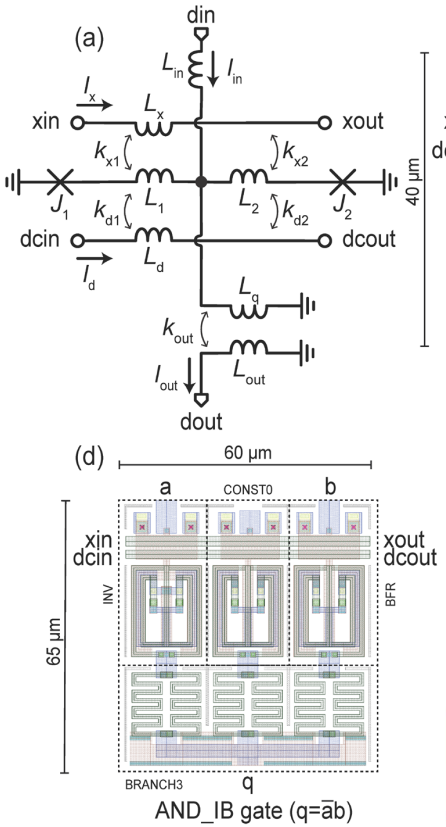
Cell library: minimalist design

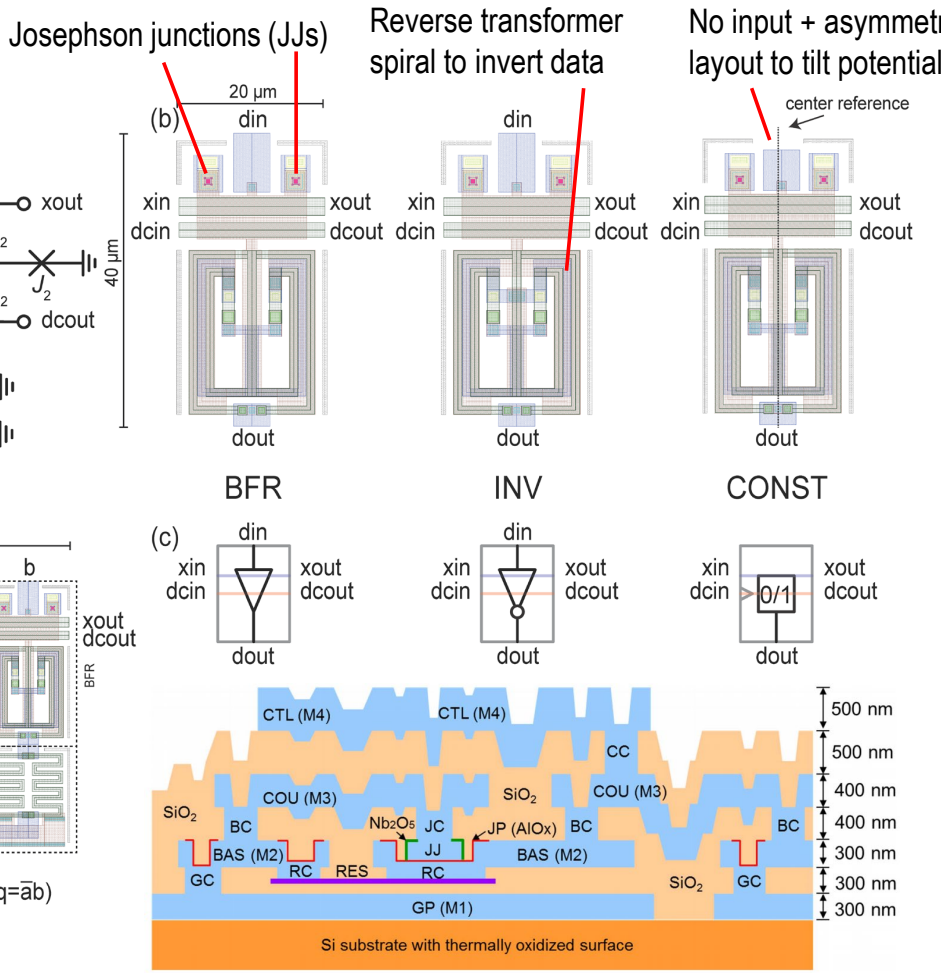
L_{in} = 1.13 pH
L_x = 5.67 pH
L_d = 6.16 pH
L_1, L_2 = 1.53 pH
L_q = 7.88 pH
L_{out} = 31.9 pH
k_{d1},k_{d2} = -0.154
k_{x1},k_{x2} = -0.209
kout = -0.515
J_1, J_2 = 50 μA

Excitation/clock lines are 50Ω microstriplines

Interconnect are shielded striplines



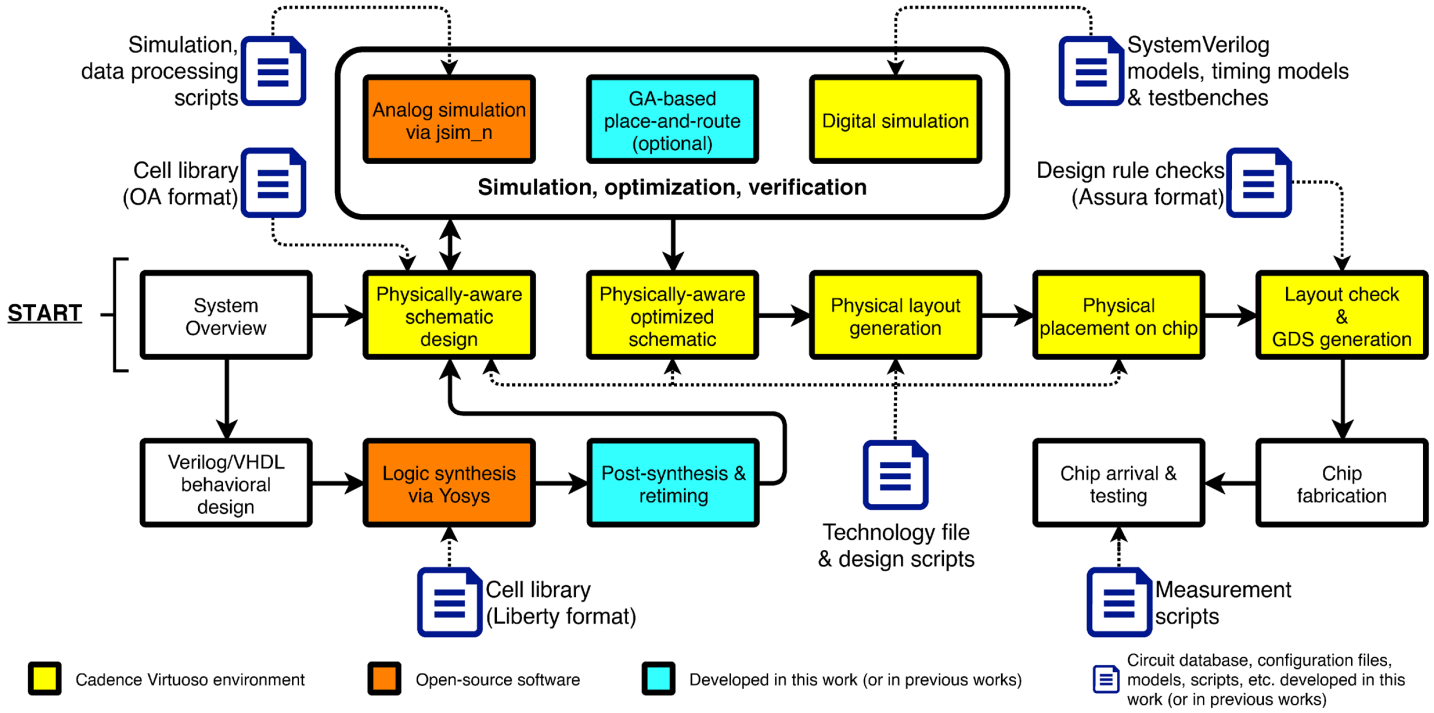




4-layer Nb/AlO$_x$/Nb 10 kA/cm^2 high-speed standard process (HSTP) by AIST, Tsukuba, Japan

N. Takeuchi *et al.*, *Supercond. Sci. Technol.*, vol. 30, no. 3, p. 035002, Mar. 2017.
C. L. Ayala *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 5, p. 054006, Mar. 2020.

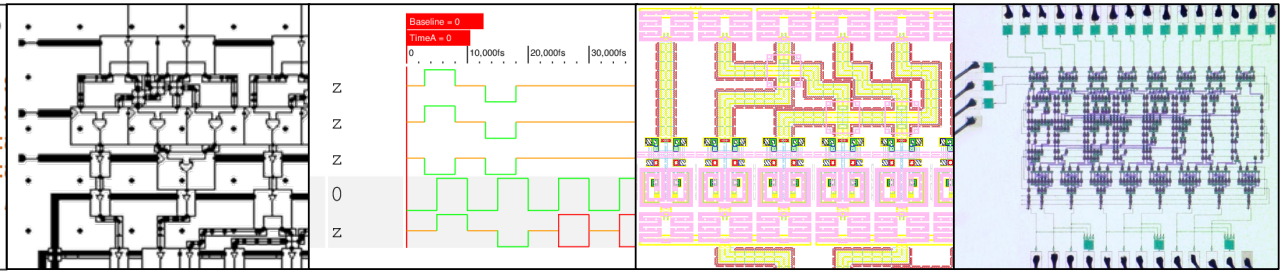
Overall AQFP design flow



C. L. Ayala *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 5, p. 054006, Mar. 2020.

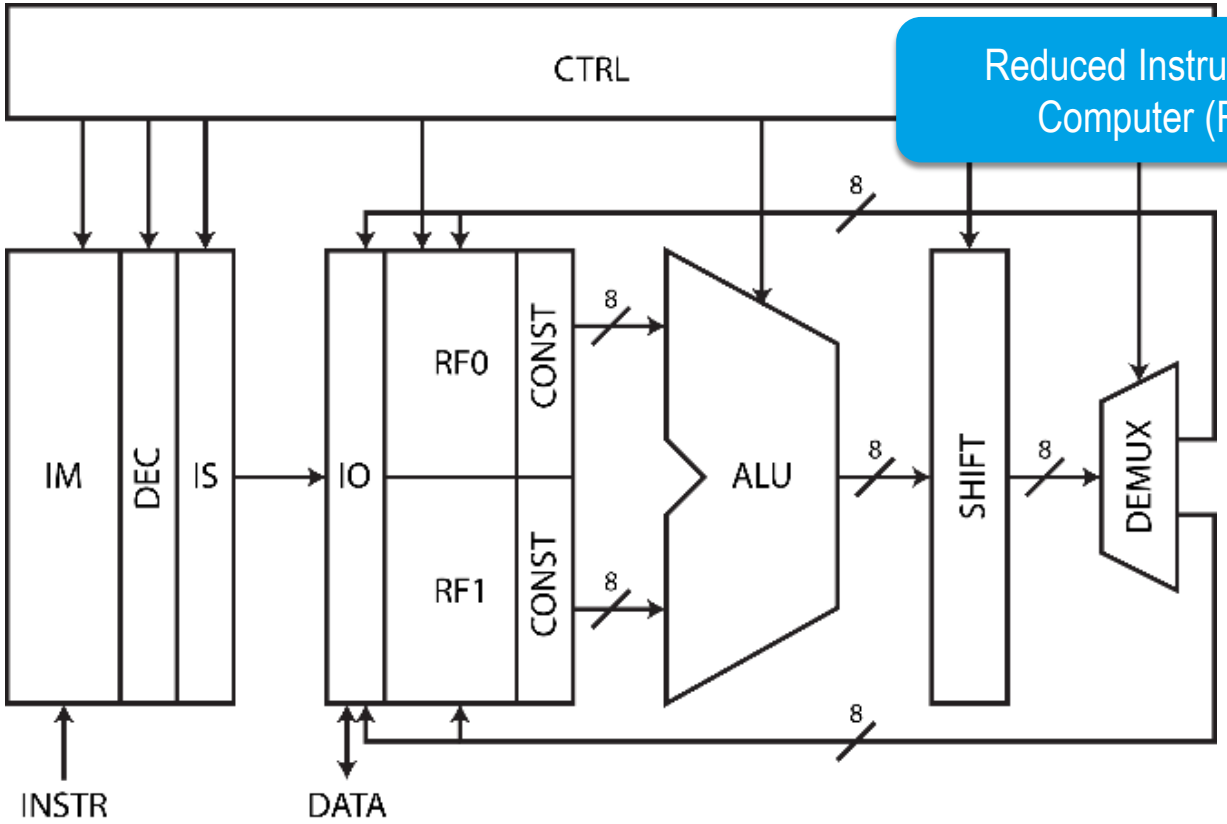
Verilog/VHDL | Schematic | Digital Sim. | Layout | Chip

```
always @(data_in, sh_ctrl, sh_amt)
  case(sh_ctrl)
    2'b00 : data_out = data_in <<
    2'b01 : data_out = data_in >>
    2'b10 : data_out = $signed(dat
    2'b11 : data_out = $signed(dat
    default : data_out = data_in;
  endcase
end
```



Perspective from ASC 2016

12



8-bit 5 GHz Microprocessor General purpose

Branching, logic, add/sub/shift ~10 instructions

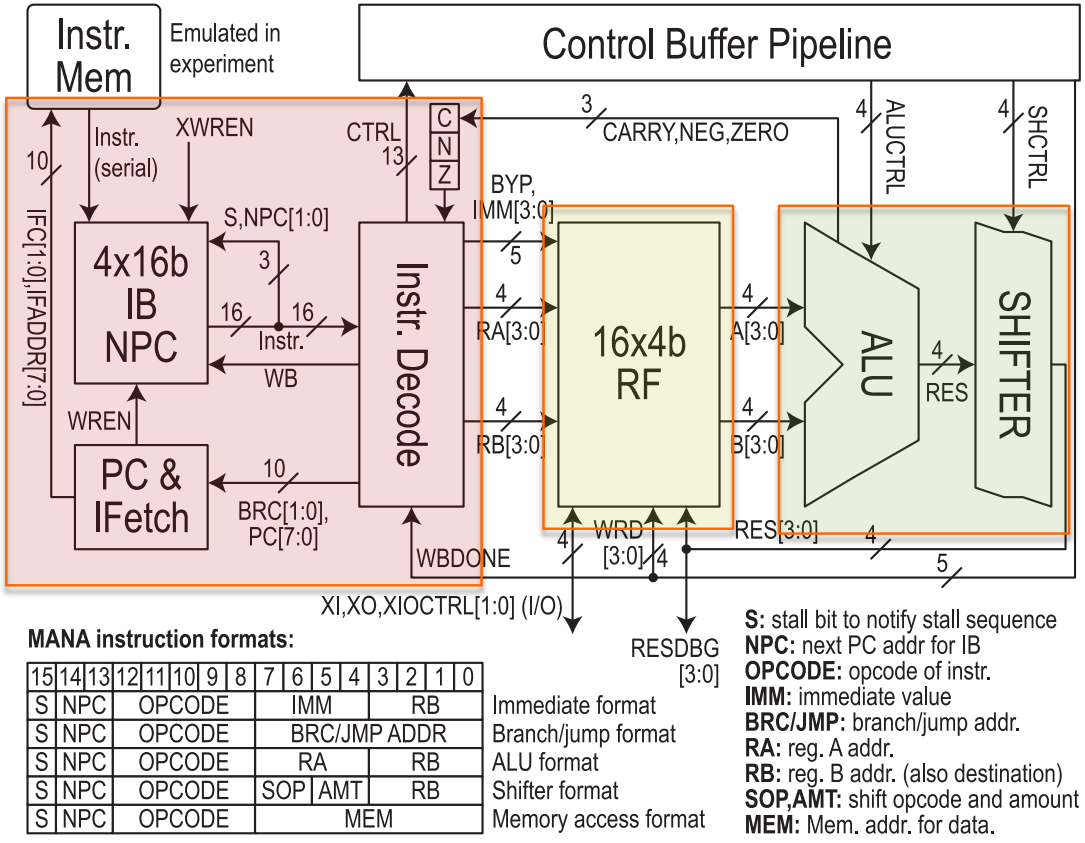
Advanced version: VLIW, SIMD

Majority logic optimization

7mm x 7mm 21k Josephson junctions

MANA microarchitecture

13



MANA instruction formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
S	NPC		OPCODE					IMM						RB		Immediate format
S	NPC		OPCODE					BRC/JMP ADDR								Branch/jump format
S	NPC		OPCODE					RA						RB		ALU format
S	NPC		OPCODE					SOP		AMT				RB		Shifter format
S	NPC		OPCODE					MEM								Memory access format

S: stall bit to notify stall sequence
NPC: next PC addr for IB
OPCODE: opcode of instr.
IMM: immediate value
BRC/JMP: branch/jump addr.
RA: reg. A addr.
RB: reg. B addr. (also destination)
SOP,AMT: shift opcode and amount
MEM: Mem. addr. for data.

MANA – Monolithic Adiabatic iNtegration Architecture

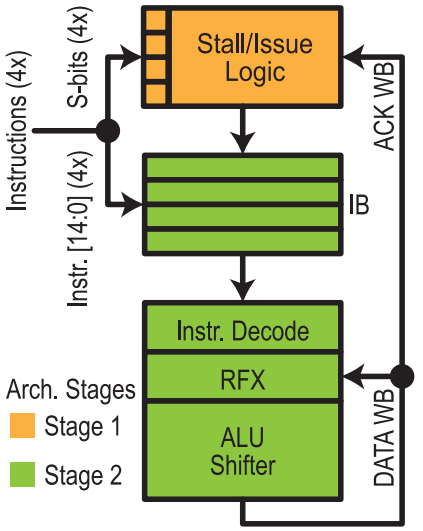
- **Goal:** Demonstrate AQFP can do both logic and memory
- RISC-like datapath + dataflow-like control
- In-order, single-issue
- 4-bit data word size
- 16-bit instr. word
- Program branching
- 21,460 JJs in 1 x 1 cm^2 chip
- 15 fJ/op at RT @ 5 GHz
- 4-phase 5 GHz clock
- Latency: 108 clock phases or 27 cycles (5.4 ns @ 5 GHz)

Instruction Buffer, Decode, and Issue (IDI)	Register File with external I/O (RFX)	ALU-Shifter (EX)	Ctrl buffer, routing, write-back (WB)
5,596 JJs	**8,142 JJs**	**2,238 JJs**	**5,484 JJs**
8 cycles (32 phases)	**8 cycles (32 phases)**	**9 cycles (36 phases)**	**17 cycles (68 phases) overlapped 2 cycles (8 phases) write-back**

MANA instruction set architecture

14

Instruction Word																Description
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	S=Stall bit, NPC= OPCODE=operation code,
S	NPC		OPCODE					RA				RB				RA = address for operand A, RB = address for operand B
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NOP, no operation, used for stalling
0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	HALT, end program
1	0	0	0	0	0	0	1	JMP ADDR								JMP, absolute jump to [JMP ADDR]
1	IBI	NPC	0	0	0	1	0	JMP ADDR								BNEG, branch to [JMP ADDR] if NEG flag is set
1	IBI	NPC	1	0	0	1	0	JMP ADDR								BNNEG, branch to [JMP ADDR] if NEG flag is NOT set
1	IBI	NPC	0	0	0	1	1	JMP ADDR								BEQ, branch to [JMP ADDR] if EQ flag is set
1	IBI	NPC	1	0	0	1	1	JMP ADDR								BNEQ, branch to [JMP ADDR] if EQ flag is NOT set
S	IBI	NPC	0	0	1	0	0	IMM				RB				ANDI, bitwise AND with immediate: R[RB]=R[RB]&&IMM
S	IBI	NPC	0	0	1	0	1	IMM				RB				LI, load immediate: R[RB]=[IMM]
S	IBI	NPC	0	0	1	1	0	0	0	AMT		RB				SRL, shift right logical: R[RB]=R[RB]>>[AMT]
S	IBI	NPC	0	0	1	1	0	0	1	AMT		RB				SRA, shift right arithmetic: R[RB]=R[RB]>>>[AMT]
S	IBI	NPC	0	0	1	1	1	0	0	AMT		RB				SLL, shift left logic: R[RB]=R[RB]<<[AMT]
S	IBI	NPC	0	0	1	1	1	0	1	AMT		RB				SLA, shift left arithmetic (same as SLL) : R[RB]=R[RB]<<<[AMT]
S	IBI	NPC	0	1	0	0	0	RA				RB				ADD, addition: R[RB]=R[RA]+R[RB]
S	IBI	NPC	1	1	0	0	0	RA				RB				ADDNW, add with no write: R[0]=R[RA]+R[RB]
S	IBI	NPC	0	1	0	0	1	RA				RB				SUB, subtract: R[RB]=R[RA]+(~R[RB]+1)
S	IBI	NPC	1	1	0	0	1	RA				RB				SUBNW, subtract with no write: R[0]=R[RA]+(~R[RB]+1)
S	IBI	NPC	0	1	0	1	0	RA				RB				XOR, bitwise XOR R: [RB]=R[RA]⊕R[RB]
S	IBI	NPC	0	1	0	1	1	RA				RB				XNOR, bitwise XNOR: R[RB]=~(R[RA]⊕R[RB])
S	IBI	NPC	0	1	1	0	0	RA				RB				AND, bitwise AND: R[RB]=R[RA]&&R[RB]
S	IBI	NPC	1	1	1	0	0	RA				RB				ANDNB, bitwise AND not B: R[RB]=R[RA]&&~R[RB]
S	IBI	NPC	0	1	1	0	1	RA				RB				OR, bitwise OR: R[RB]=R[RA]||R[RB]
S	IBI	NPC	1	1	1	0	1	RA				RB				ORNB, bitwise OR not B: R[RB]=R[RA]||~R[RB]
S	IBI	NPC	0	1	1	1	0	MADDR								LFM, load from memory: R[14,R15]=MEM[MADDR][Hi,Lo]
S	IBI	NPC	0	1	1	1	1	MADDR								WTM, write to memory: MEM[MADDR]=R[R14]:R[R15]



Architecturally 2-stage pipeline

- **Stage 1:** determine stall based on prefetched stall bits (1 cycle latency)
- **Stage 2:** fetch instruction from IB, decode, execute, write back (107 cycles total)
- Allows peak IPC of 1

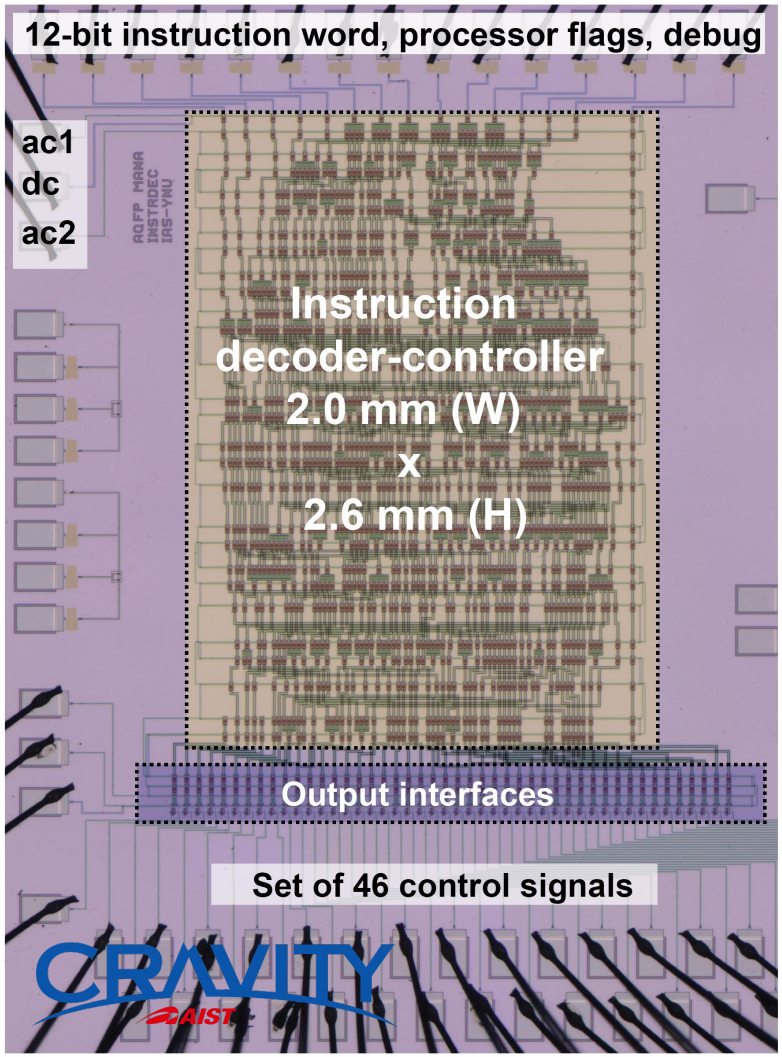
	Instruction	S	NPC		Opcode					RA				RB			
Instr. 1	add $4, **$3**	1	0	1	0	1	0	0	0	0	1	0	0	0	0	1	1
Instr. 2	add **$3**, $6	0	1	0	0	1	0	0	0	0	0	1	1	0	1	1	0
Instr. 3	xor $5, $7	0	1	1	0	1	0	1	0	0	1	0	1	0	1	1	1

Instr. 2 depends on Instr. 1's **$3**. Compiler sets S-field of Instr. 1 to '1' thus Instr. 2 must wait.

S-field – stall-bit: compile-time hazard detection + hardware stall

- Stall-bit tells next instruction to wait
- Propagates with its instruction
- Returns with processed data as ACK signal to notify next instruction can be issued

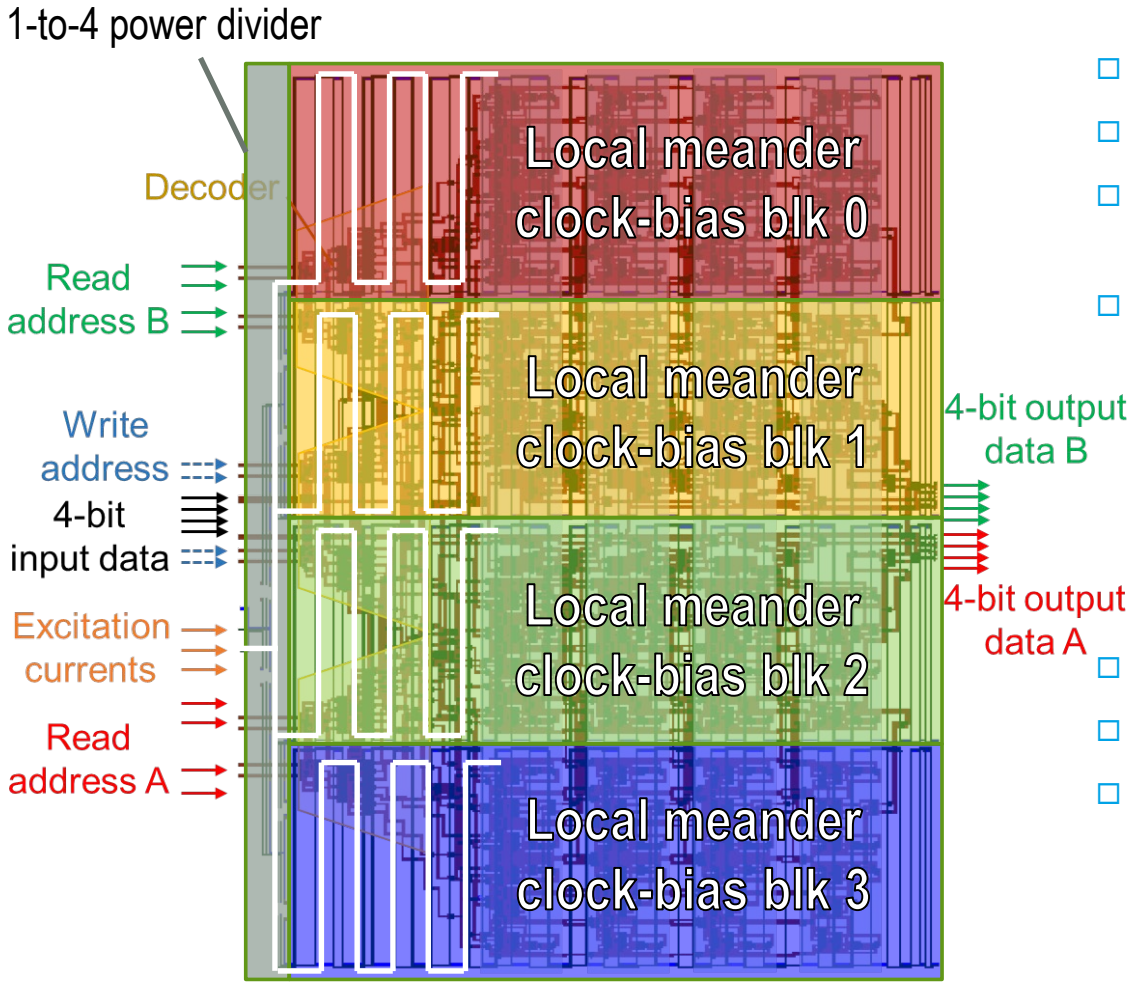
Breakout: MANA instruction decoder-controller



- Input:
  - 12-bit instruction word
  - Processor flags (ZERO, NEG)
  - Debug input
- Generates 46 control signals + debug
- Logic synthesis and GA-based place-and-route
- Updates for MANA integration
  - 16-bit instruction word
  - Addition of CARRY flag
  - NPC (next PC) changed to request next block of 4 instructions
    - Was used to avoid long PC calculation every cycle
    - Now IB is stall logic controlled parallel shift register
    - All jumps/branches will force a stall
- 2.0 mm x 2.6 mm
- 2664 JJs
- Latency:
  - 7 cycles for datapath signals (1400 ps @ 5 GHz)
  - 1 cycle for stall logic (200 ps @ 5 GHz)

C. L. Ayala et al., *ISEC* (2019), Riverside, CA, USA.

Breakout: MANA register file (16 x 4-bit)

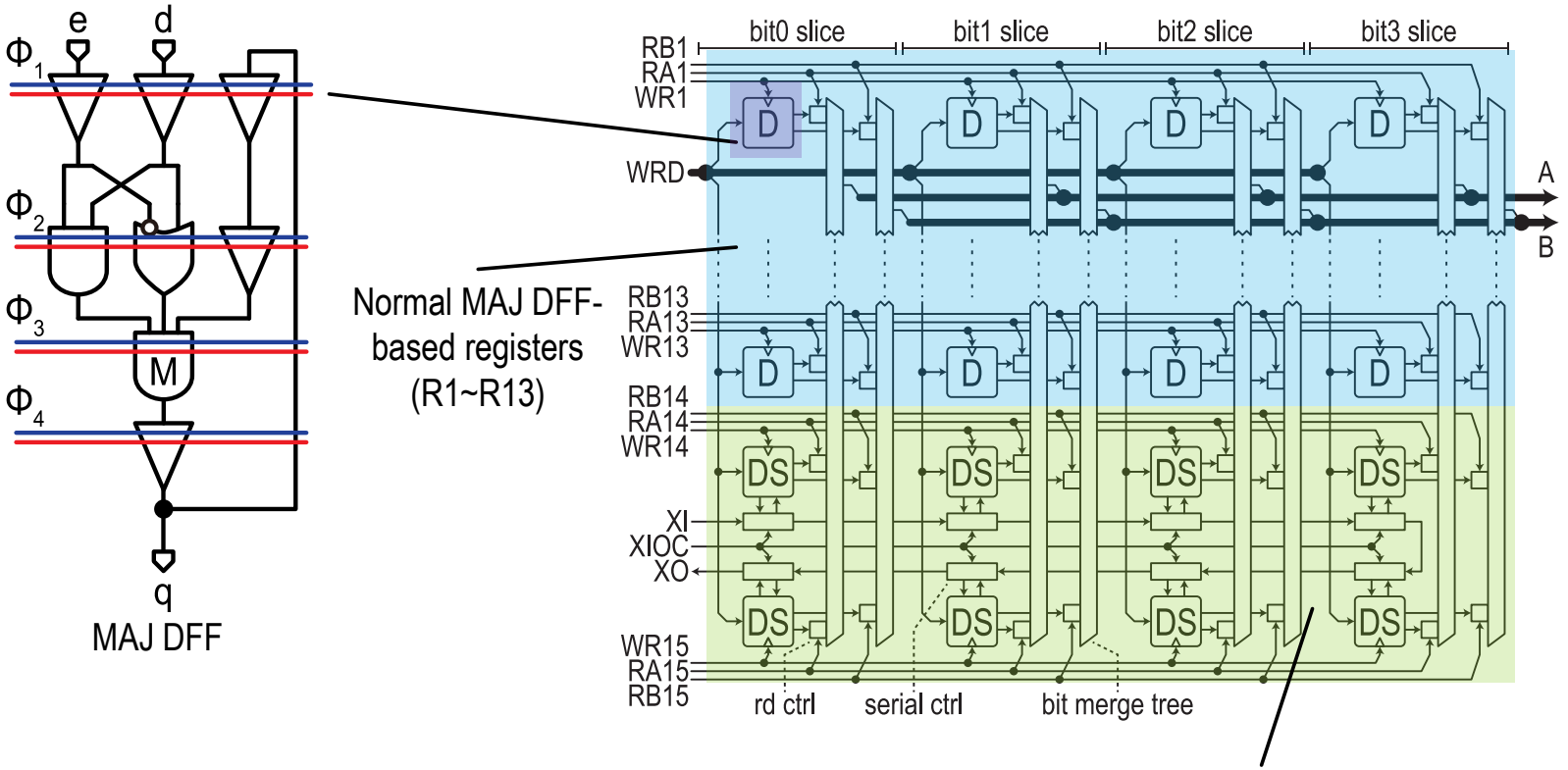


- 16-word x 4-bit
- 2-read, 1-write ports
- Memory: gate-level loop with enable
- Circuit divided into 4 clocked blocks
  - Microstrip velocity 161μm/ps
  - Roundtrip meandering clock length < 5 mm sufficient to avoid timing errors [1]
- 4.7 mm x 6.6 mm
- ~6000 JJs
- Latency: 7.25 cycles (1450 ps @ 5 GHz)

M. Nozoe et al., ASC 2018, Seattle, USA.

[1] C. L. Ayala *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 5, p. 054006, Mar. 2020.

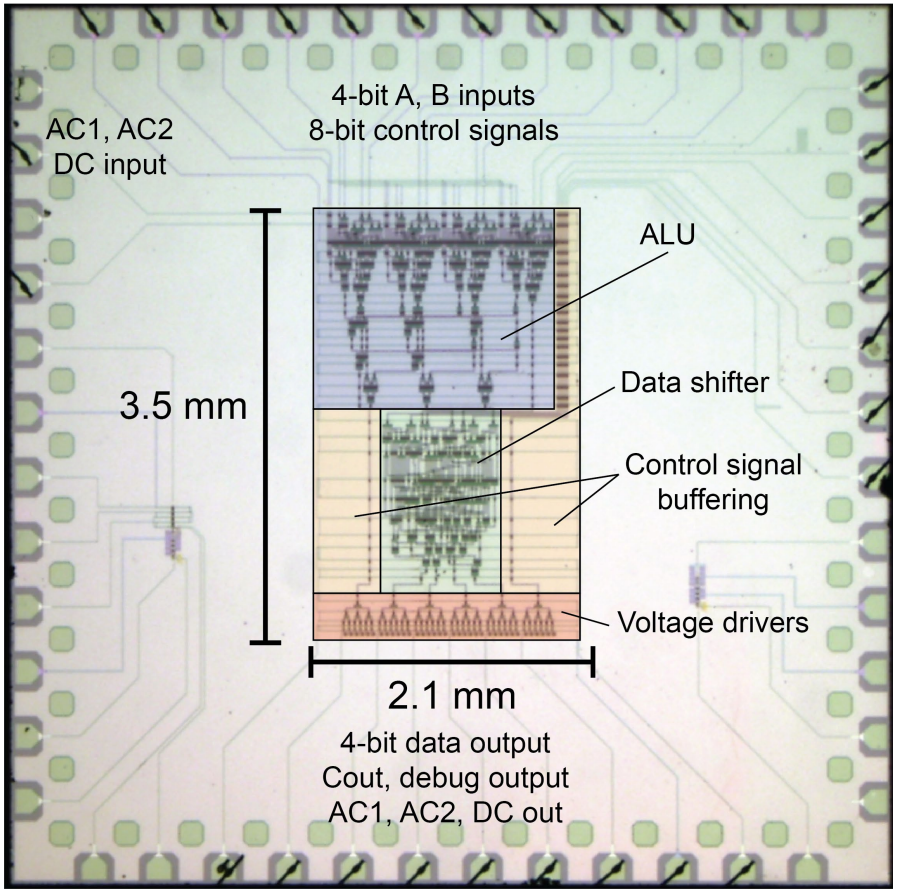
Breakout: MANA register file (16 x 4-bit)



Updates for MANA integration

- R0 remains zero-constant
- R1 → normal register, no longer ones-constant
- R14, R15 modified to interface with serial I/O

Breakout: MANA EX high-speed chip



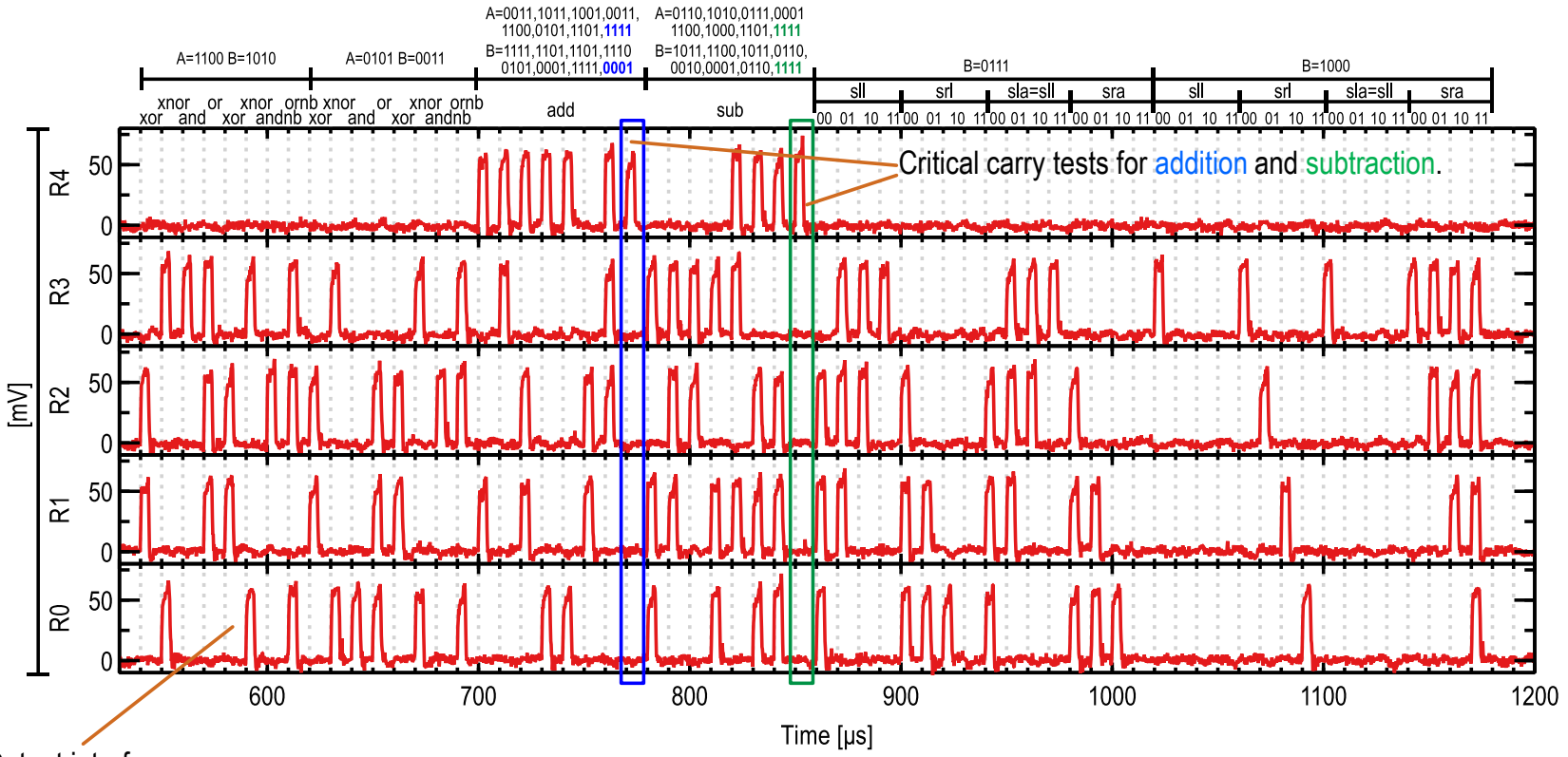
- MANA EX high-speed chip
  - Nb/AlO_x/Nb 10 kA/cm^2 technology
  - ALU-shifter datapath + control signal buffering
  - **ALU:** MAJ-based Kogge-Stone adder [1] with in-place logic operators
  - **Shifter:** Synthesized logic-arithmetic data shifter [2]
  - 7 mm x 7 mm chip
  - 2.1 mm x 3.5 mm core
  - 2076 JJs
  - Latency: 9 cycles (1800 ps @ 5 GHz)
- High-speed considerations
  - Roundtrip of meandering clock < 5 mm
  - High-speed voltage drivers [3]
  - High-speed He-immersion chip probe
    - AC clock sources
    - BERT: Single bit data generator, single bit output checker

[1] C. L. Ayala et al., IEEE Trans. Appl. Supercond., vol. 27, no. 4, pp. 1–7, Jun. 2017.
[2] C. L. Ayala et al., ISS 2017, Tokyo, Japan.
[3] N. Takeuchi et al., *Appl. Phys. Lett.*, vol. 110, no. 20, p. 202601, May 2017.

CRAVITY AIST

Breakout: MANA EX high-speed chip

19

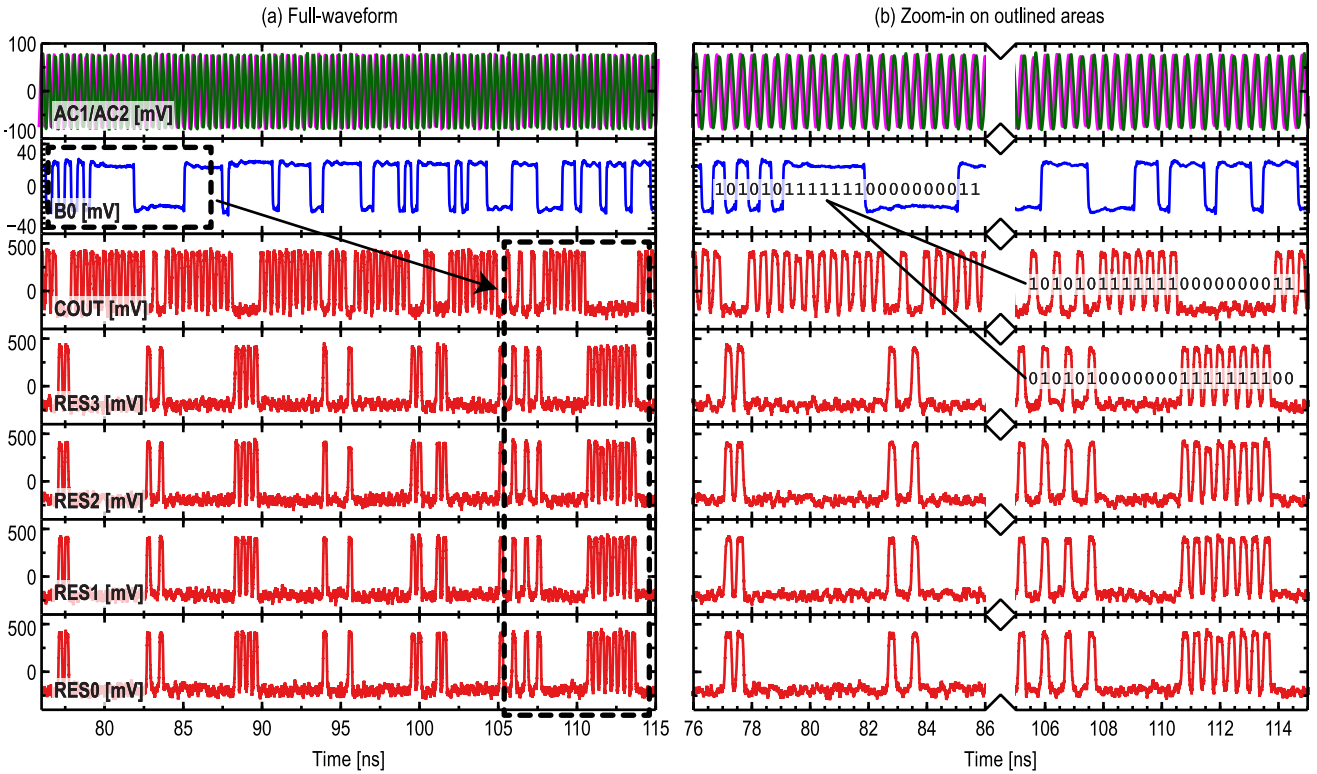


Output interface uses unipolar return-to-zero encoding.

Functionally exhaustive low-speed test (100 kHz)

- Tested logical operators, addition/subtraction (random and carry propagate), and shifter operations.
- All tests passed.

Breakout: MANA EX high-speed chip



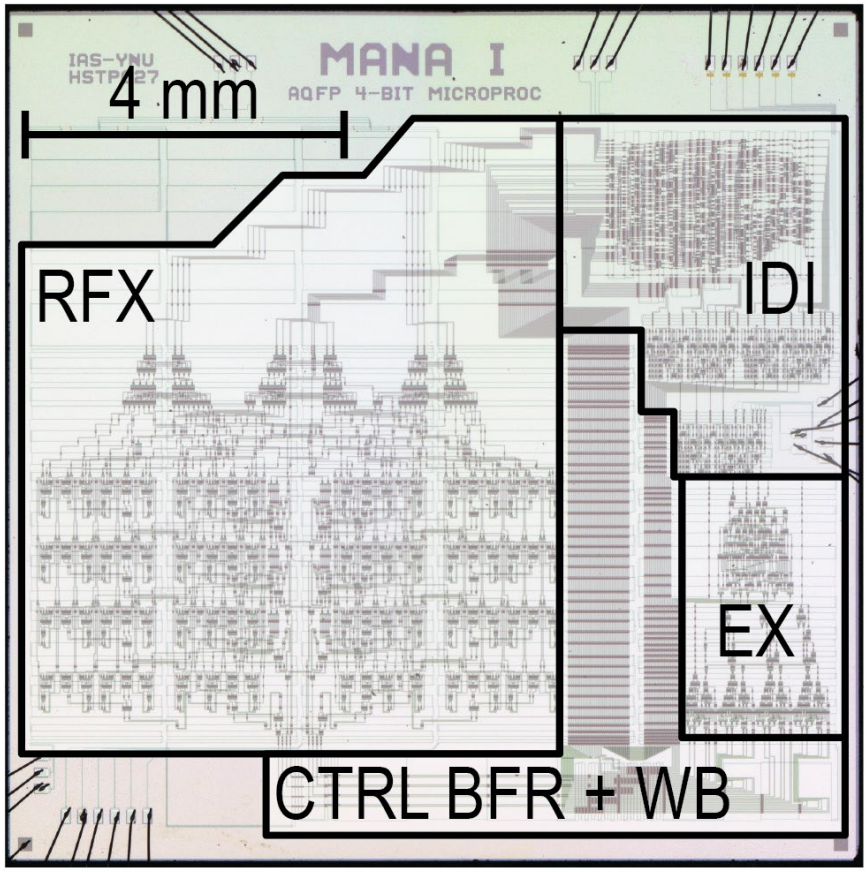
Critical carry-propagate high-speed test pattern (1111 + 0001)

- B[0] high-speed pseudo-random input
- B[3:1] fixed to '0'
- A[3:0] fixed to '1'

High-speed 2.5 GHz (T=400 ps) test

- Expected outputs: COUT←B[0]; RES[3:0]←!B[0]
- 1 GHz ~ 2.5 GHz operated successfully
- 3 GHz operation unstable
  - Fall-time of output too slow, may need to improve output interface or experimental setup

MANA prototype chip

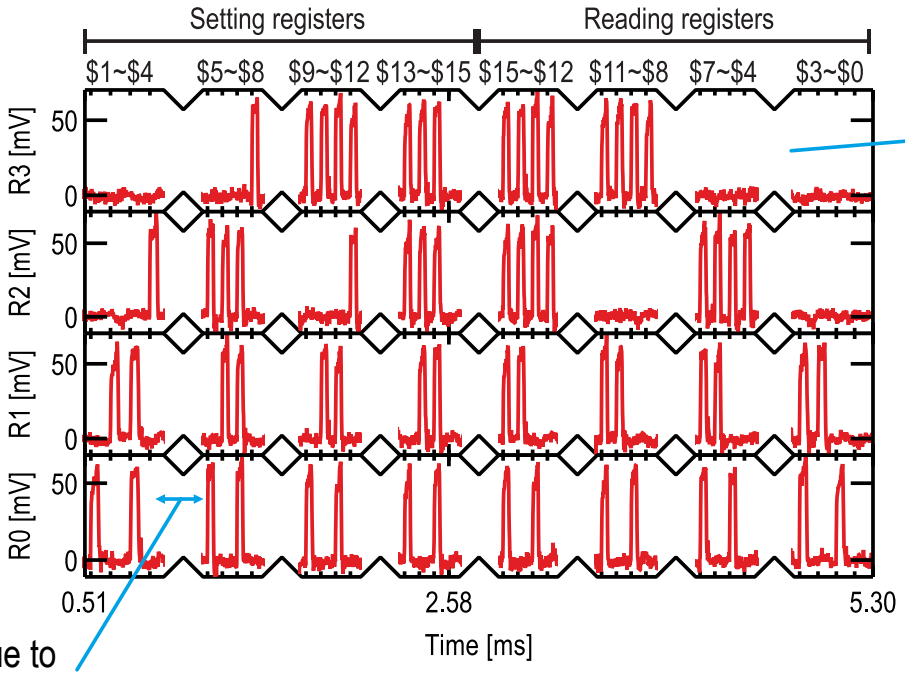


- MANA prototype chip
  - Nb/AlO$_x$/Nb 10 kA/cm^2 technology
  - All stages integrated together by hand
  - 1 cm x 1 cm
  - Unoptimized clock network
  - Wire-bonded
  - 21,460 JJs
  - Latency: 27 cycles (5.4 ns @ 5 GHz)
- Experiment
  - Low-speed testing
  - 4x16-bit instruction blocks manually loaded to IB of IDI serially
  - 4-bit debug output tapped from WB data

MANA prototype chip

Smoke test: set and read registers

(1) Clear all registers via $0
(2) Set registers $1=0x1, $2=0x2, $3=0x3…
(3) Read registers from $15 down to $0



Demonstration of peak IPC=1

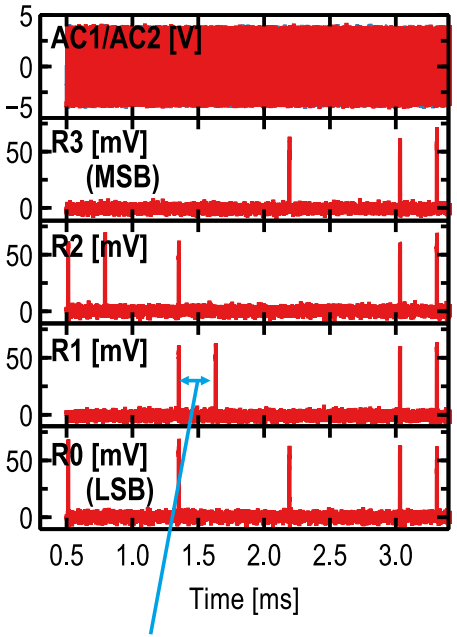
64-cycle stall due to serial loading of 4x16b instructions

Smoke test passes at 100 kHz.

MANA prototype chip

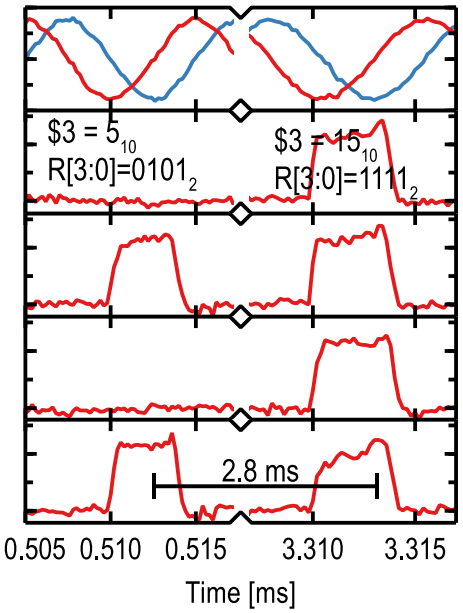
Test program 1: add/sub + branch

(a) Full-waveform [0.5 ms to 3.4 ms]



27-cycle stall due to data/ctrl hazards

(b) Zoom-in of first and last result



(c) Test program 01

```
//Zero all reg with $0
//Set $1=0x1, $2=0x2, $3=0x3, $4=0x4…

//Main program loop
00: add $3, $2      //add 2 to $3
01: subnw $9, $3    //compare to 9 in $9
10: bneq 0x00       //if !zero, go to 0x00
11: add $3, $6      //add 6

//Check program
00: add $3, $0      //Check $3, expect 15
```

(d) Output sequence

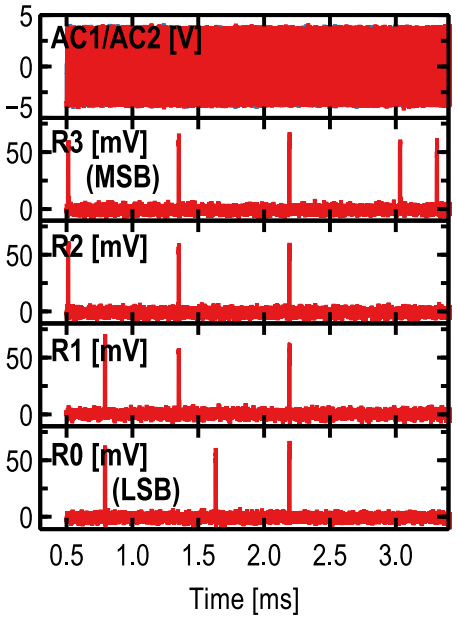
```
RES1: 0b0101  //1st add: $3 = $3+$2 = 5
RES2: 0b0100  //1st cmp: $9-$3 = 4
RES3: 0b0111  //2nd add: $3 = $3+$2 = 7
RES4: 0b0010  //2nd cmp: $9-$3 = 2
RES5: 0b1001  //3rd add: $3 = $3+$2 = 9
RES6: 0b0000  //3rd cmp: $9-$3 = 0
RES7: 0b1111  //Add 6: $3 = $3+$6 = 15
RES8: 0b1111  //Check: $3 = $3+$0 = 15
```

Test program 1 successfully passes.

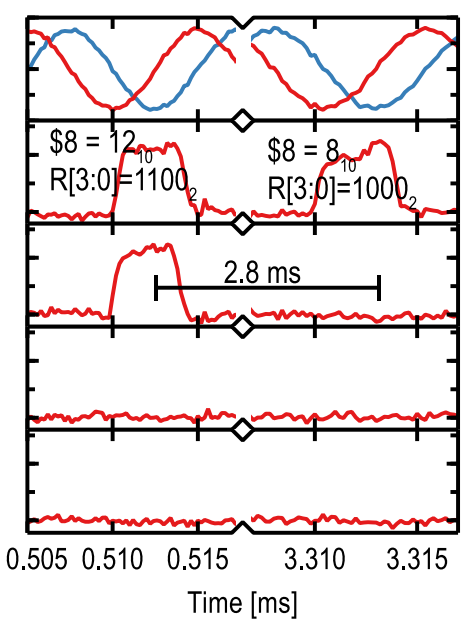
MANA prototype chip

Test program 2: shift/sub + branch

(a) Full-waveform [0.5 ms to 3.4 ms]



(b) Zoom-in of first and last result



(c) Test program 02

```
//Zero all reg with $0
//Set $1=0x1, $2=0x2, $3=0x3, $4=0x4…

//Main program loop
00: sra 01, $8       //arith. sh by 1 on $8
01: subnw $15, $8    //compare to 15 in $15
10: bneq 0x00        //if !zero, go to 0x00
11: sll 03, $8       //sll by 3 on $8

//Check program
00: or $8, $0      //Check $8, expect 8
```

(d) Output sequence

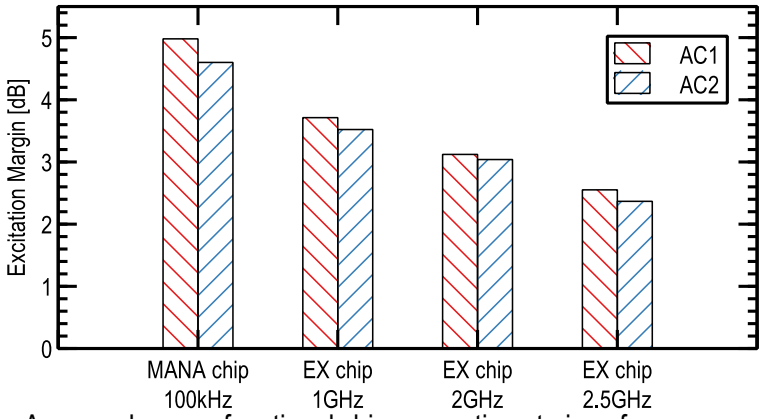
```
RES1: 0b1100  //1st sra: $8 = 1000->1100
RES2: 0b0011  //1st cmp: $15-$8 = 3
RES3: 0b1110  //2nd sra: $8 = 1100->1110
RES4: 0b0001  //2nd cmp: $15-$8 = 1
RES5: 0b1111  //3rd sra: $8 = 1110->1111
RES6: 0b0000  //3rd cmp: $15-$8 = 0
RES7: 0b1000  //sll: $8 = 1111->1000
RES8: 0b1000  //Check: $8 = $8|$0 = 8
```

Test program 2 successfully passes.

RF R/W, ALU execution, branching, and hardware stalling successfully demonstrated.

MANA prototype chip

Excitation margins of chips



Averaged across functional chips operating at given frequency.

Statistics of measured chips

Wafer	Chip 1	Chip 2	Chip 3	I_c[a]	Working
MANA-W1	100 kHz[b]	X	100 kHz	110.3%	5 / 6 chips
MANA-W2	100 kHz	100 kHz	100 kHz	107.5%	
EX-W1	2.3 GHz	2.5 GHz	2.1 GHz	96.0%	7 / 12 chips
EX-W2	2.1 GHz	X	100 kHz	90.8%	
EX-W3	1.5 GHz	U	1.2 GHz	87.8%	
EX-W4	X	U	X	91.1%	

'U' denotes unstable or partial operation.
'X' denotes no meaningful output.
[a] Measured I_c over designed I_c
[b] Note that MANA chips were tested only up to 100 kHz.

Comparison with other demonstrated adiabatic work

	[1]	[2]	[3]	This work	This work
Circuit	16 b CLA	8 b DLX processor	16 b MIPS processor	4 b MANA processor	4 b EX (ALU-shifter)
Status	Tested	Tested	Layout in progress	Tested	Tested
Technology	0.8 µm CMOS	0.18µm NMOS	90nm CMOS	AQFP Nb/AlO$_x$/Nb	AQFP Nb/AlO$_x$/Nb
Clk. Rate	4 MHz (tested)	880 kHz (tested)	0.5 GHz (simulated)	100kHz (tested)	**2.5 GHz (tested)**
Supply	2.5 V dc	1.8 V dc	1 V dc	1 mA ac	1 mA ac
Energy/op	4 pJ	8.5 pJ	3 fJ[a]	**15 fJ[b]**	**1.6 fJ[b]**

[1] J. Lim *et al.*, *IEEE JSSC*, vol. 34, no. 6, pp. 898–903, Jun. 1999.
[2] S. Kim et al., *in Proc. of Comp. Frontiers – CF '05*, 2005.
[3] R. Celis-Cordova *et al.*, in *IEEE ICRC*, Nov. 2019.
[a] Authors simulated 3 b shift register. AQFP equivalent is 4.2 aJ with cooling.
[b] Already includes cooling overhead coefficient of 1000x.

- Wide AC1/AC2 excitation margins
  - 5 dB / 4.6 dB for MANA at 100 kHz
  - 2.6 dB / 2.4 dB for EX chip at 2.5 GHz
- Measured tests repeatable across multiple chips and wafers.
- Superior speed and energy when compared with other demonstrated adiabatic work.
- More work to be done to have a clear competitive edge over bleeding edge FinFET.

Outlook

How do we move forward with AQFP logic?

Comparison of AQFP INV and FinFET INV FO3/FO4

	AQFP	5 nm FinFET	7 nm FinFET
Power Supply	2 x 1 mA AC + 1 mA DC	0.45 V ~ 0.65 V	0.45 V ~ 1 V
Delay (ps)	~10 [3]	?? ~ 8.3	0.667 ~ 40
Switching Energy (fJ)	~0.0014 @ 5 GHz	0.106 ~ 0.291	0.111 ~ 1.317

Includes 1000x cooling overhead for AQFP

Area efficiency

Cell-level

- Advanced process such as MIT LL SFQ5ee [1]
- Directly coupled QFP (DQFP) [2]
- Novel compact memory

Design methodology

- Physical rows with multiple excitation phases available

Latency / clock distribution

- Delay line clocking [3]
- Power divider clocking [4]
- Clock domain crossing synchronizers

Flux trapping

- Moat embedded interconnects [5]

Advanced EDA tools

- Flux trapping analysis [6]
- Flexible chip-level integration tools [7]
- More mature tools [7]

[1] Y. He *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 3, p. 035010, Feb. 2020.
[2] N. Takeuchi *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 6, p. 065002, May 2020.
[3] N. Takeuchi *et al.*, *Appl. Phys. Lett.*, vol. 115, no. 7, p. 072601, Aug. 2019.
[4] Y. He *et al.*, *Appl. Phys. Lett.*, vol. 116, no. 18, p. 182602, May 2020.
[5] C. J. Fourie *et al.*, *IEEE Trans. on Appl. Supercond.*, vol. 30, no. 6, pp. 1–9, Sep. 2020.
[6] K. Jackman *et al.*, *IEEE Trans. on Appl. Supercond.*, vol. 27, no. 4, pp. 1–5, Jun. 2017.
[7] IARPA SuperTools research program

FinFET data sources:
- E. Sicard, *Introducing 7-nm FinFET technology in Microwind*. 2017.
- A. Stillmaker and B. Baas, "Scaling equations for the accurate prediction of CMOS device performance from 180nm to 7nm," *Integration*, vol. 58, pp. 74–81, Jun. 2017.
- N. Collaert, "Device architectures for the 5nm technology node and beyond," presented at the SEMICON Taiwan, 2016.
- S. Sinha et al., "Design benchmarking to 7nm with FinFET predictive technology models," in *Proceedings of the 2012 ACM/IEEE international symposium on Low power electronics and design - ISLPED '12*, Redondo Beach, California, USA, 2012, p. 15.

Summary

- AQFP Logic
  - Superconductor logic using Josephson junctions operating adiabatically
  - Energy dissipation: 1.4 aJ/op at 5GHz (includes cooling)

- MANA processor
  - 4-bit prototype design to show AQFP logic can do both processing and storage
  - Nb/AlO_x/Nb 10 kA/cm^2 superconductor process
  - Key processor operations demonstrated: R/W, ALU execution, stalling, program branching at 100 kHz
  - Standalone EX stage operated up to 2.5 GHz
  - First demonstration of adiabatic computing using superconductor logic

- Promising technology platform for next generation data centers and supercomputers
- Challenges still exist particularly in improving area efficiency and latency at large-scale

Stage-by-stage summary of MANA

Stage	Description	Total JJs	Latency (cycles)	fJ/op[a]
IDI	Instruction buffer, Decode, Issue	5596	8	3.917
RFX	Register File with eXternal I/O interface	8142	8	5.699
EX	EXecution stage (ALU-shifter)	2238	9	1.567
WB	Write Back, ctrl, buffering, routing	5484	2	3.839
	Total:	**21460**	**27**	**15.022**

Includes 1000x cooling overhead

Questions?

Thank You

This work was supported by the Grant-in-Aid for Scientific Research (S) No. 19H05614 and the Grant-in-Aid for Early Career Scientists No. 18K13801 from the Japan Society for the Promotion of Science (JSPS).

This work was also supported by the VLSI Design and Education Center (VDEC) of the University of Tokyo in collaboration with Cadence Design Systems, Inc.

The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) using the high-speed standard process (HSTP).