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Cryogenic electrical interfaces for large-scale spin-qubit quantum processors

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QuTech

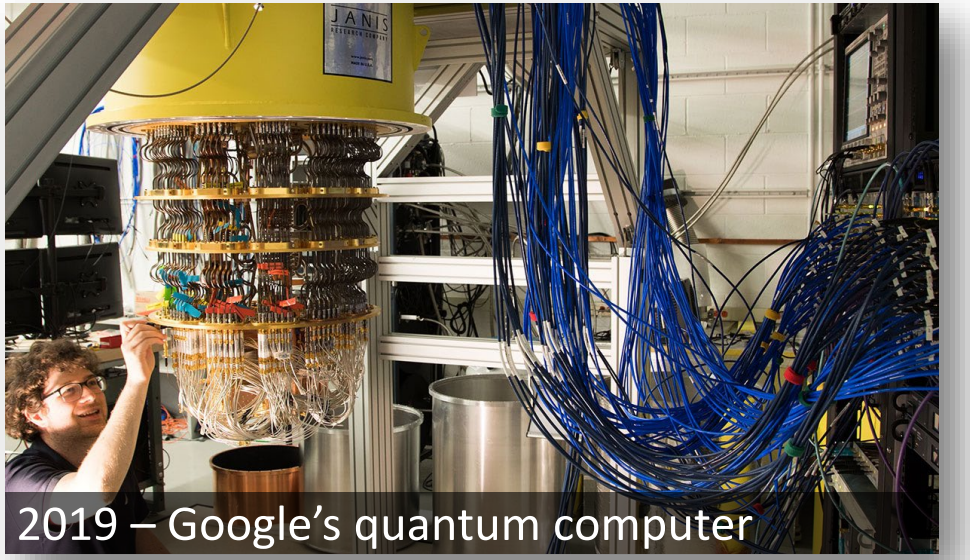
TU Delft

Quantum & Computer Engineering

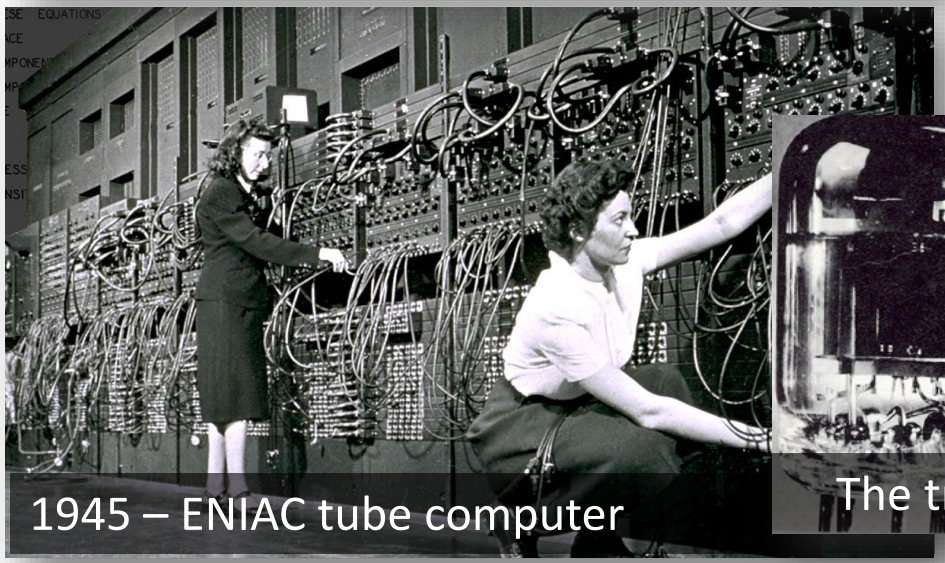
WOLTE 16

Cagliari, June 5th, 2024

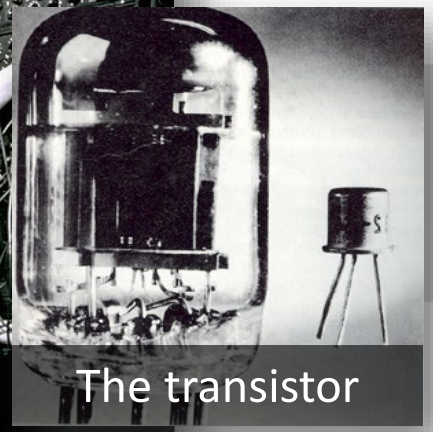
Today's Quantum Computers (and tomorrow?)



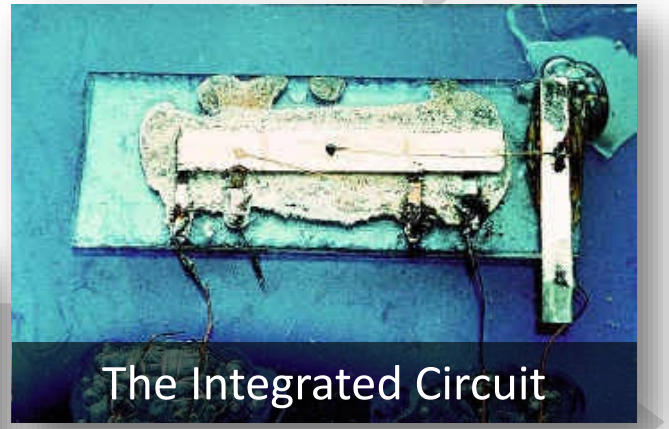
2019 – Google's quantum computer



1945 – ENIAC tube computer



The transistor

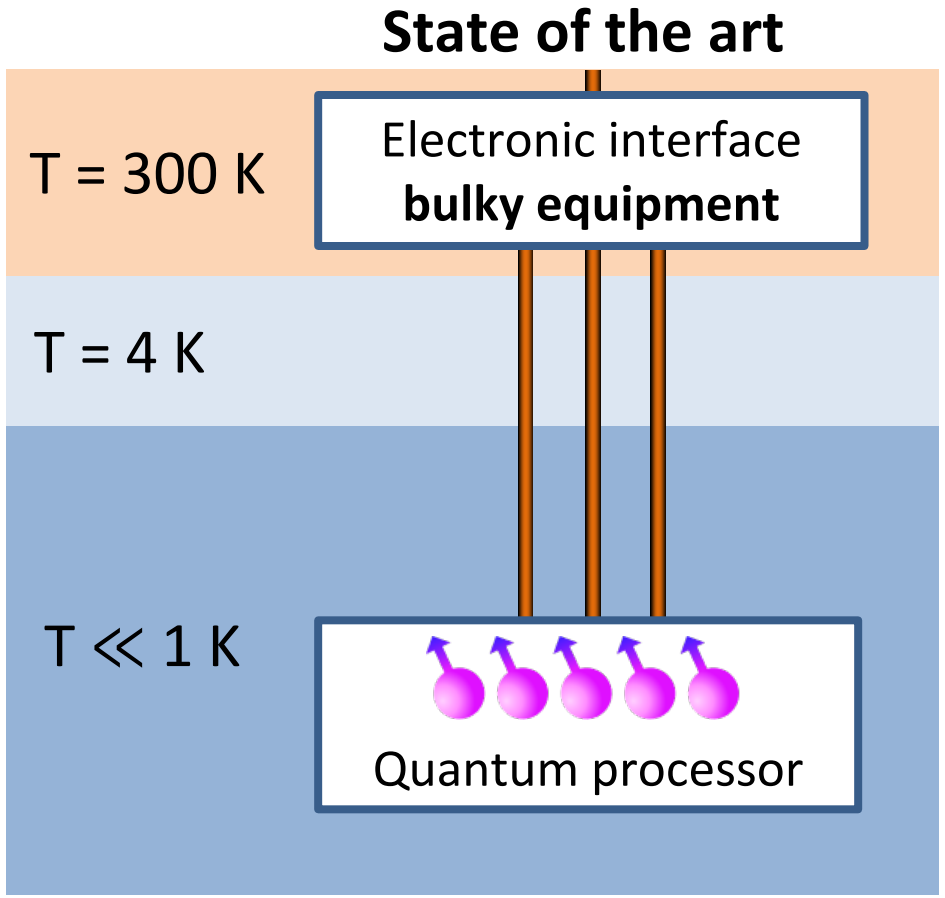


The Integrated Circuit

?

2024 – Silicon-based computers

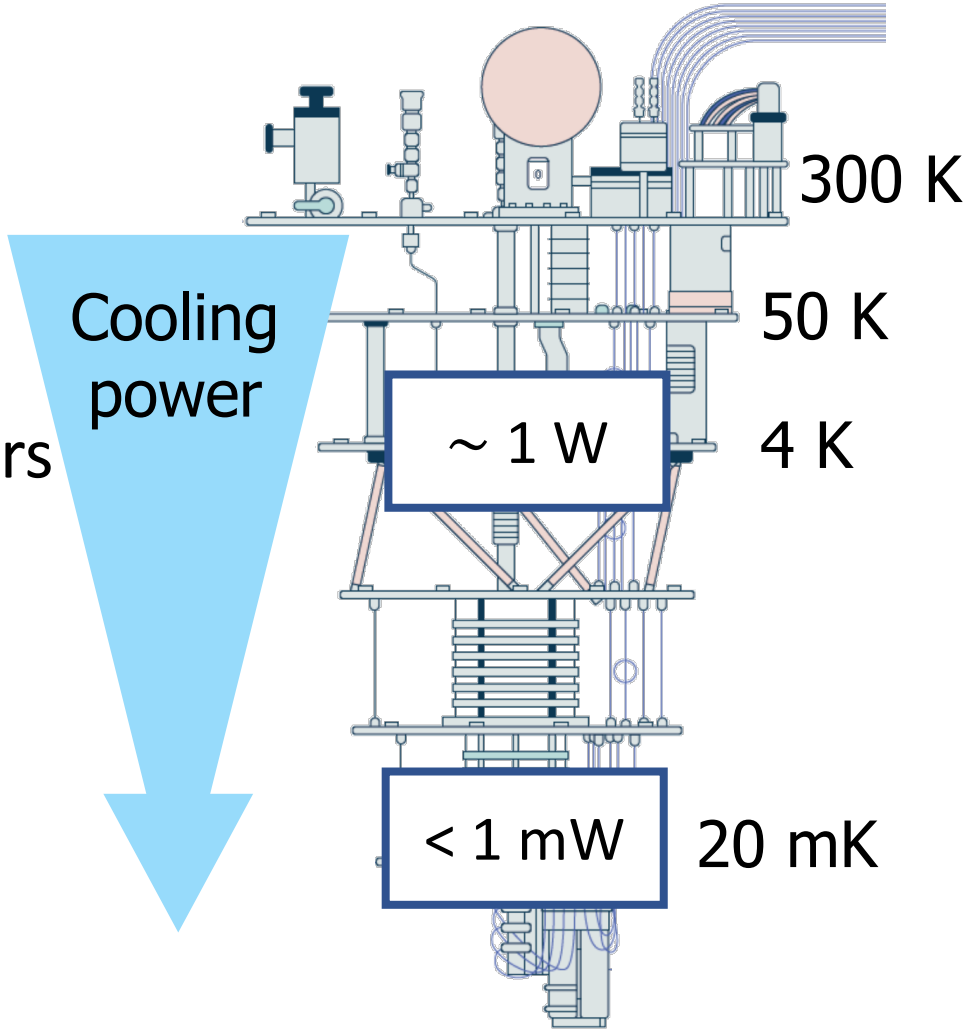
Toward a large-scale quantum computer



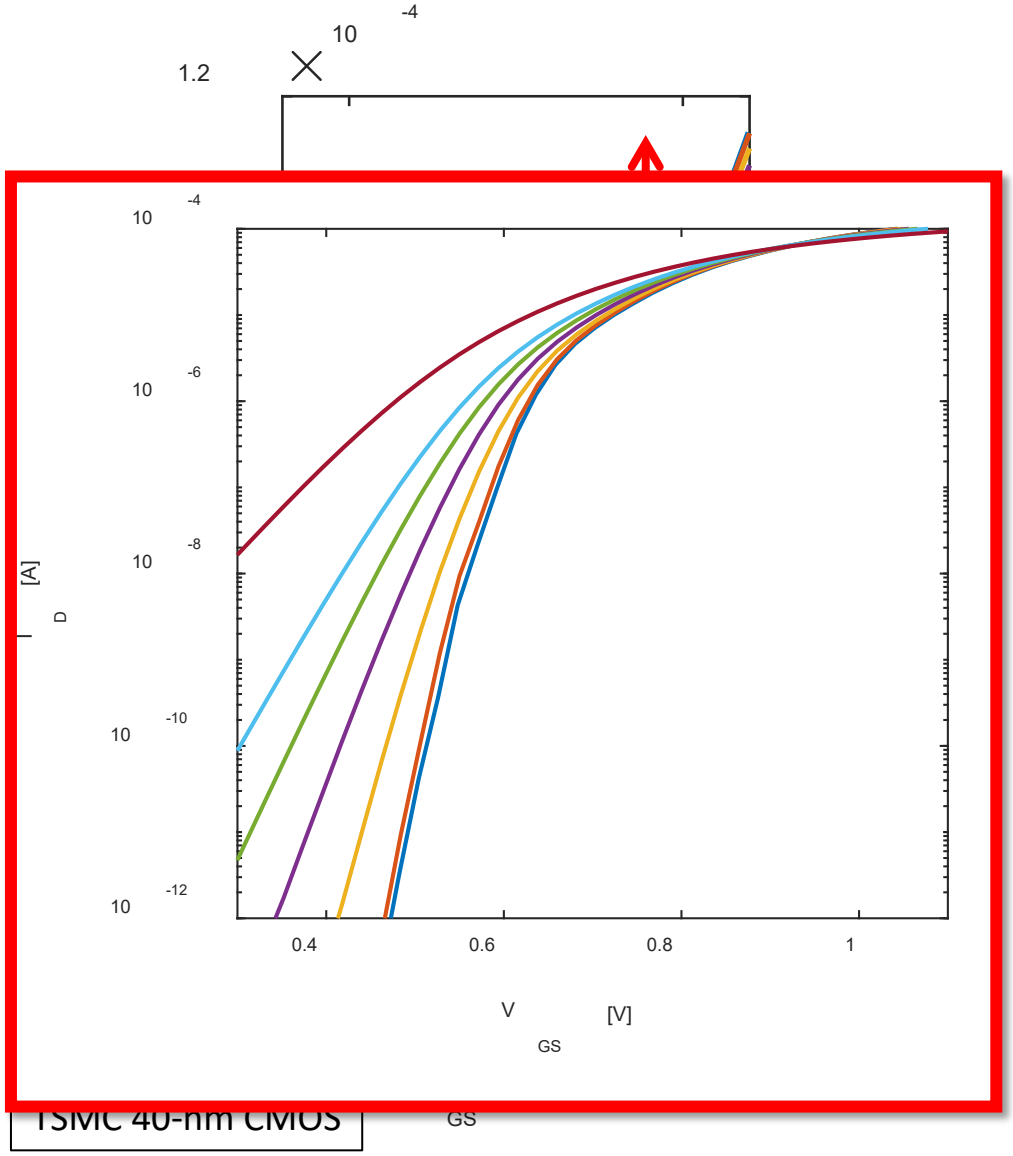
Cryogenic and **integrated** electronic interface
for **large-scale** quantum computers

Challenges for Interface Electronics

- High-Performance
  - Do not limit qubit *fidelity*
- Power dissipation
  - Compatible with existing cryo-refrigerators
  - Typical figure: 1 mW/qubit
  - Fundamental limit: *heat extraction*
- Cryogenic technology
  - Operate at 4 K and below
  - Very Large Scale of Integration (VLSI)
  - **Cryogenic CMOS (cryo-CMOS)**



Commercial CMOS going cryo – Cryo-CMOS



[Incandela JEDS 2018; Patra JEDS 2020; 't Hart JEDS 2020/2021]

- **Transistors behave as transistors**

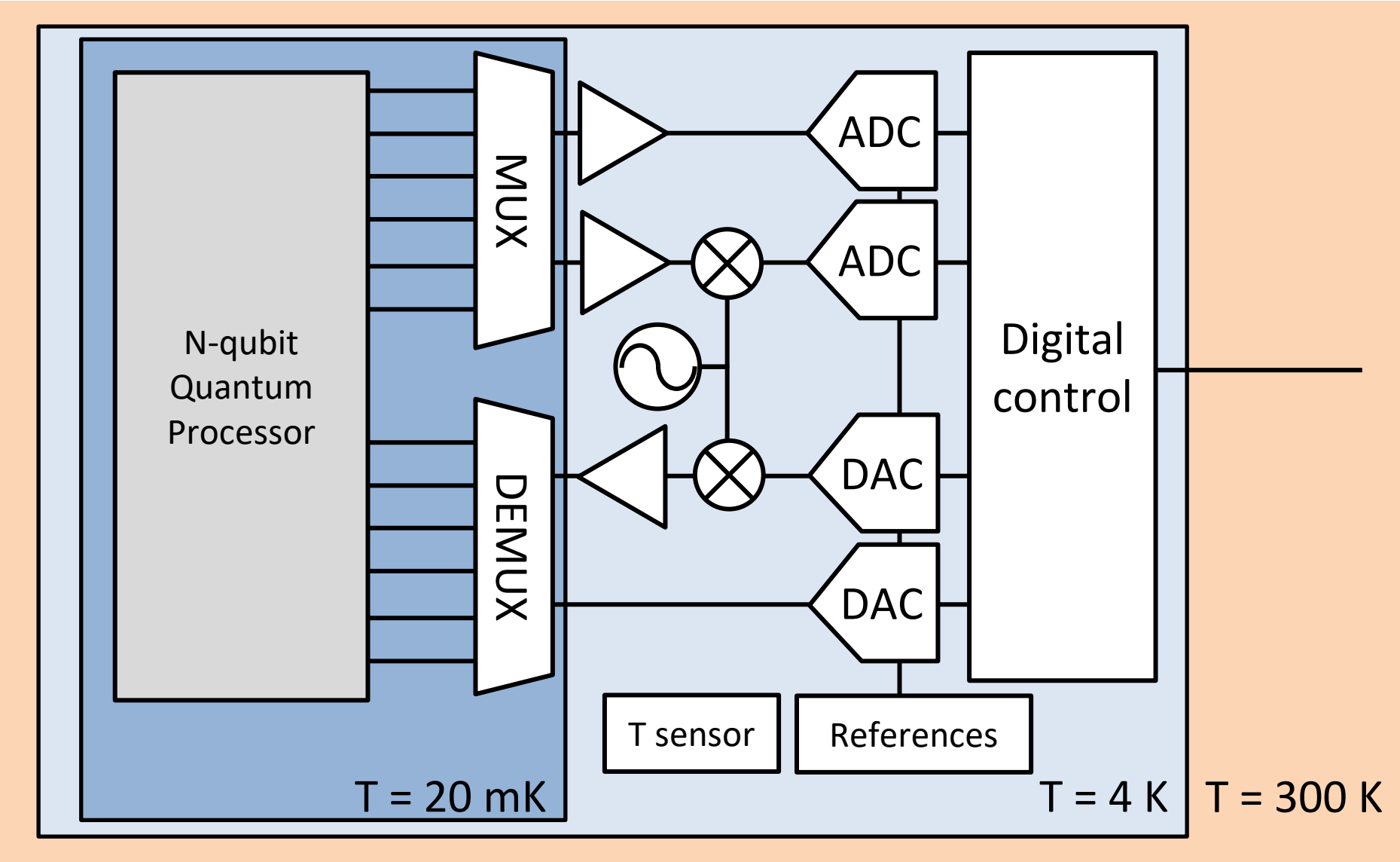
Pro's

- Higher mobility ⇒ more current ⇒ more speed
- Less resistive/capacitive parasitics
- High-quality passives (L/C)
- Steeper subthreshold slope ⇒ Less leakage
  ⇒ More transconductance/gain
- Lower thermal noise

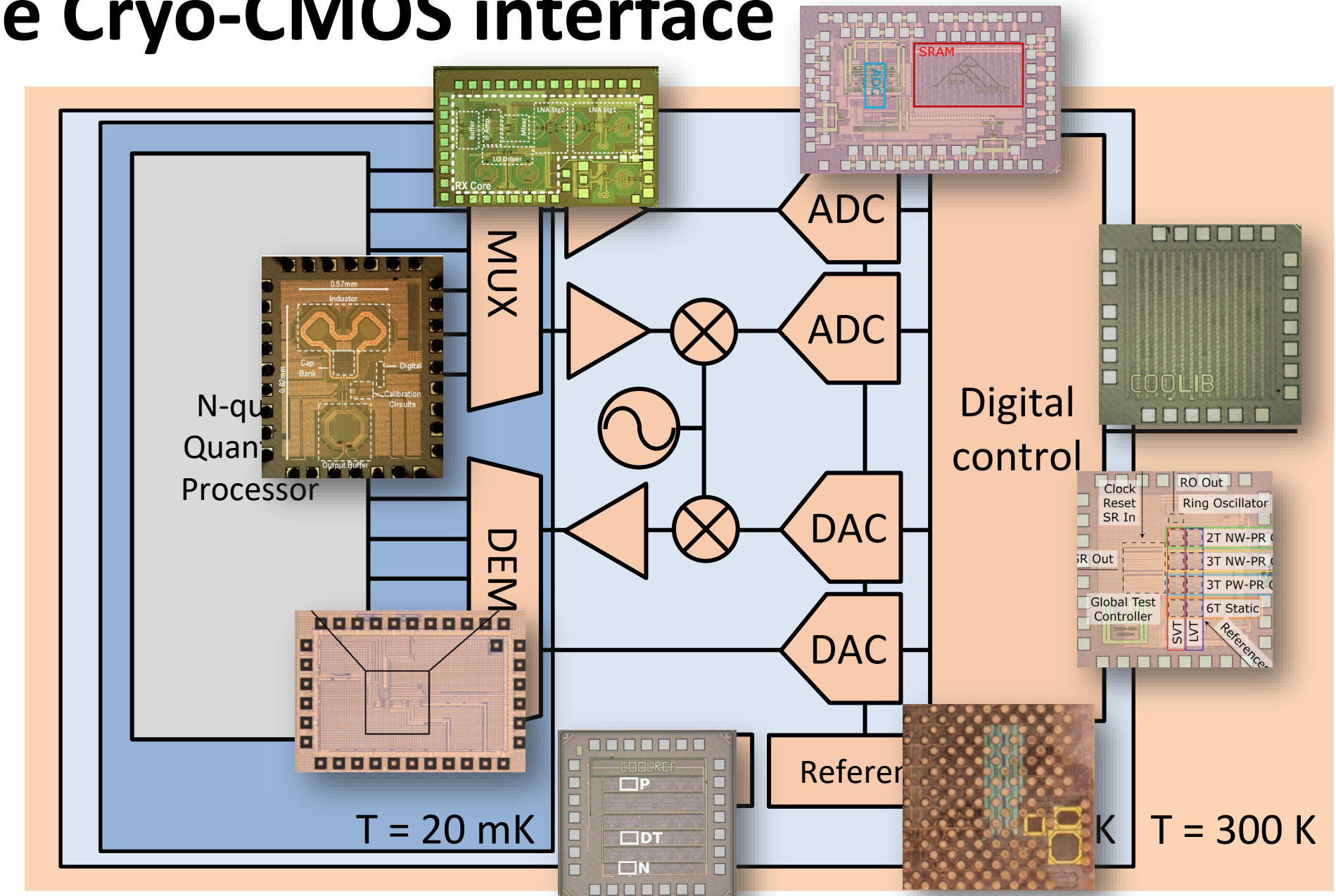
Cons'

- **No good compact models**
- Higher threshold ⇒ less voltage headroom
- (Slightly) more mismatch
- Humps/bumps in weak inversion
- Self-heating

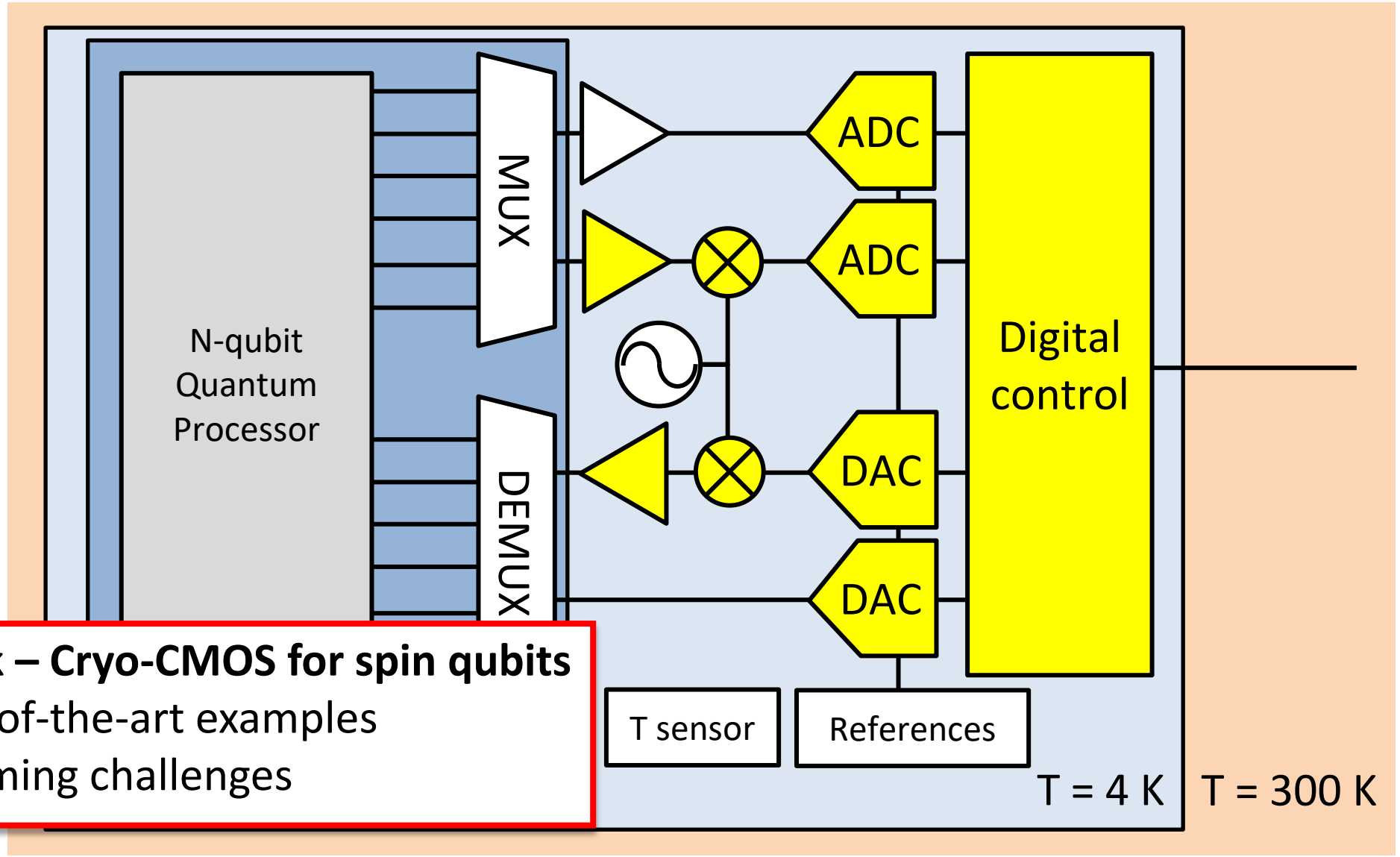
The Cryo-CMOS interface



The Cryo-CMOS interface



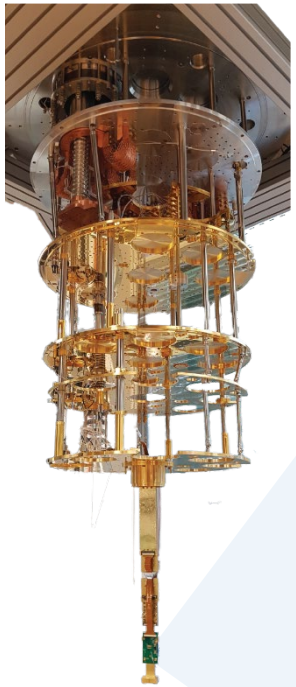
The Cryo-CMOS interface



This talk – Cryo-CMOS for spin qubits

- State-of-the-art examples
- Upcoming challenges

Cryogenic qubits

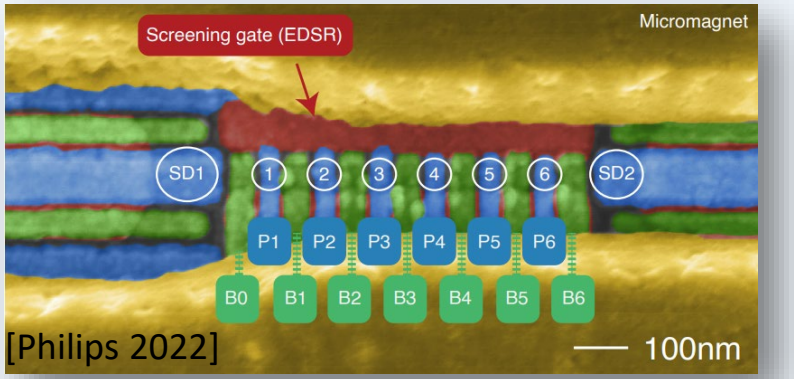


$|0\rangle$ $|1\rangle$

$|\psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle$

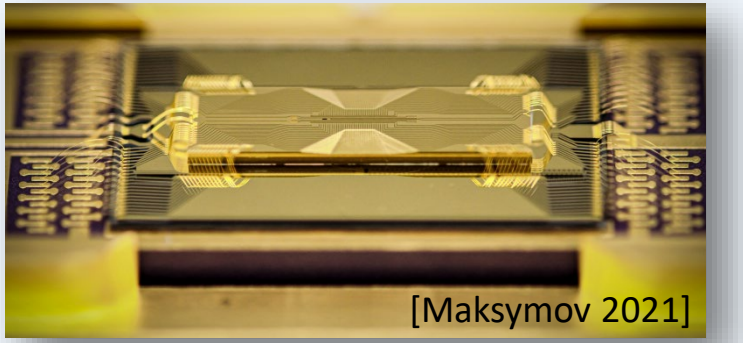
Superposition

Real-life qubits

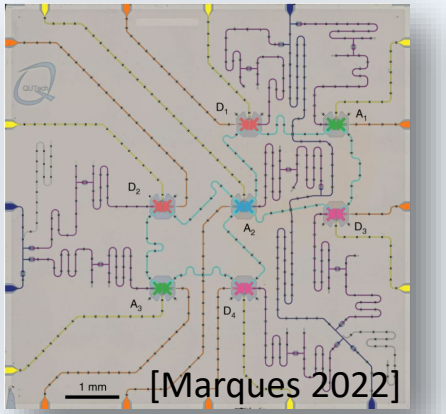


Spin qubits in semiconductors

Spin in diamonds

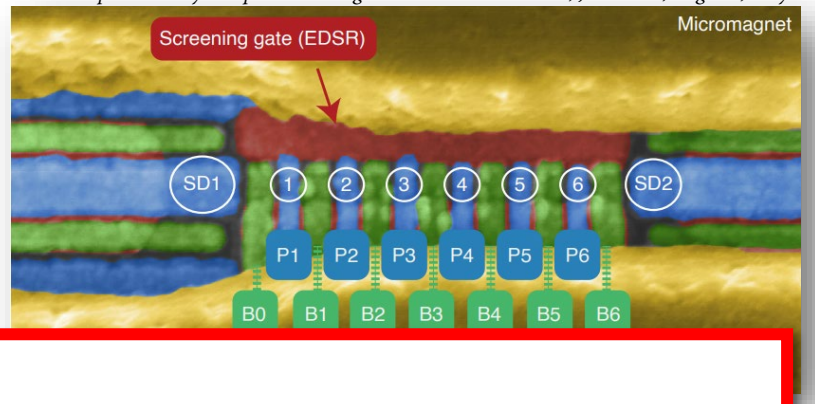


Ion traps

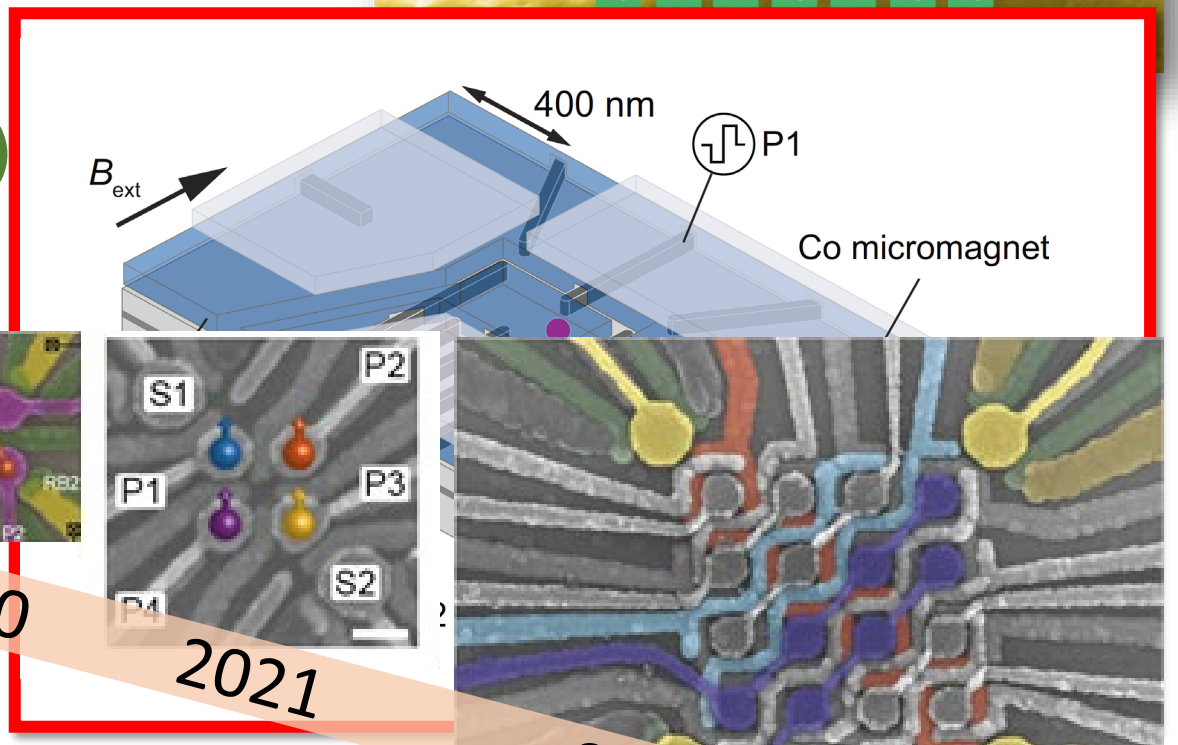


Superconducting

Spin qubits in semiconductors



- **Exploit semiconductor manufacturing**
- **Monolithic integration with electronics**
- **Good fidelity, high-temperature operation (> 1 K)**
- **Potentially, no need for microwaves**

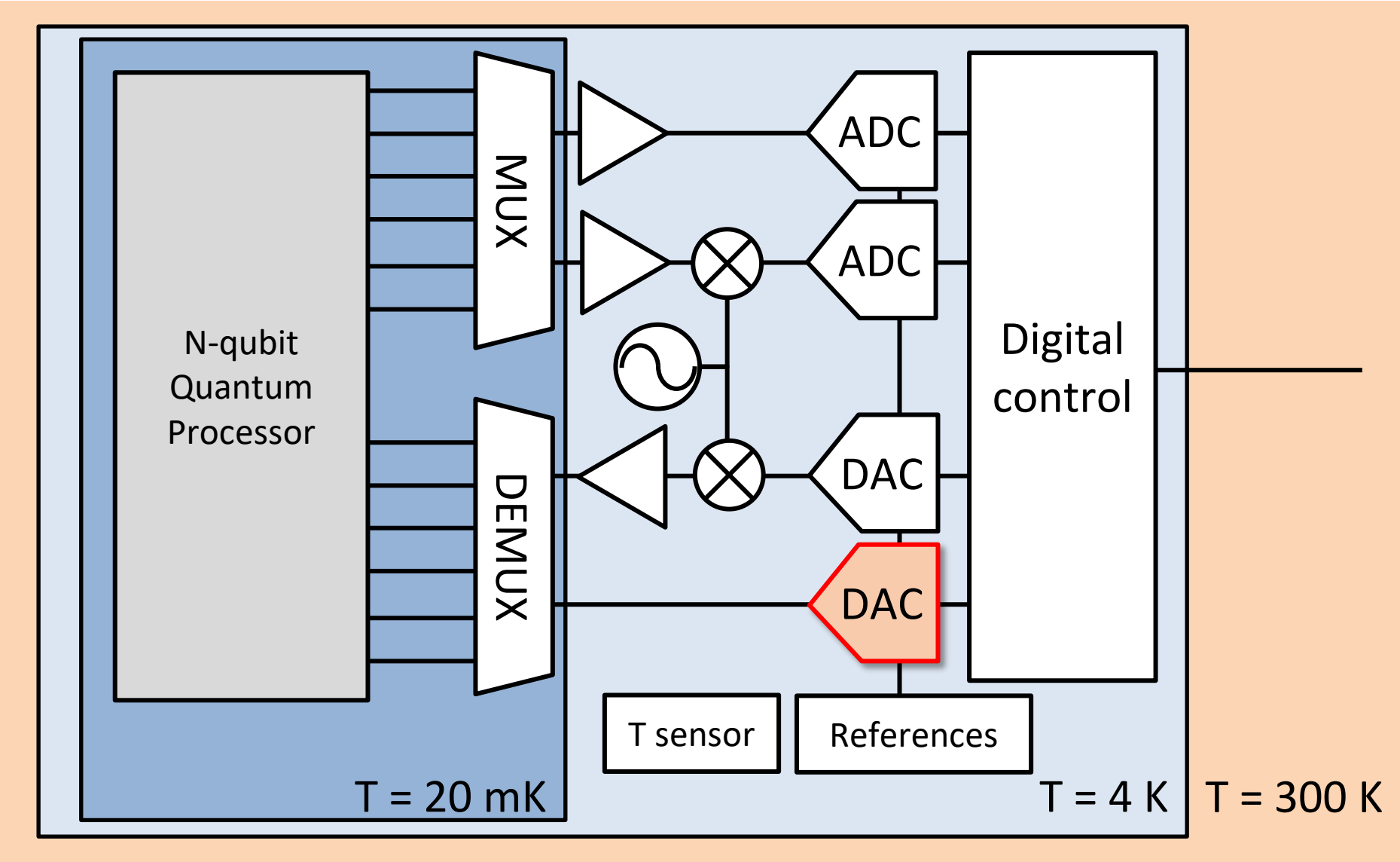


[Courtesy: M. Veldhorst, TU Delft]

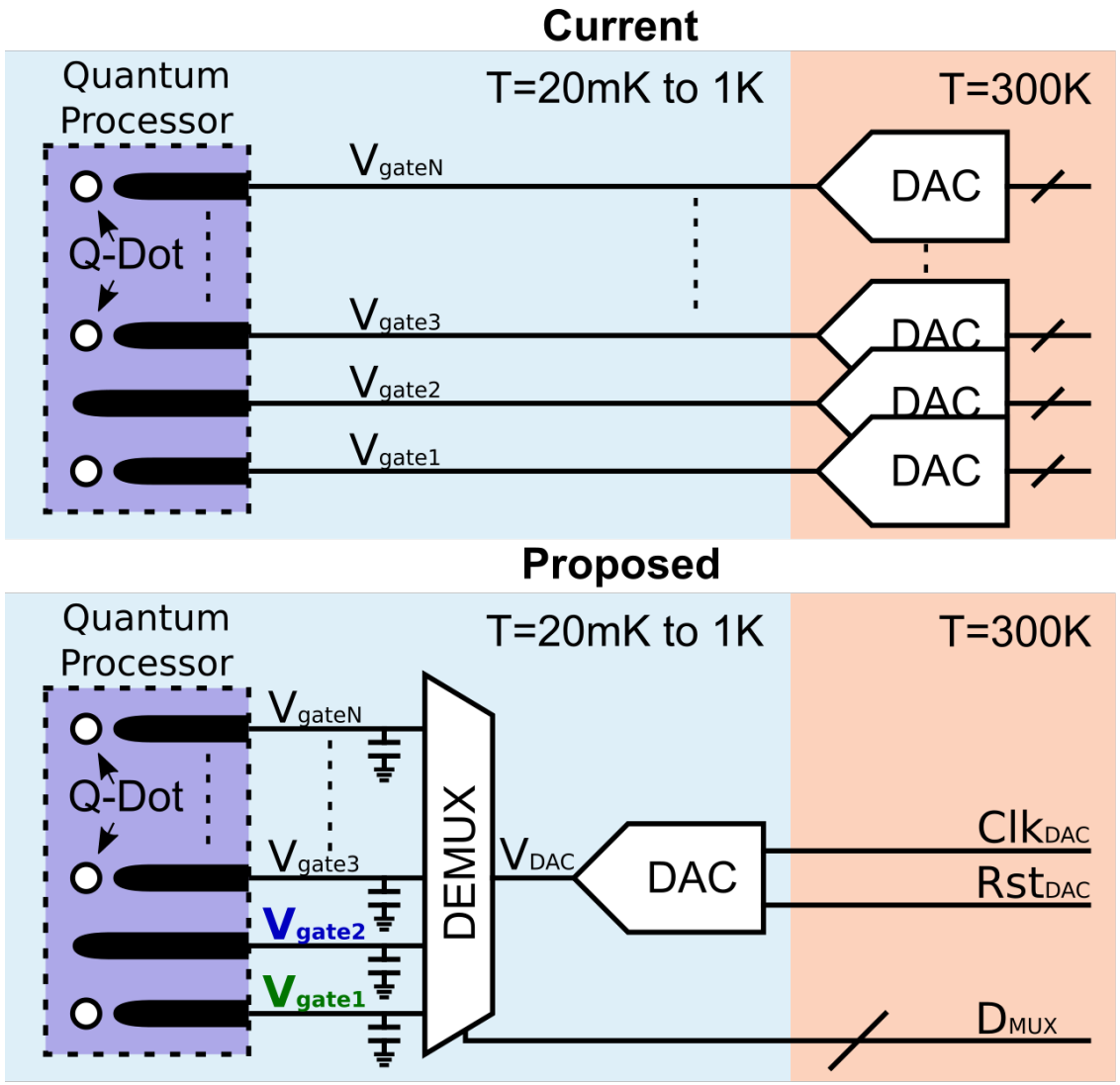
However,…

- Only small-scale demonstrations (6 qubits)
- Very fine pitch
  - ⇒ Addressability?
  - ⇒ Space for electronics?
- Need for extreme uniformity

The Cryo-CMOS interface



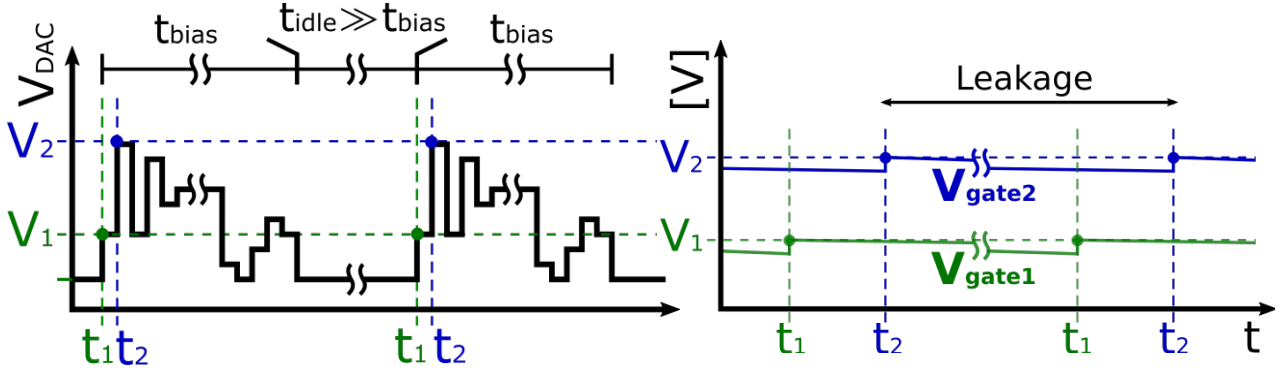
Gate biasing



[VLSI 2022]

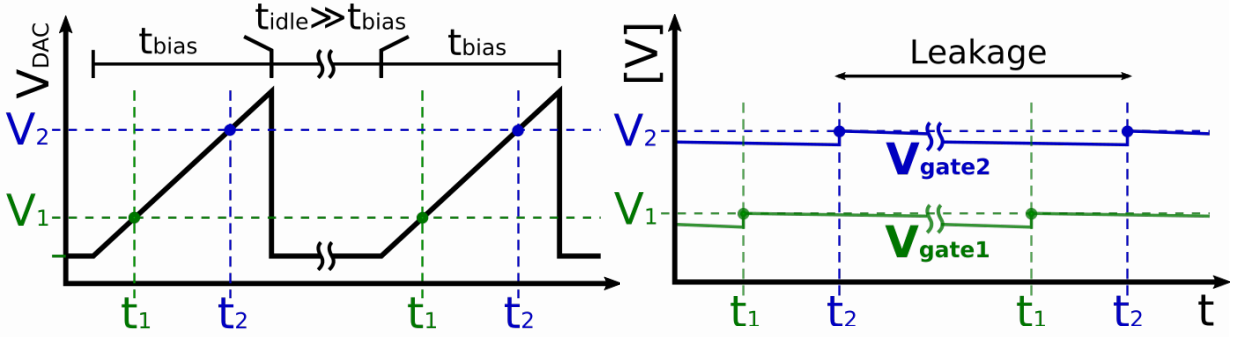
Gate biasing

Address-based biasing

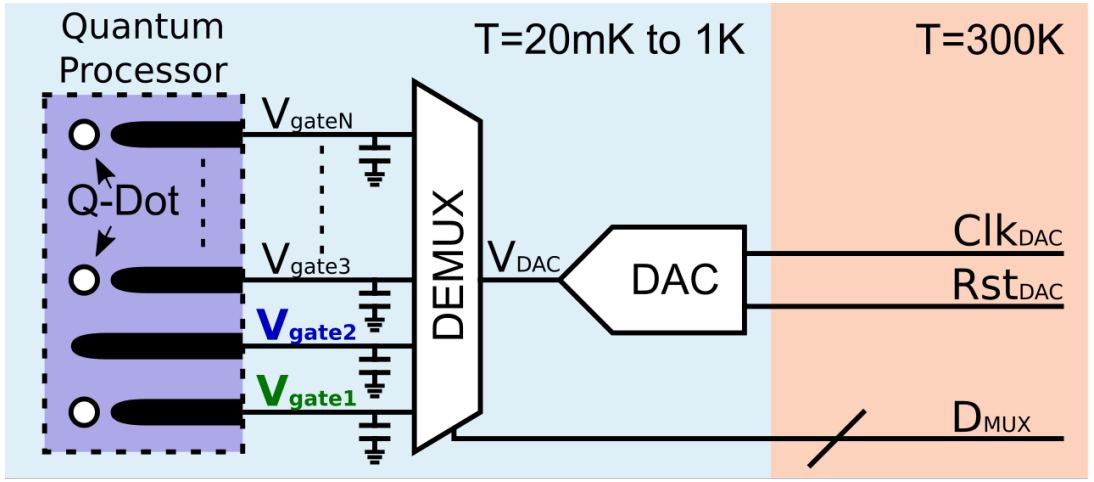


- Power ∝ N_{gates}
- Requires accurate DAC

Voltage-based biasing

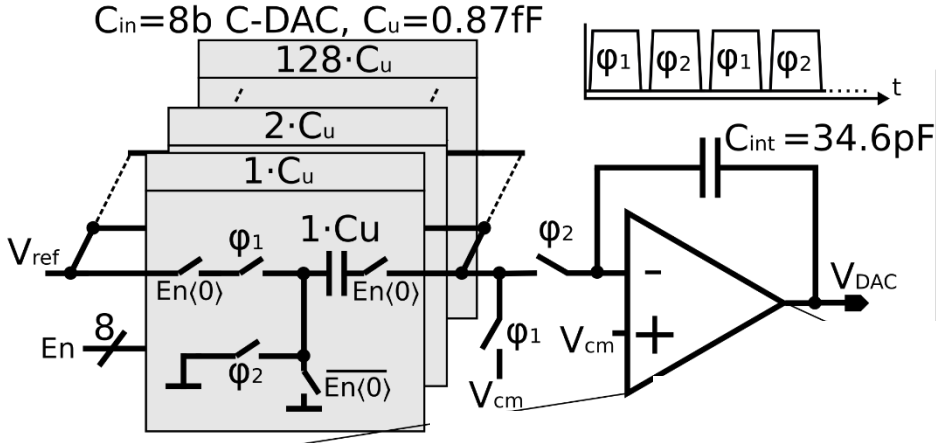


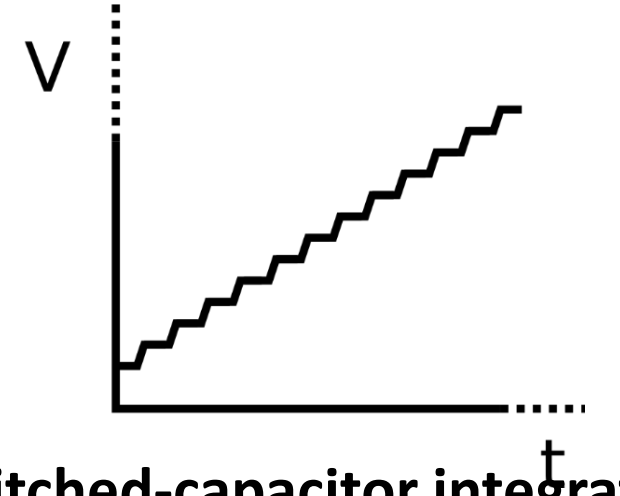
- Power ~ independent form N_{gates}
- Simplified DAC implementation



[VLSI 2022]

A cryo-CMOS Digital-to-Analog Converter



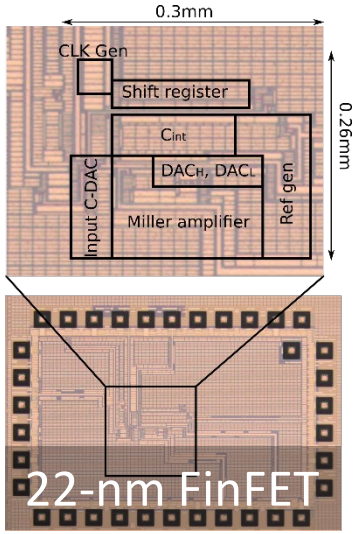


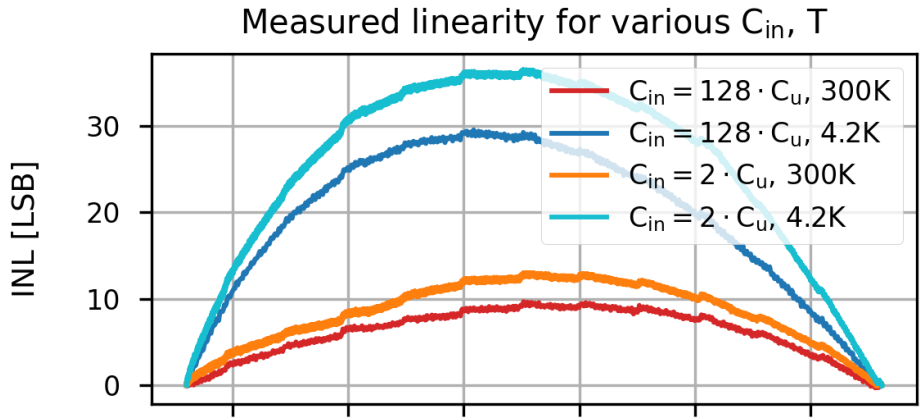
- **Switched-capacitor integrator**
  - Inherently monotonic
  - Discrete steps ⇒ easy to synch
- **Wide output range**
  - 3 V in 1.8-V process
  - Reliability by protection devices

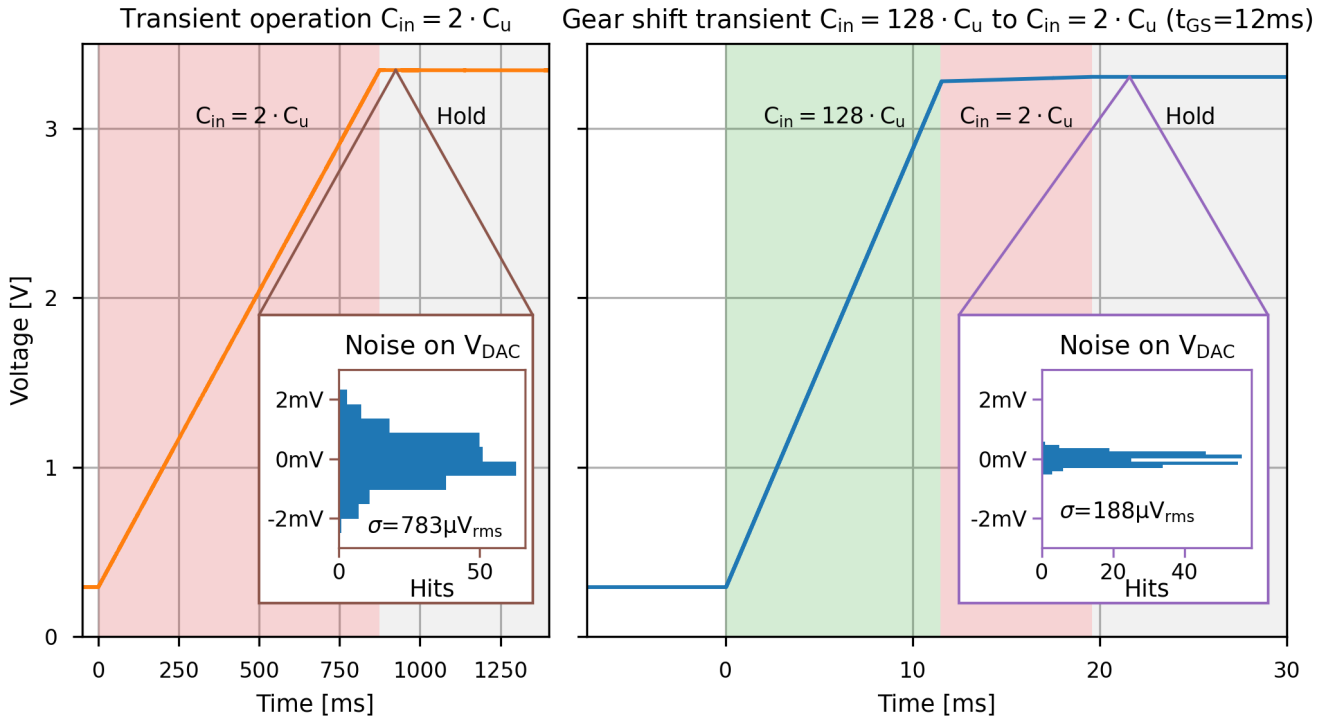
[VLSI 2022]

Cryo-CMOS DAC Results

- Power = 157 µW
- 15-bit DAC
  - 3 V range
  - Step size < 60 µV
  - Non-linearity < 2 mV
- Latency: 20 ms – 1 s

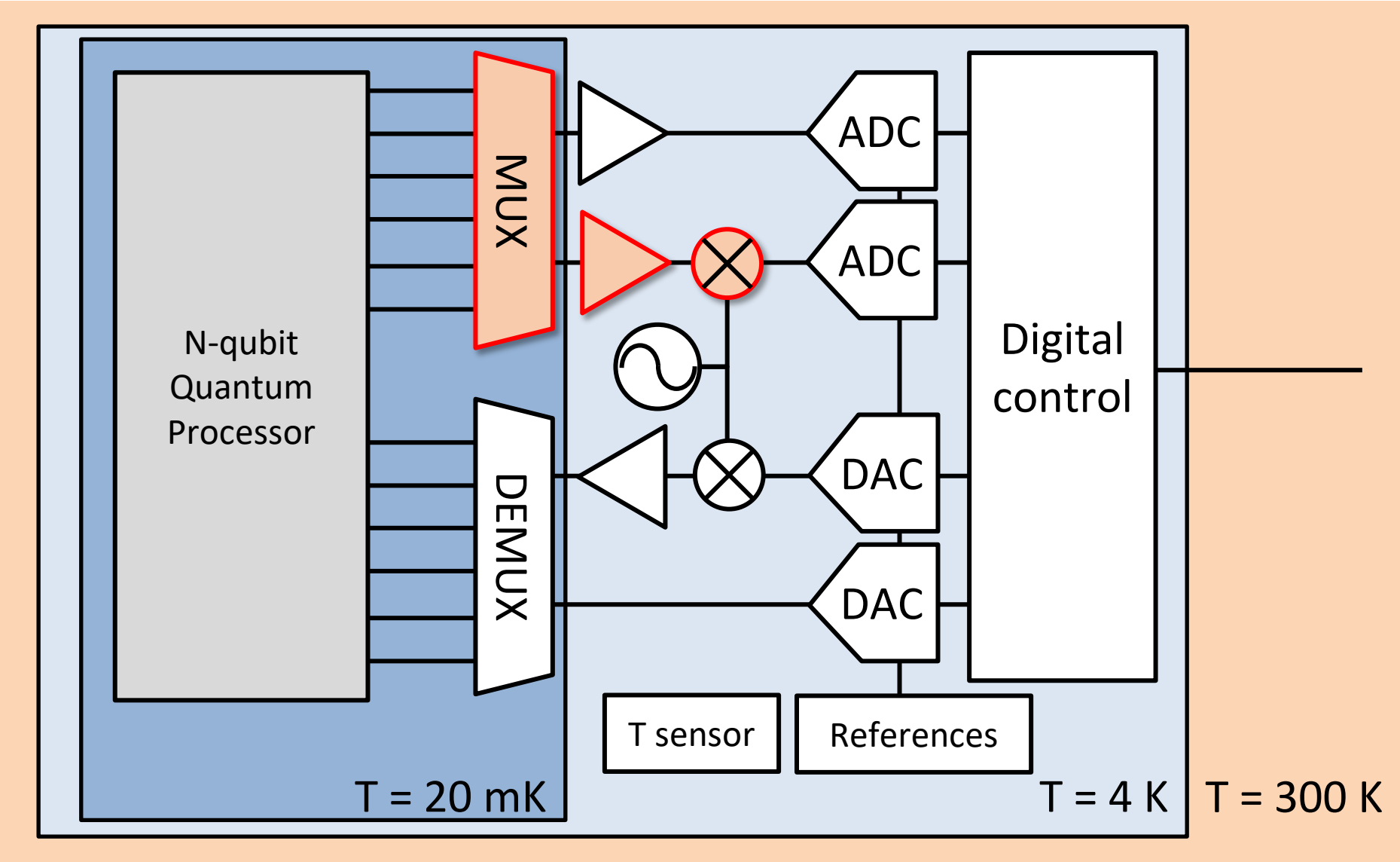




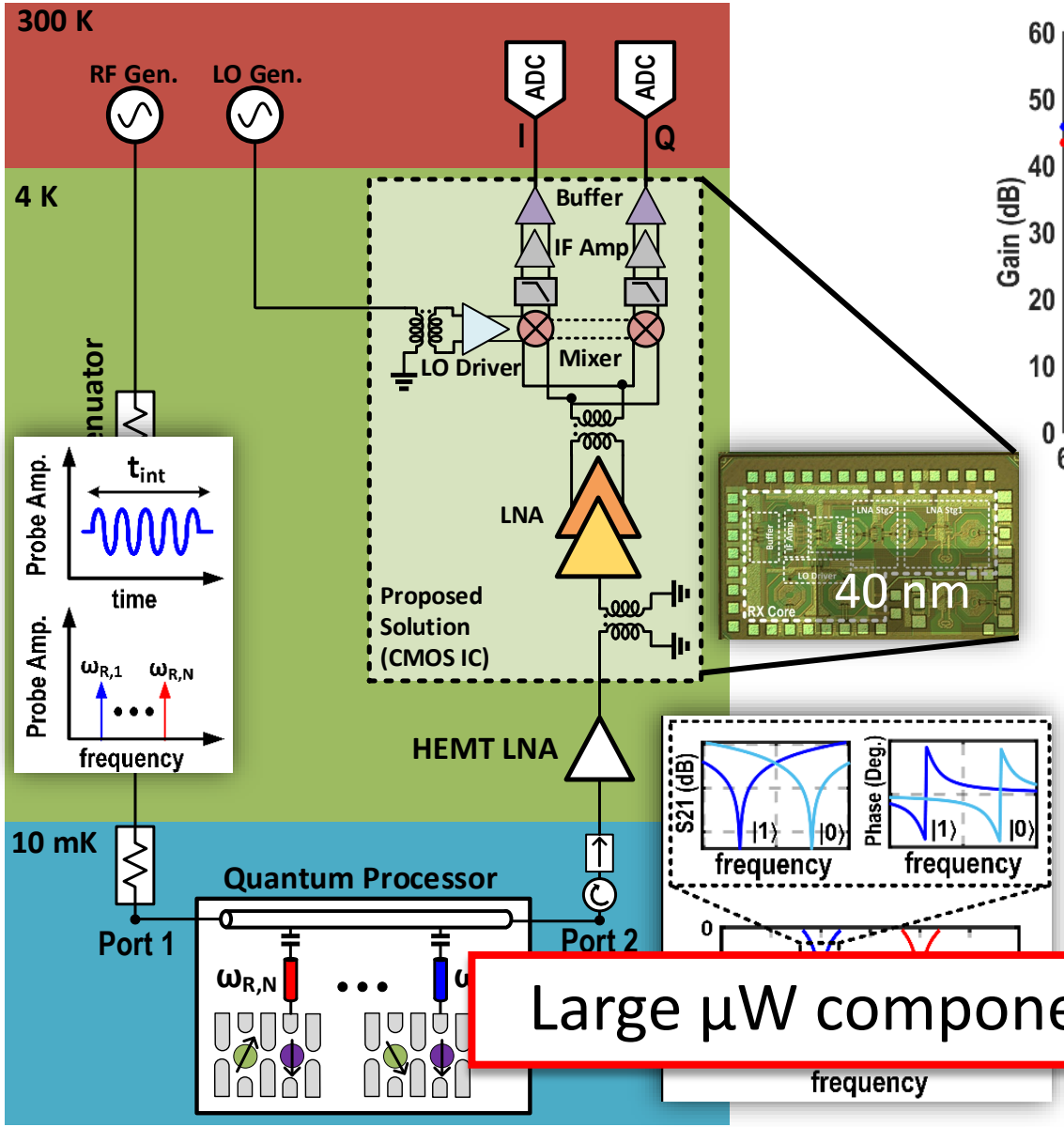


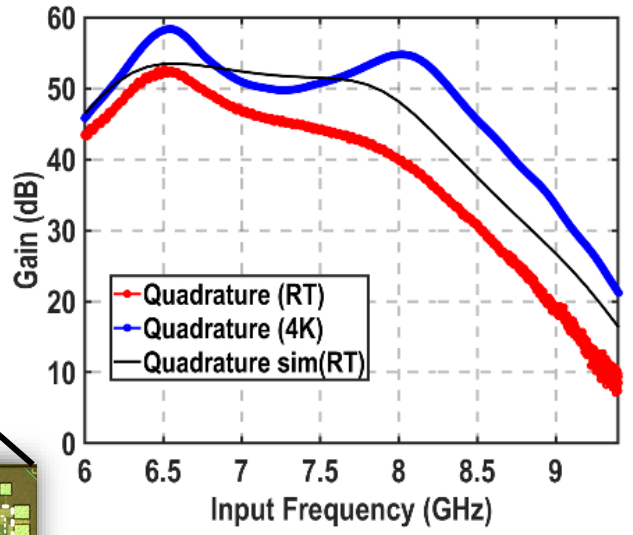
[VLSI 2022]

The Cryo-CMOS interface

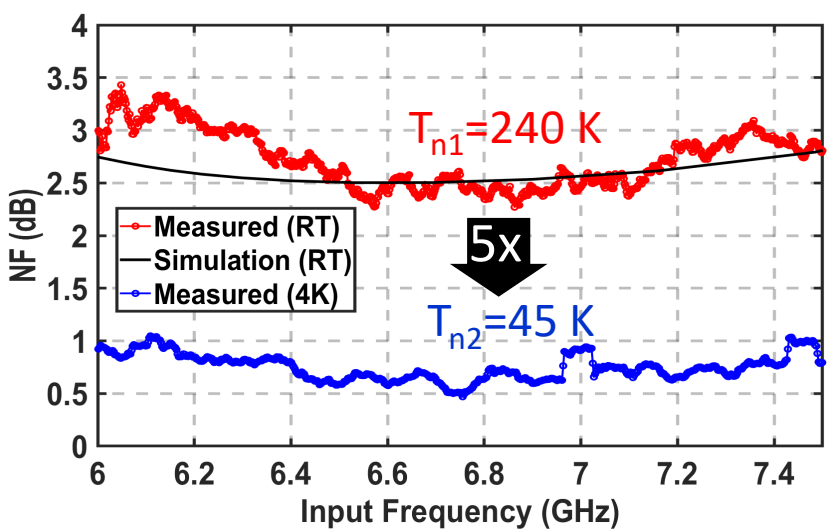


A Cryo-CMOS Readout





Noise performance

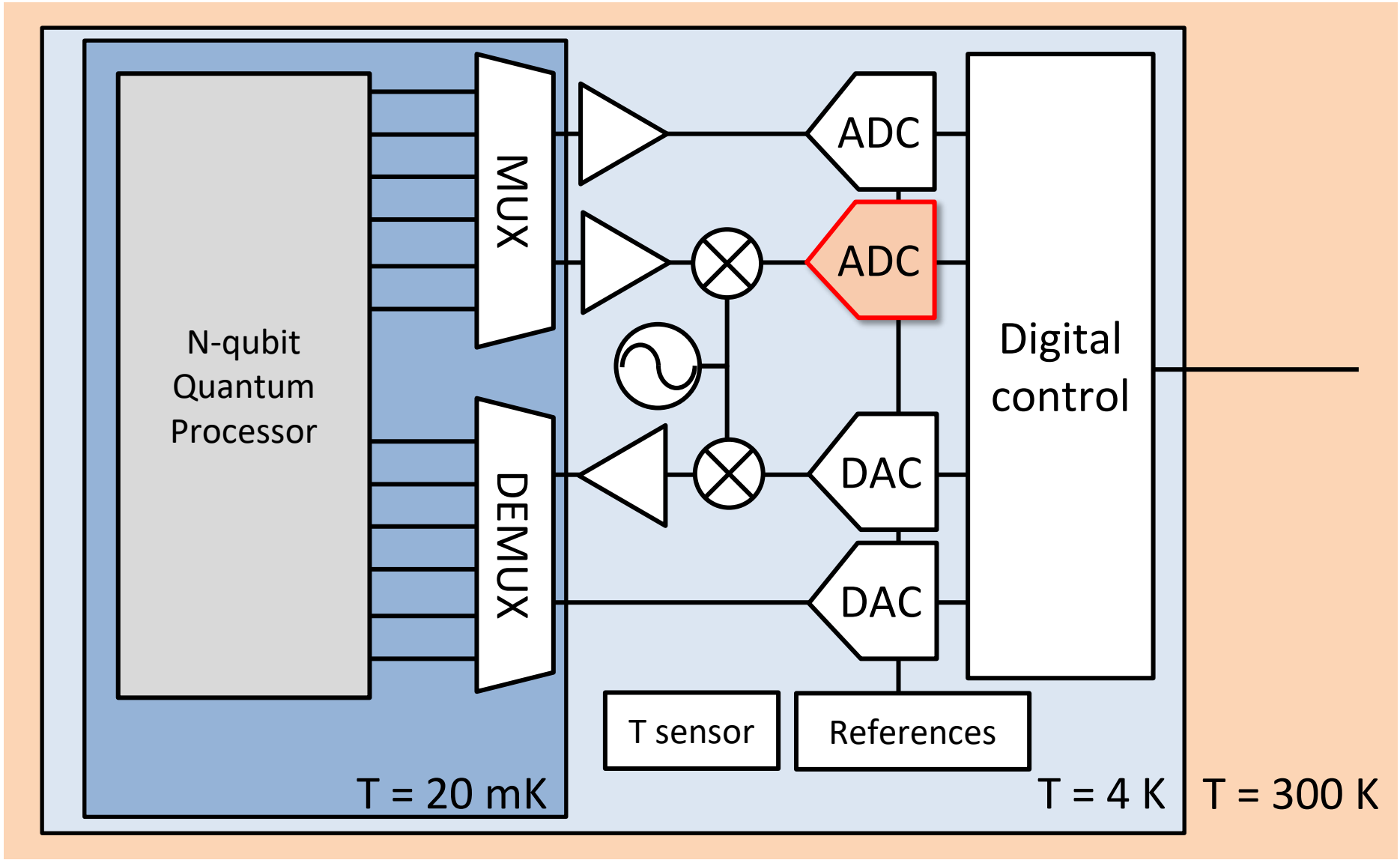


- Power = 66 mW
- 400 qubits, BW=2 MHz ⇒ **170 µW/qubit**
- But still external pre-amplifier
- Lower noise (T_n=15 K) but lower BW in [Prabowo, ISSCC 2024]

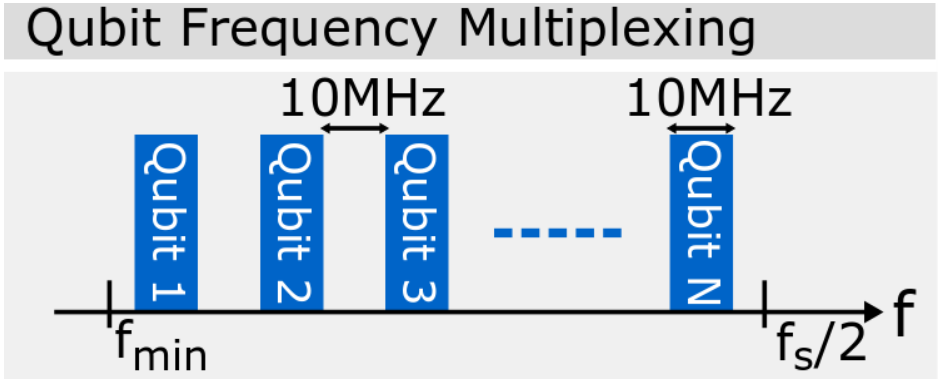
Large µW components (resonators or LC) still needed

[ISSCC 2021]

The Cryo-CMOS interface

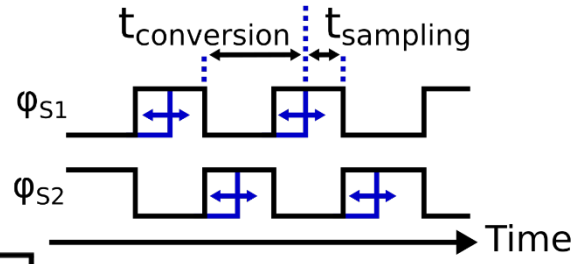


Cryo-CMOS Analog-to-Digital Converter



Requirements

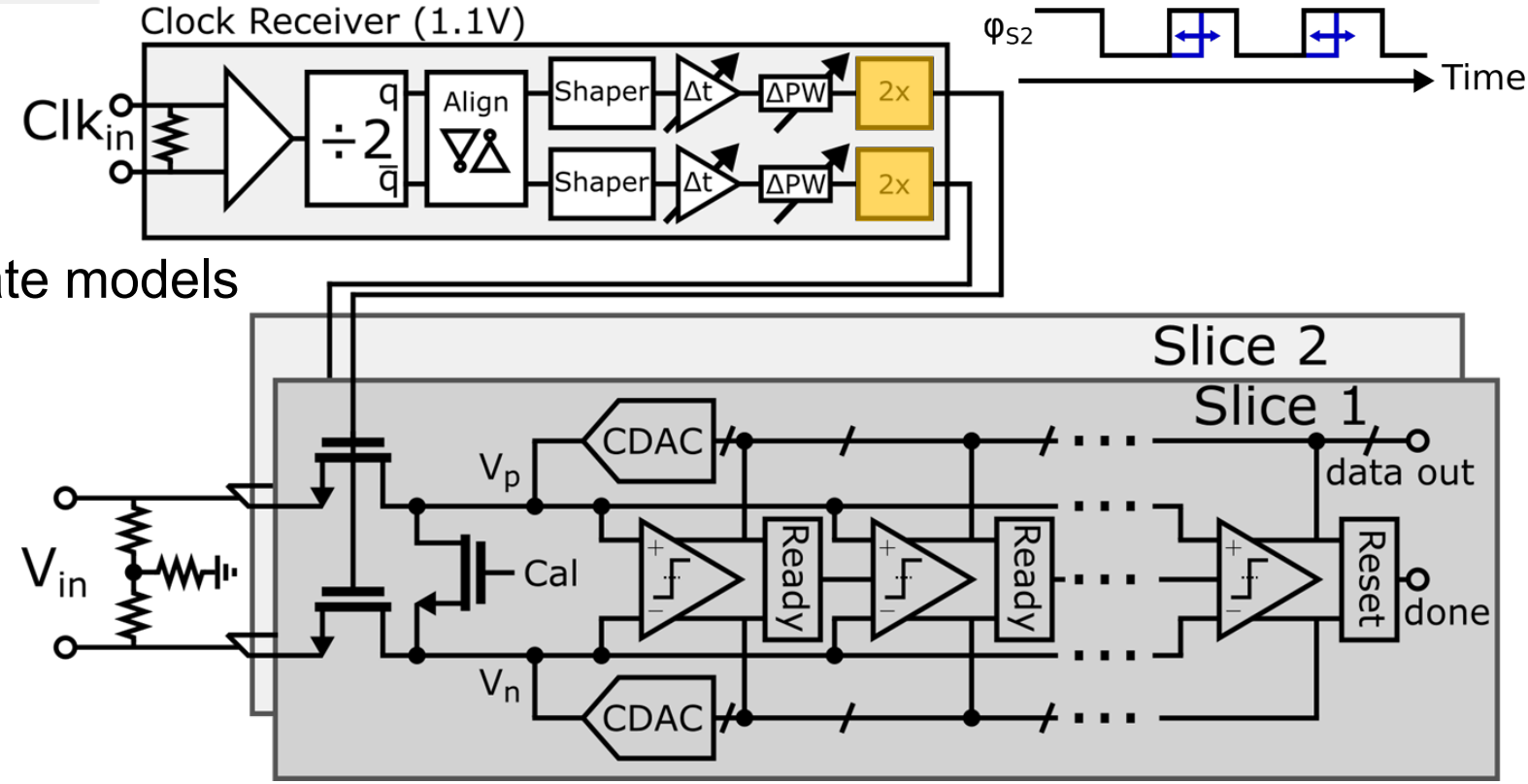
- 1 GSa/s for 20 qubit channels
- ENOB: 7 bit



Approach

- Power efficiency ⇒ SAR ADC
  - Mainly digital ⇒ no need for accurate models
- Speed
  - Loop unrolled
  - 2x time interleaved
- Cryogenic operation

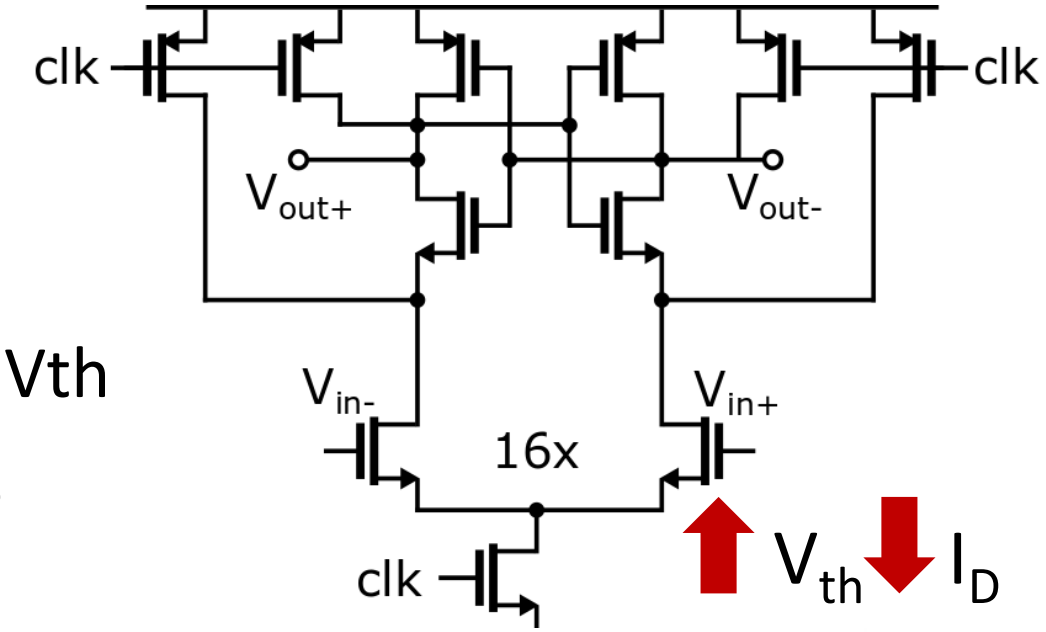
  [higher Vth, limited headroom]
  - **Boosted sampler**

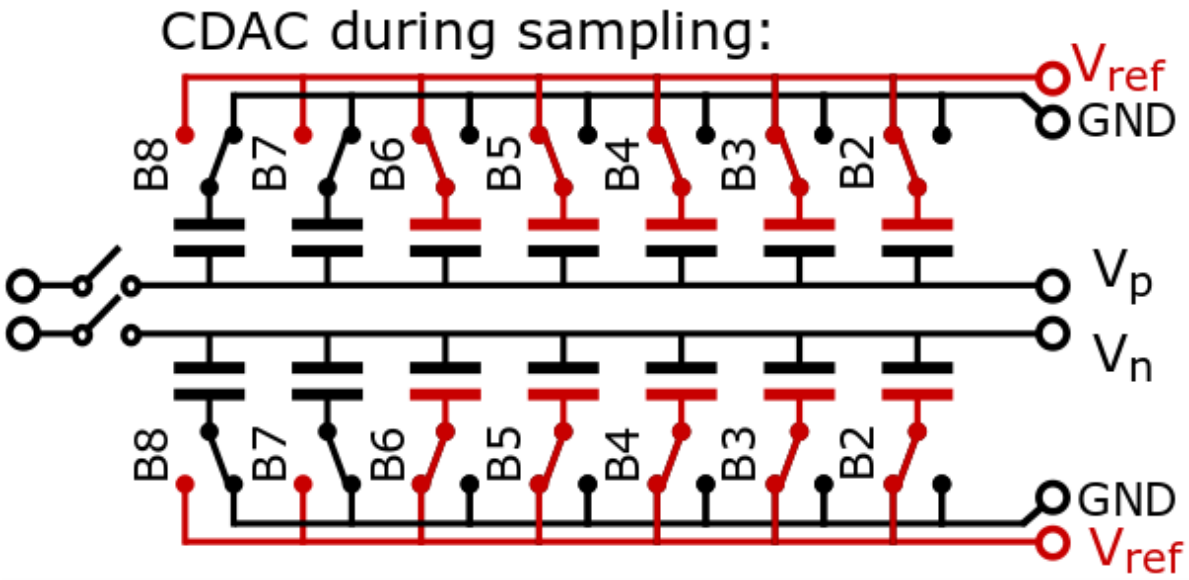


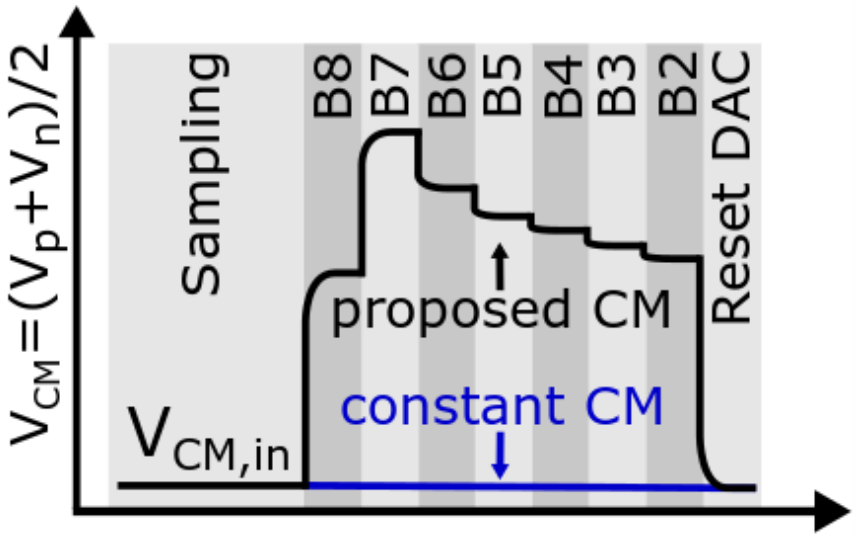
[ISSCC 2021, ESSCIRC 2022, JSSC 2023, TCAS 2023]

Cryo-CMOS comparator

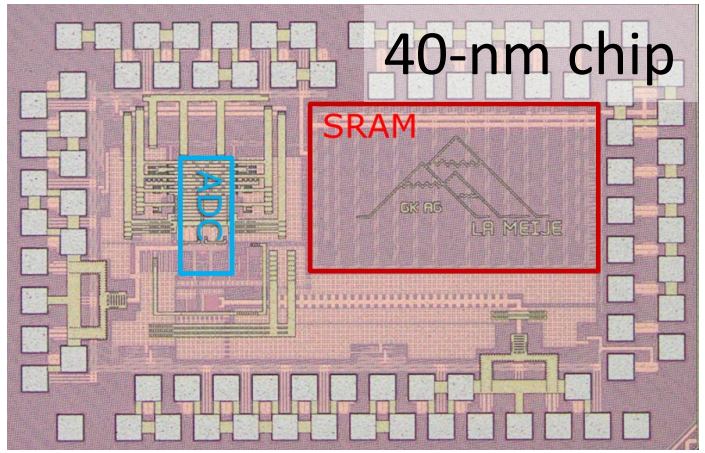
- Classical StrongARM comparator
  - Fast and power efficient
- …but speed/current degrades with higher Vth
- **Solution: adapted CM switching for CDAC**







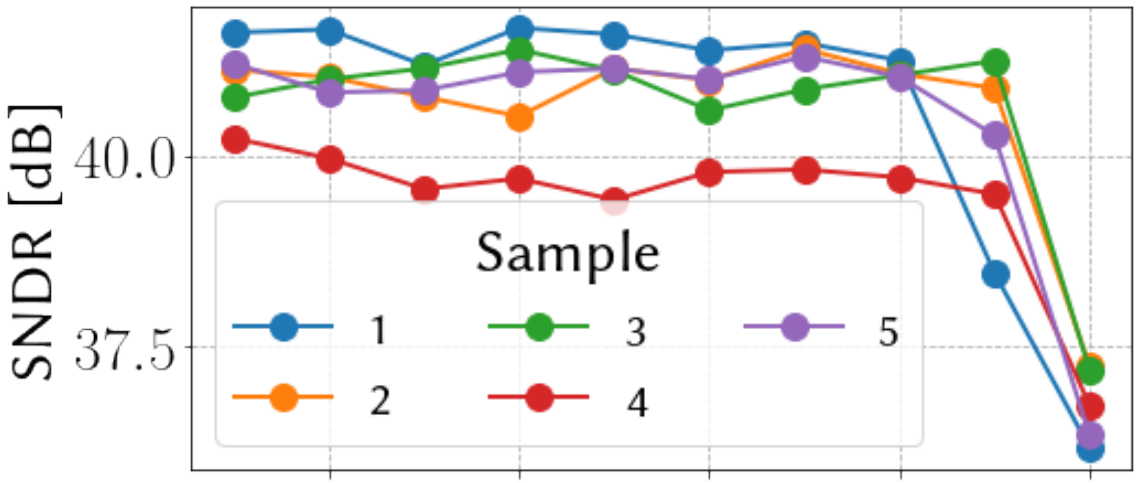
Cryo-CMOS ADC – Performance



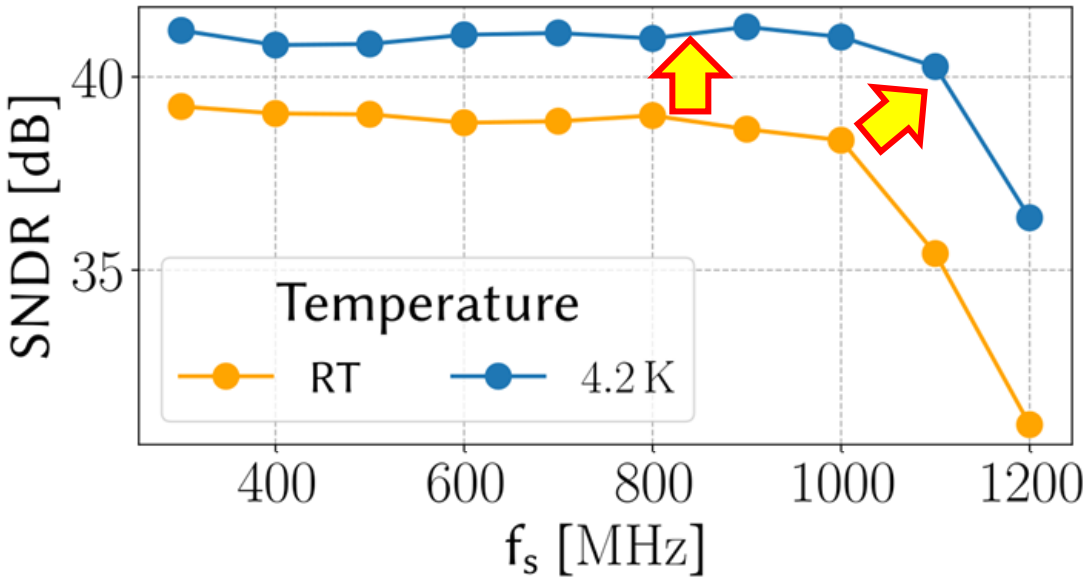
- High performance
  - 1.9 mW @ 1 GSa/s, @ 4.2 K
  - SNDR = 41 dB (6.5 ENOB)
  - State-of-the-art FoM (21 fJ/conv.step)
- Multi-qubit readout
  - 20×10 MHz channels
  - **0.1 mW/qubit**

[ISSCC 2021, ESSCIRC 2022, JSSC 2023, TCAS 2023]

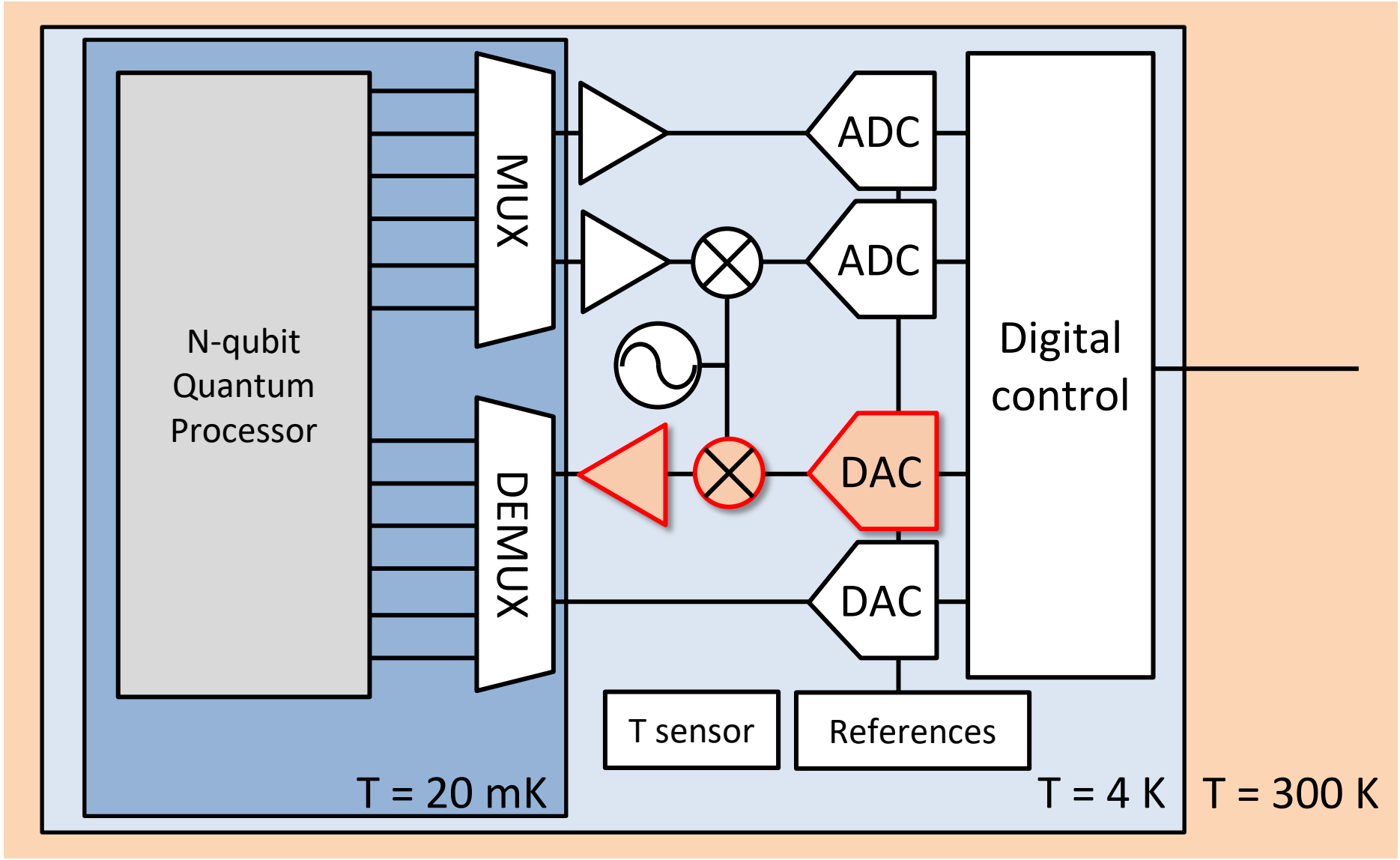
5 samples @ 4.2 K



Sample #5

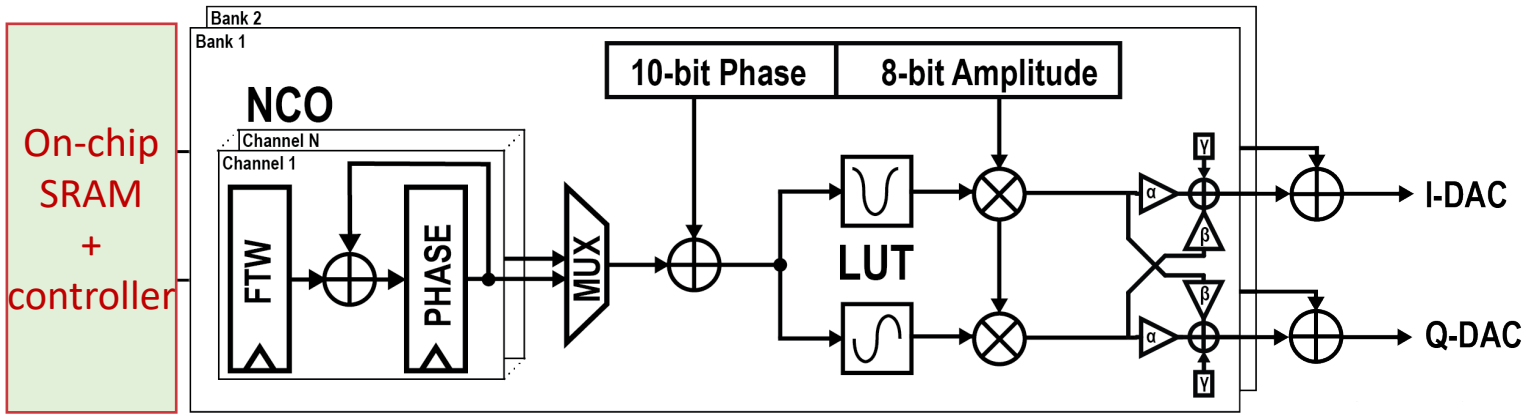


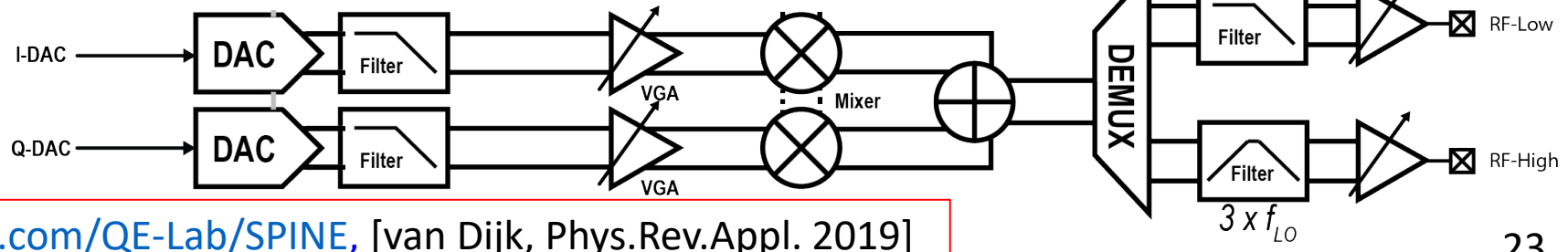
The Cryo-CMOS interface

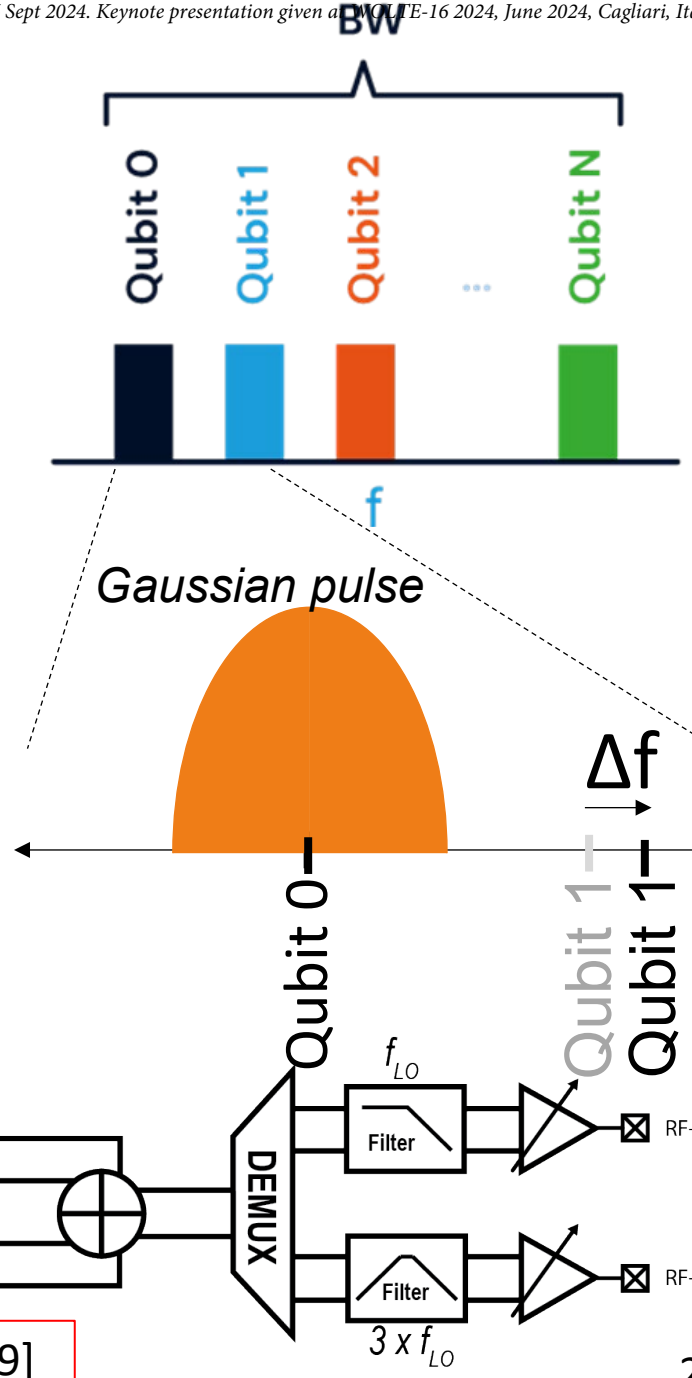


Microwave driver for spin qubits

- **Goal: minimize form factor & power**
  ⇒ FDMA: 32 qubits in 1 GHz BW
- Target electrical performance (from SPINE)
  - Fidelity > 99.99% ⇒ SNR > 44 dB, SFDR > 44 dB
- **Approach**
  - Digital-intensive architecture ⇒ flexibility

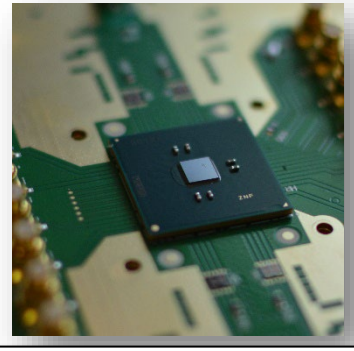






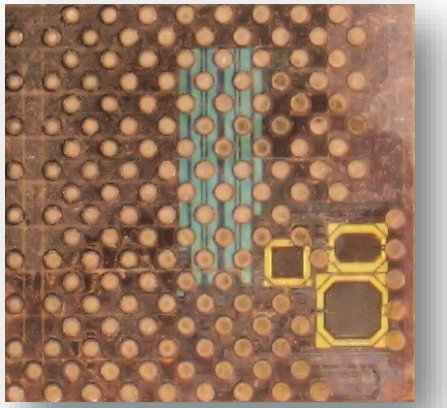
Specs obtained by SPINE: https://github.com/QE-Lab/SPINE, [van Dijk, Phys.Rev.Appl. 2019]

Horse Ridge – Results

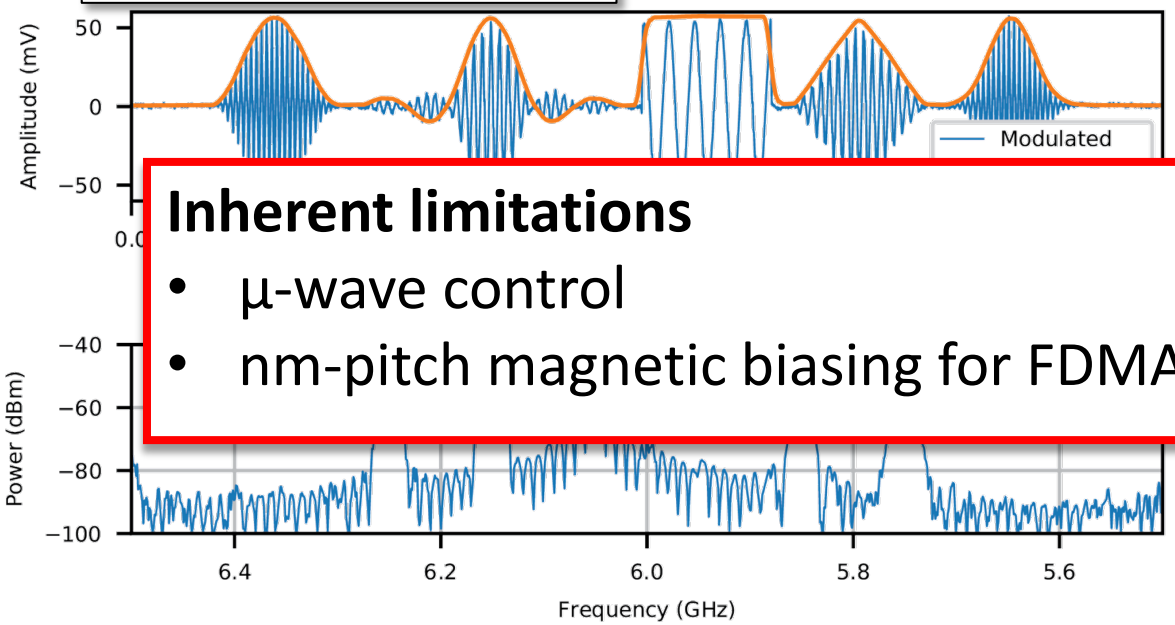


Power @ 3 K:
Analog: 1.7 mW/qubit
Digital: 9.4 mW/qubit

Intel 22-nm FinFET

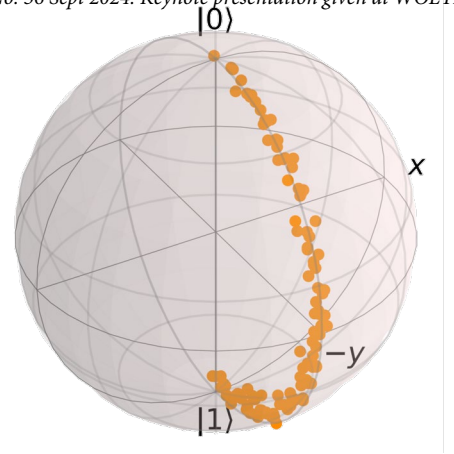


Digital + analog + RF

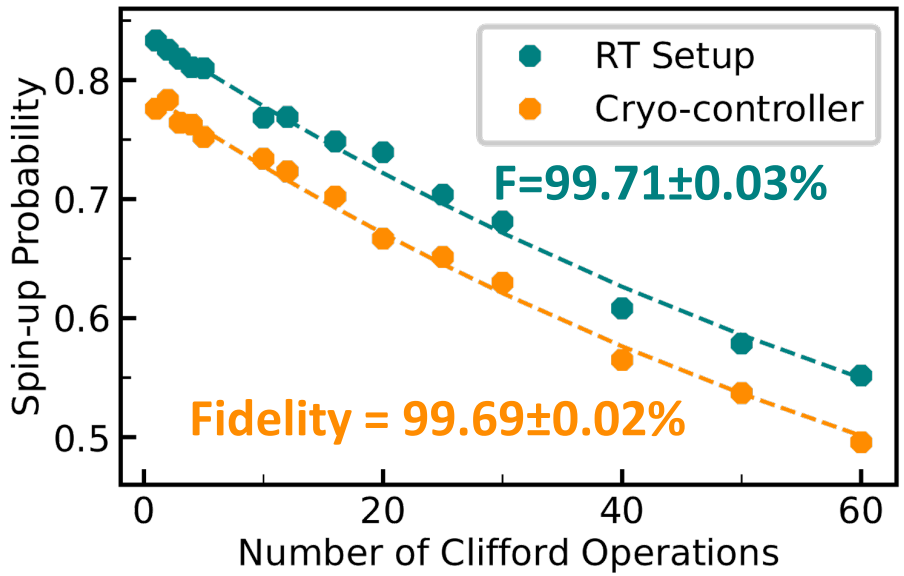


Inherent limitations

- μ-wave control
- nm-pitch magnetic biasing for FDMA



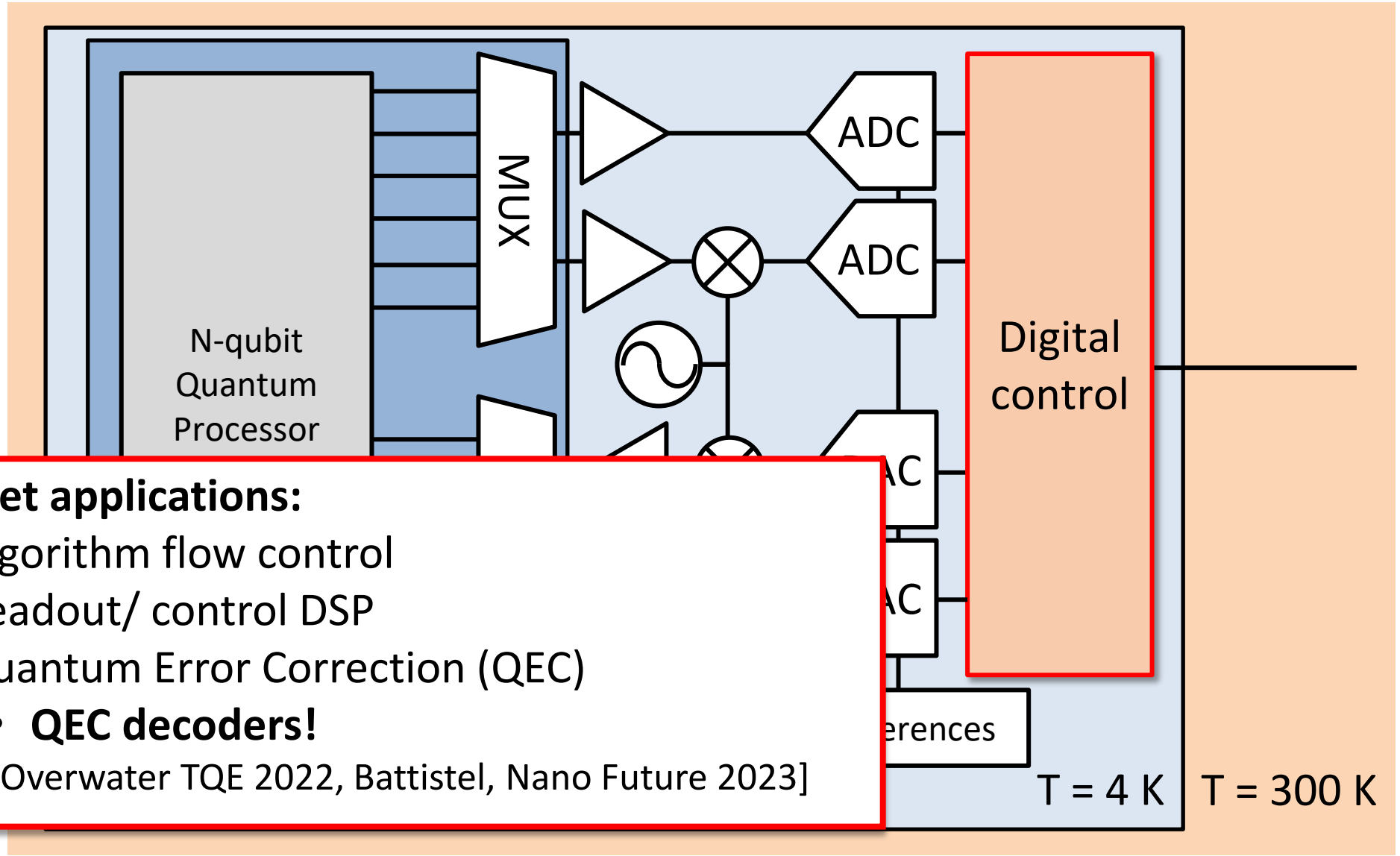
Randomized benchmarking



Fidelity not limited by cryo-CMOS!

[Xue, Nature 2021]

The Cryo-CMOS interface

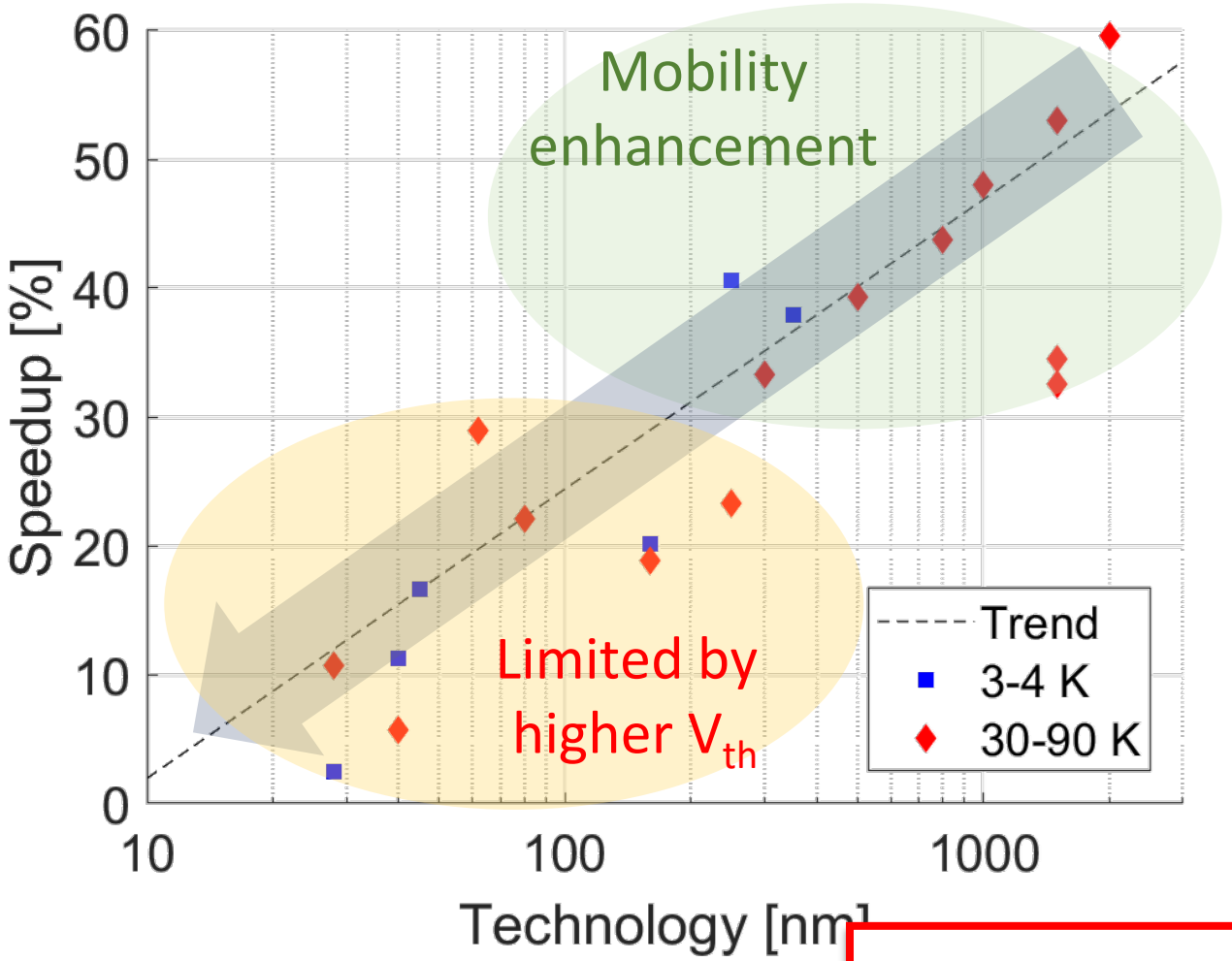


Target applications:

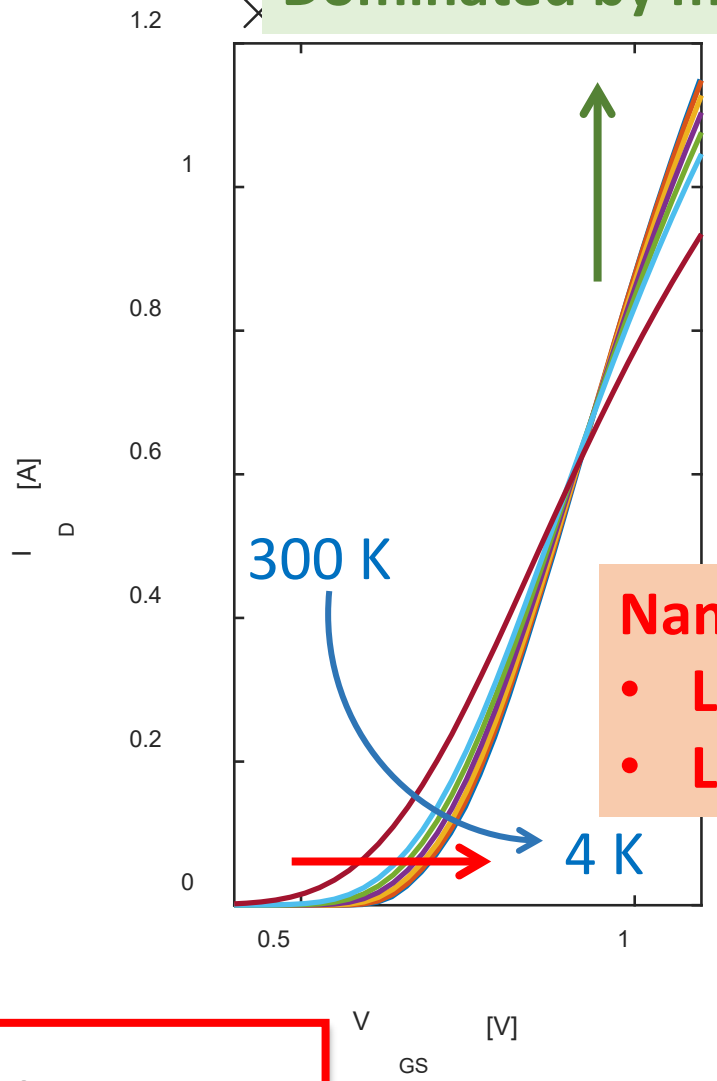
- Algorithm flow control
- Readout/ control DSP
- Quantum Error Correction (QEC)
  - **QEC decoders!**

  [Overwater TQE 2022, Battistel, Nano Future 2023]

Cryo-CMOS digital speed



Mature CMOS
Dominated by mobility increase



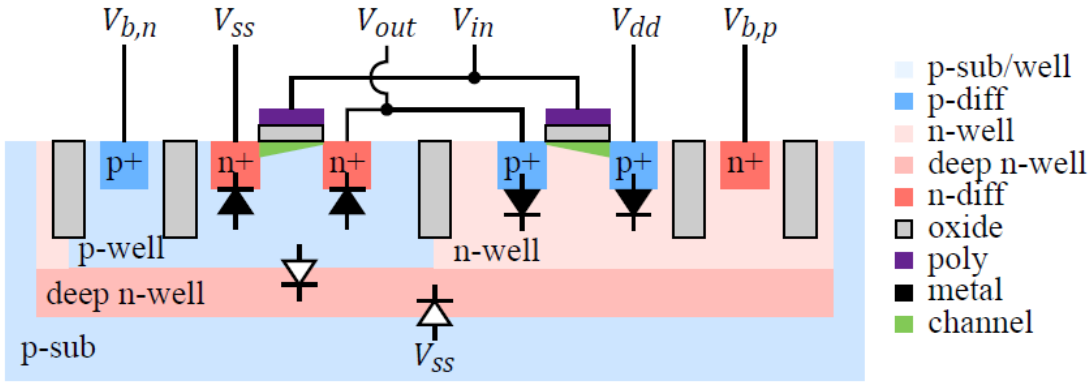
Nanometer CMOS
- Low supply
- Limited by Vth

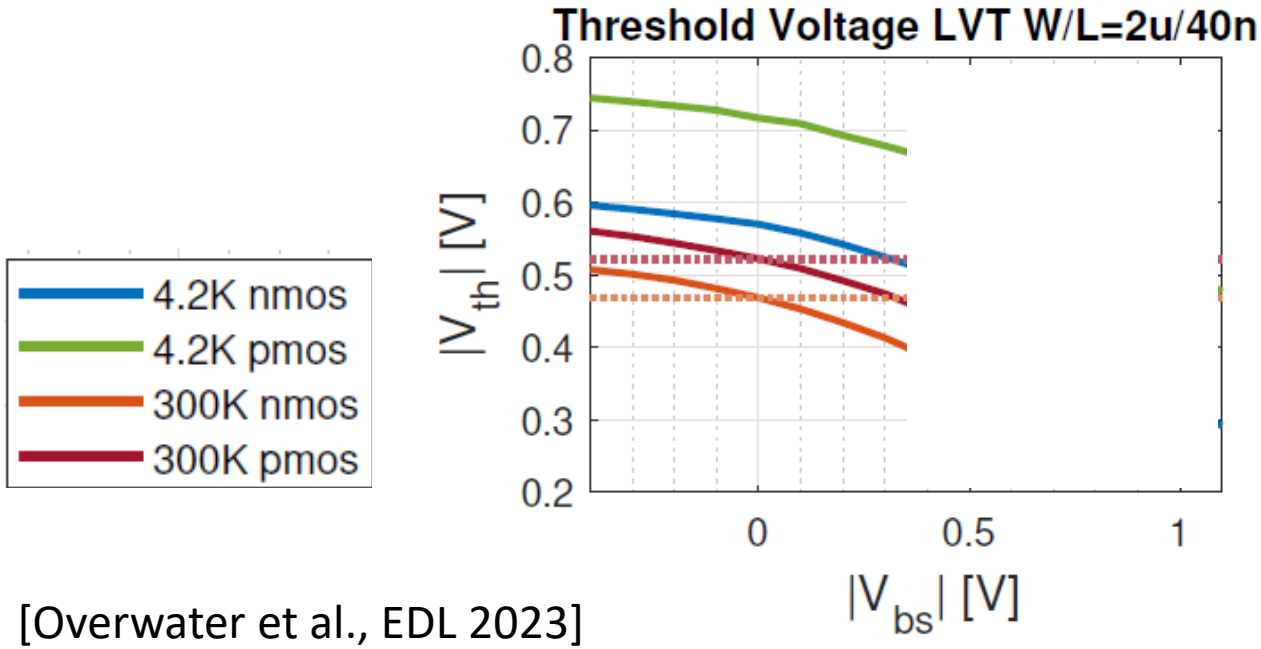
How to get a low V_{th}?

[Homulle 2019]

Tune down the threshold voltage

- Modify the process (doping)
- Low Vth (LVT) option
- Back biasing in FD-SOI
  - Specific process
  - High back-bias voltage (> 2 V) > Vdd
- Forward Body Bias in bulk CMOS?
  - Traditionally small change in Vth

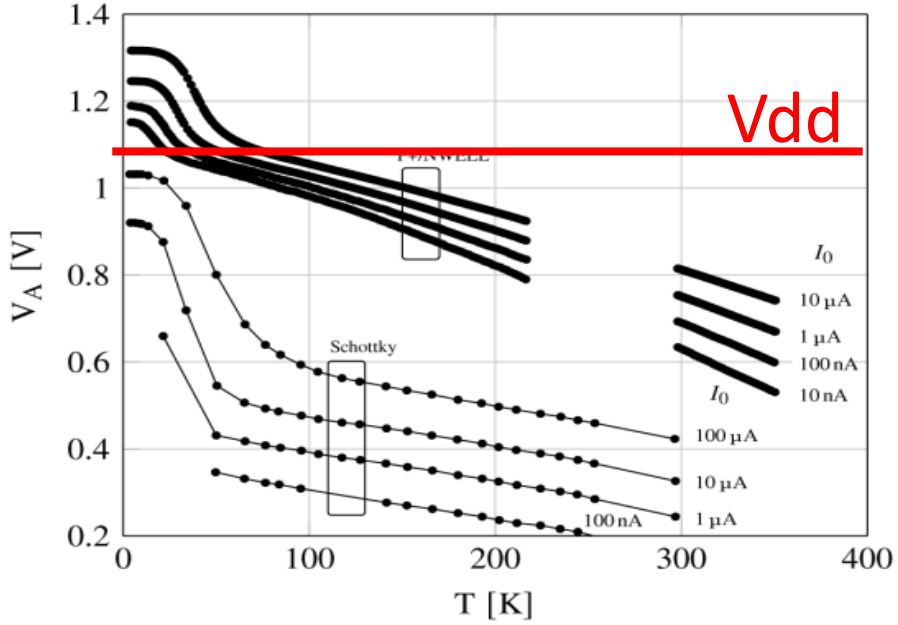




[Overwater et al., EDL 2023]

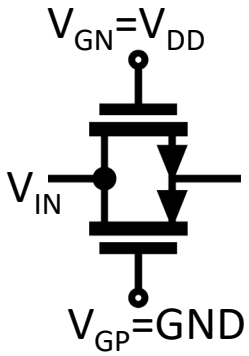
Why is it possible at 4 K?

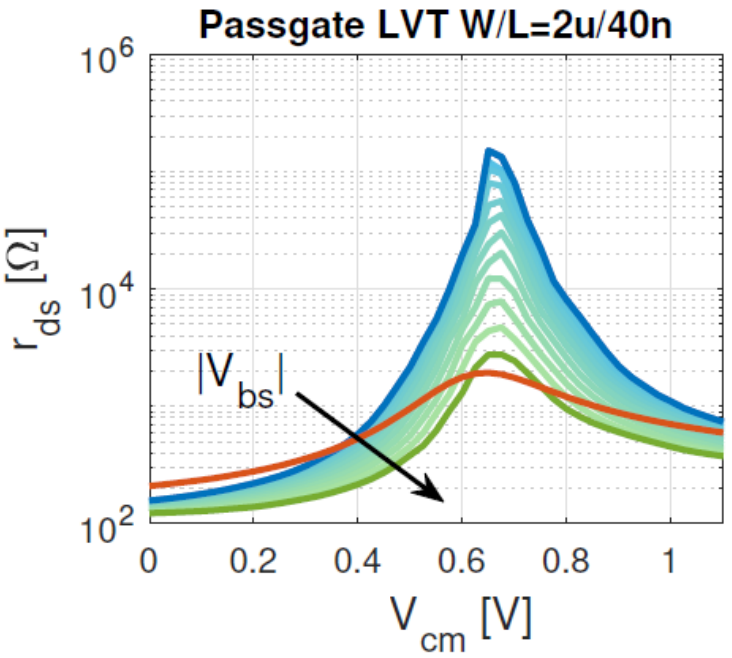
- Diodes do not turn on at 4K
- Even for Vdd



Cryogenic-Aware Forward Body Biasing (FBB)

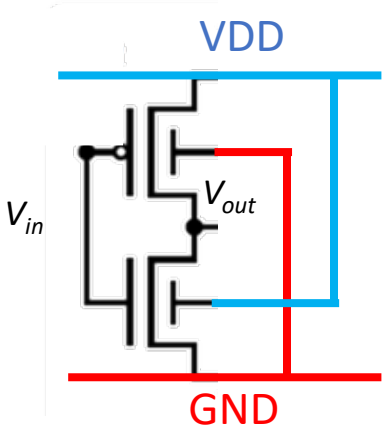
Pass-gate switches

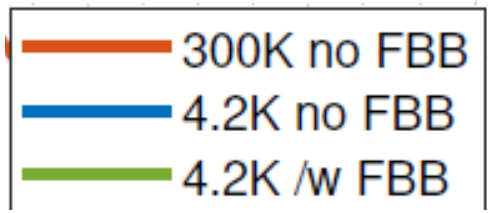


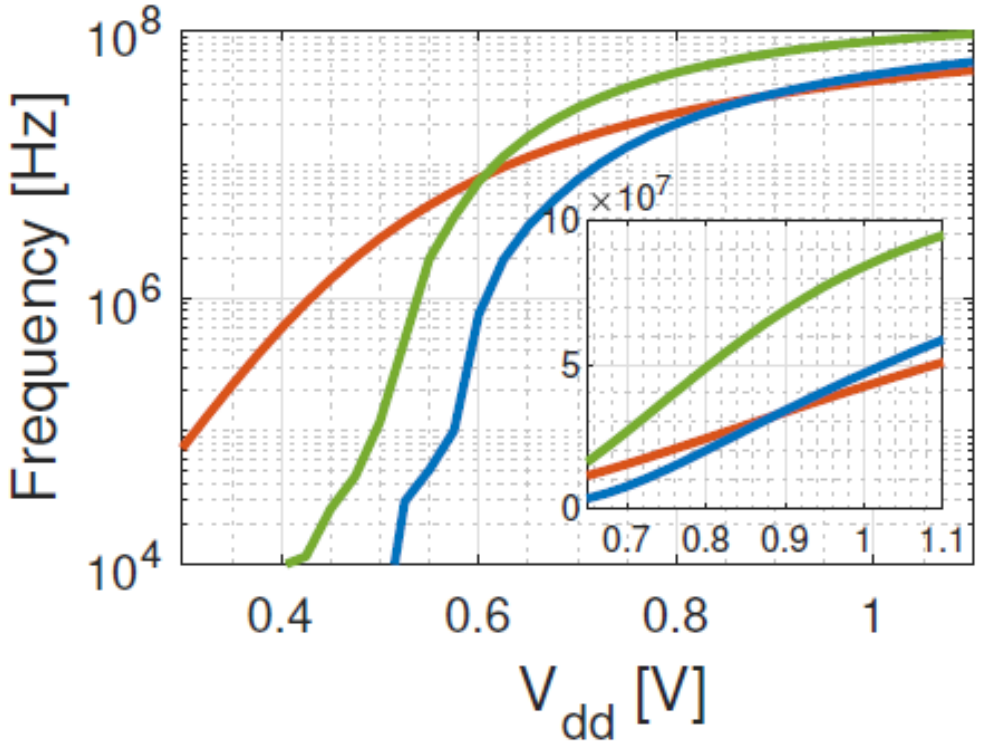


[Overwater et al., EDL 2023]

Digital logic

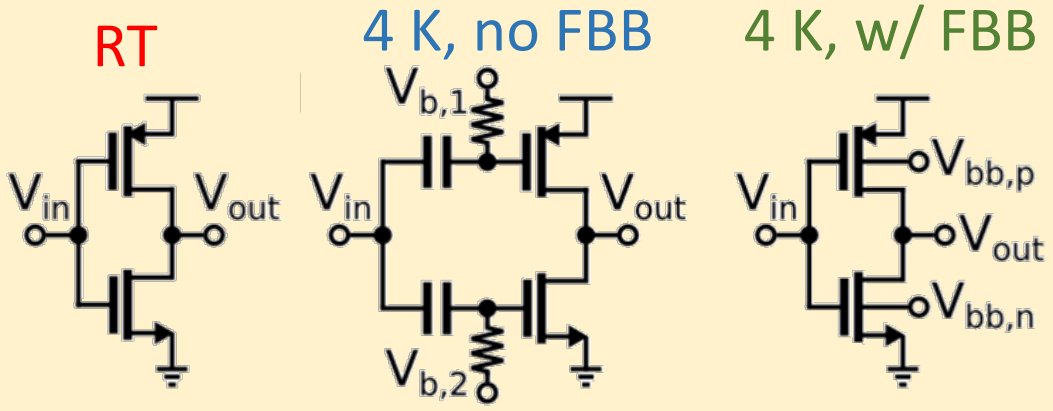




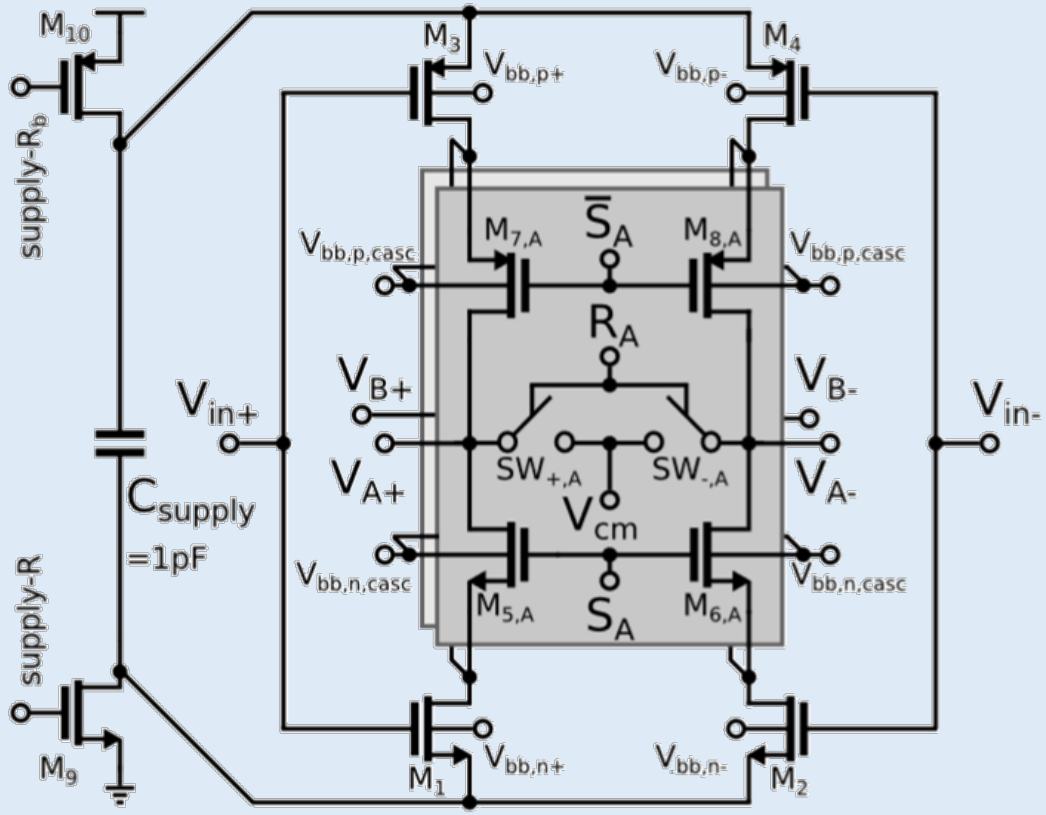


Cryogenic-Aware FBB – Analog Circuits

Efficient inverter-based amplifier



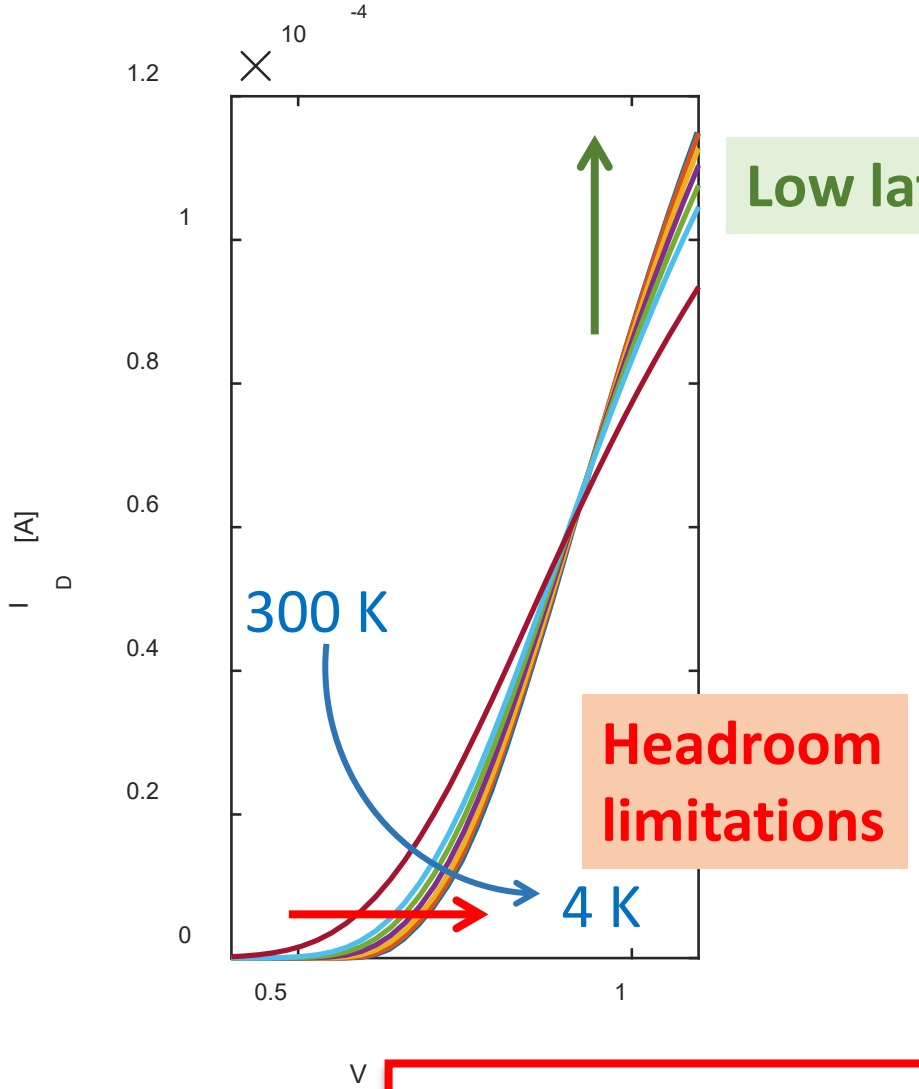
Efficient floating-inverter amplifier



- Use FBB to
  - Maximize linearity
  - Reduce switch impedance
  - Offset compensation
- **Achieve 6.1 ENOB @ 1 Gsa/s driving SAR ADC**

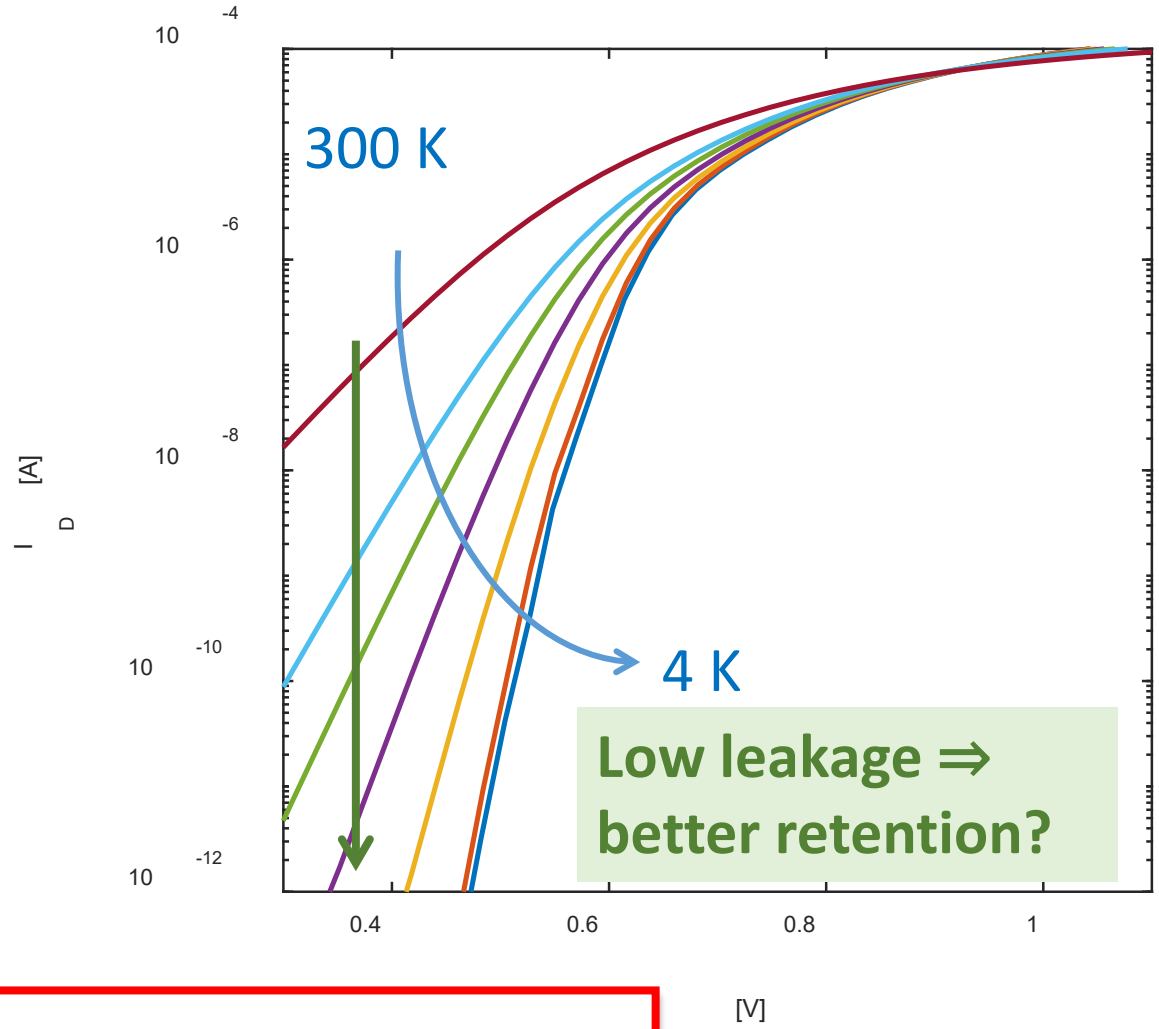
[Kiene et al., TCAS 2023]

… and the memories?



Low latency

Headroom limitations



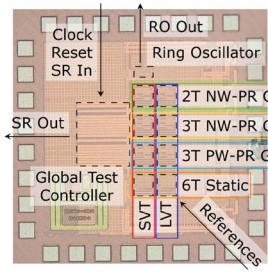
Low leakage ⇒ better retention?

Best memory design for cryo-CMOS?

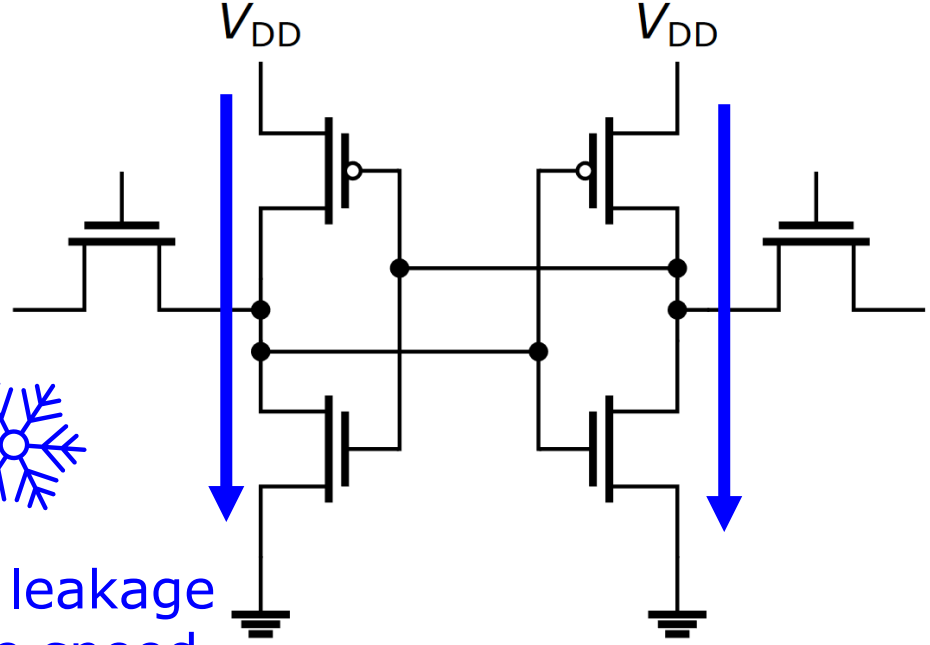
TSMC 40-nm CMOS

Cryo-CMOS memories

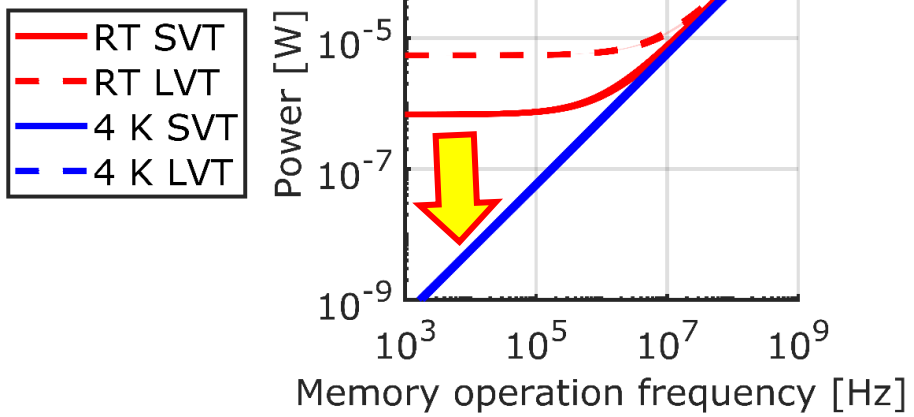
40-nm CMOS



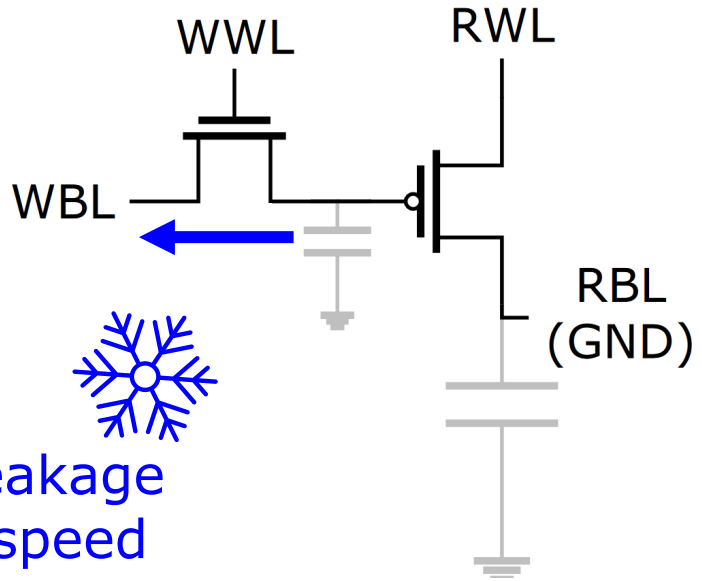
Static memories (6T SRAM)



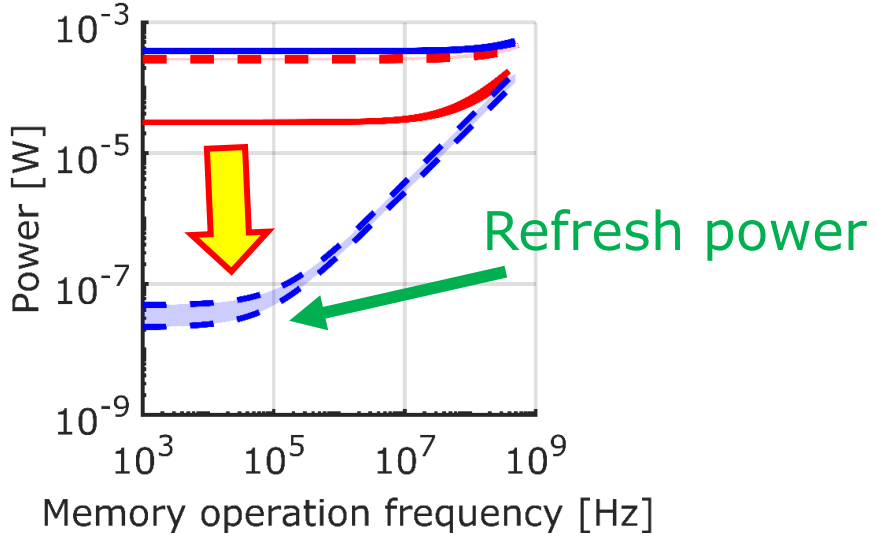
Less leakage
More speed



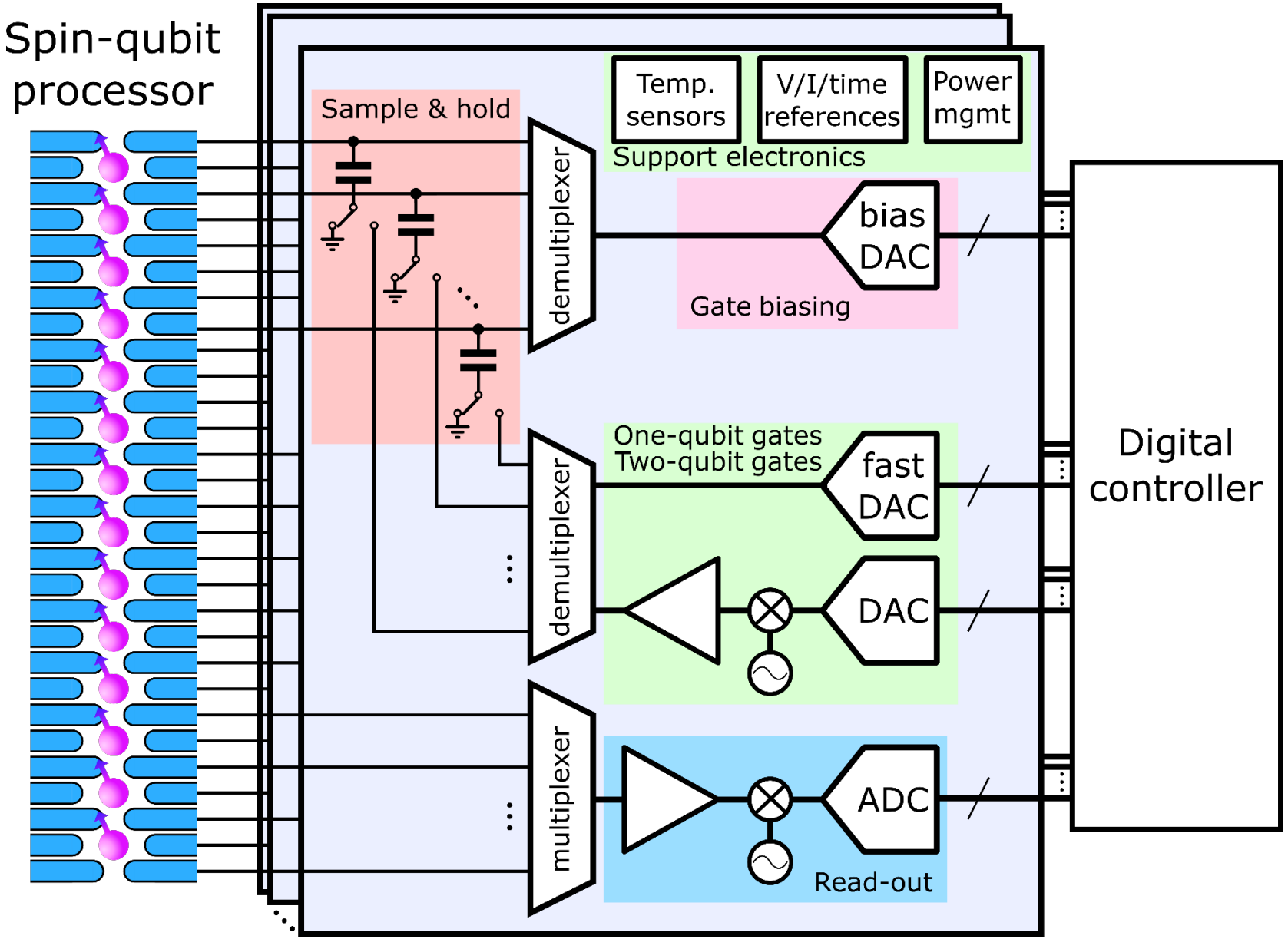
Dynamic memories (2T DRAM)



Less leakage
More speed



Towards a scalable spin-qubit QC



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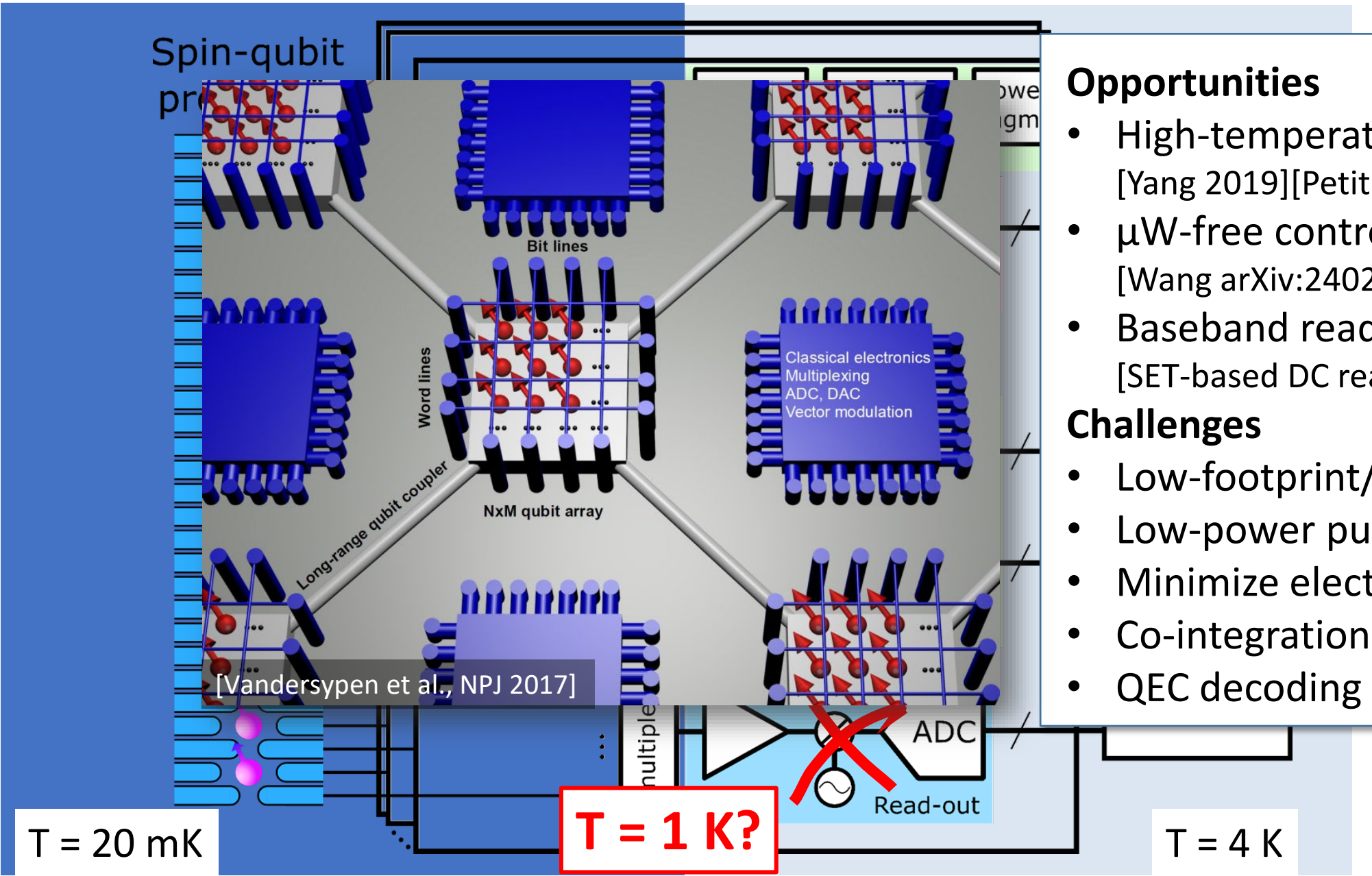


Opportunities

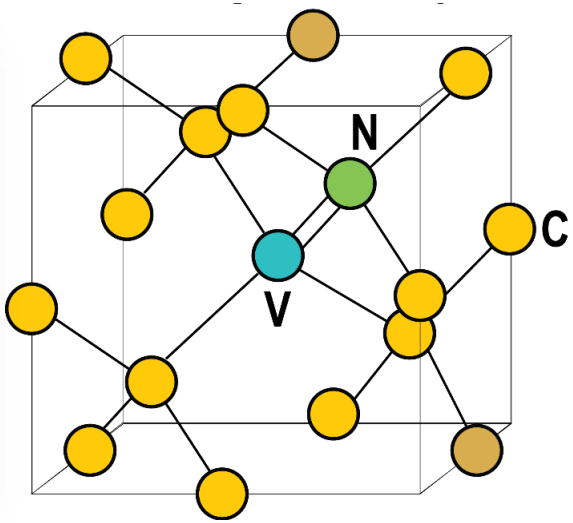
- High-temperature operation
  [Yang 2019][Petit 2020][Huang 2024]
- µW-free control
  [Wang arXiv:2402.18382]
- Baseband readout
  [SET-based DC readout]

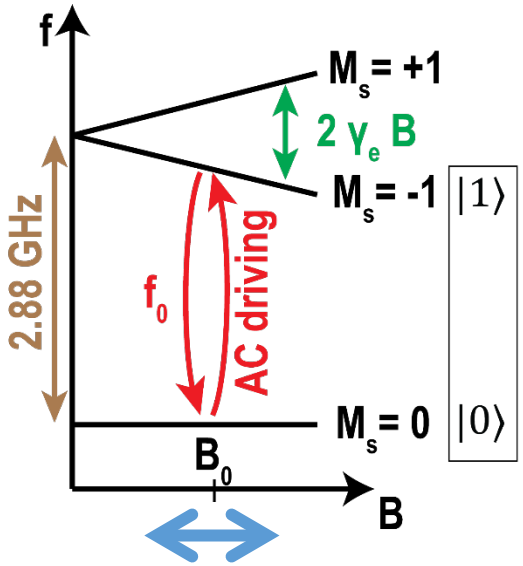
Challenges

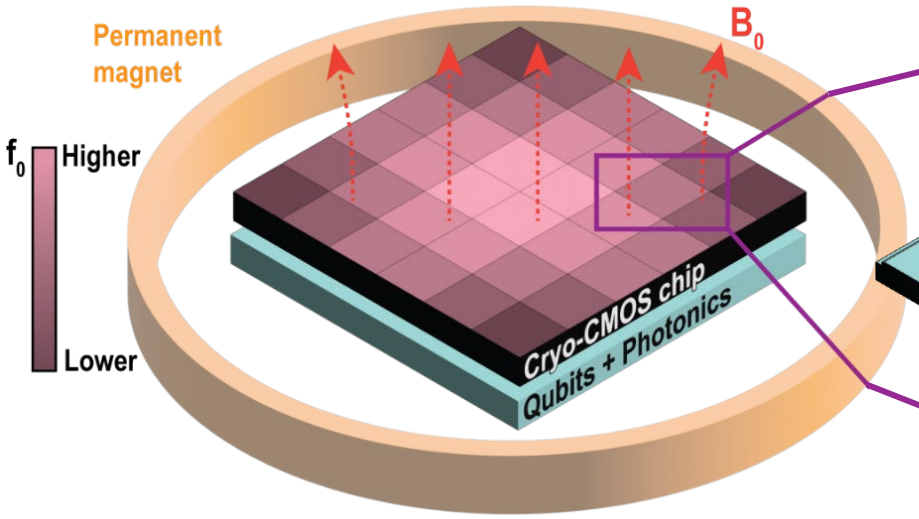
- Low-footprint/low-noise readout
- Low-power pulsing
- Minimize electrical crosstalk
- Co-integration
- QEC decoding

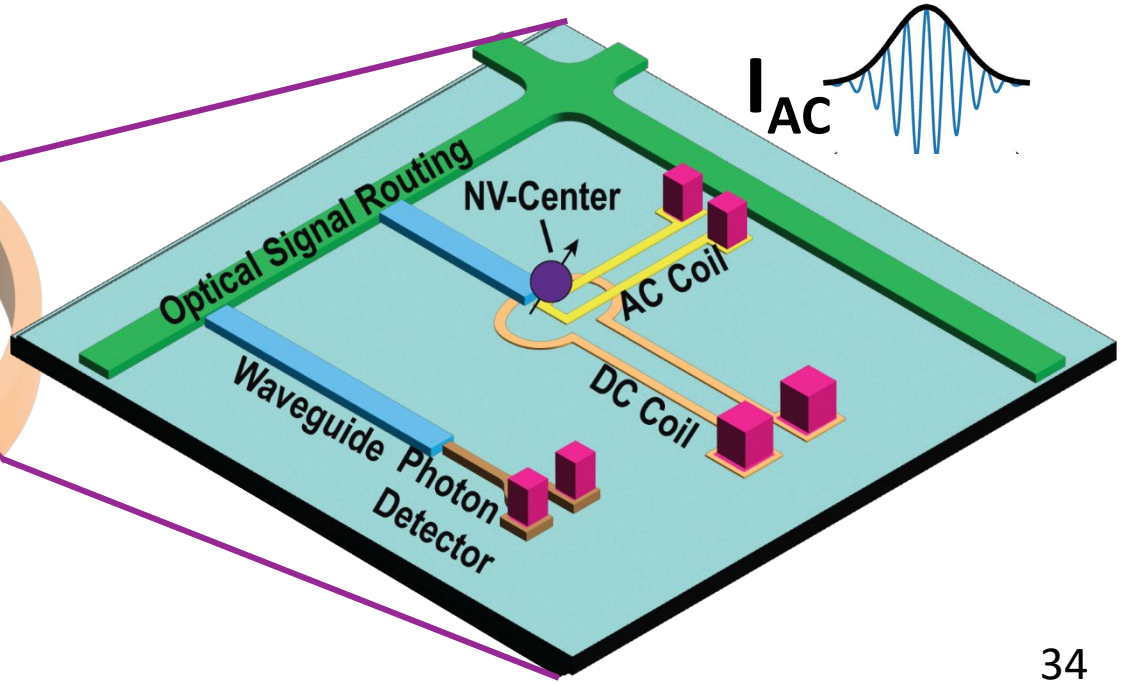
Diamond qubits (color-center qubits)

- High fidelity
- High temperature (>1 K)
- Remote entanglement (> 1 km)
- Electrical and optical control
- Hybrid co-integration ⇒ Poor coil-qubit coupling ⇒ high currents





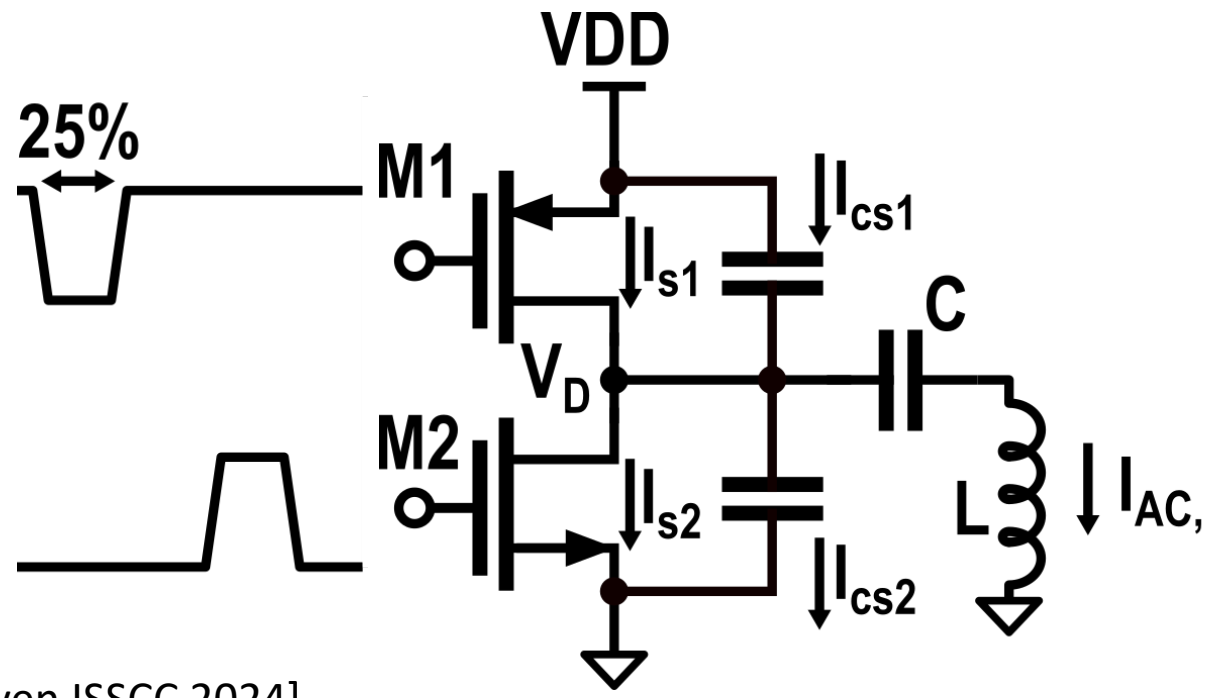


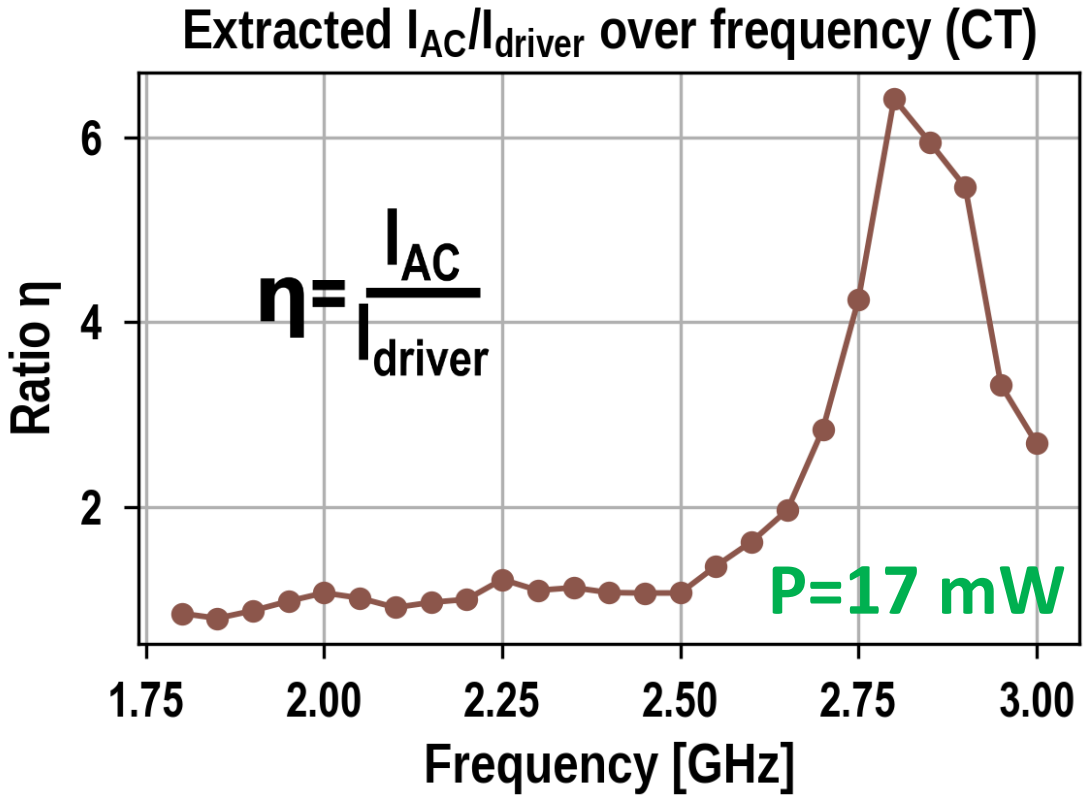


[Enthoven arXiv:2403.09526]

AC driver for diamond qubits

- **Challenge:** Large current (>10 mA_{pk} @ 2.7 GHz) but low power
- **Solution:** Class DE switch-mode driver
  - Series resonance limits max V-swing
  - No crowbar currents
  - Zero-voltage-switching

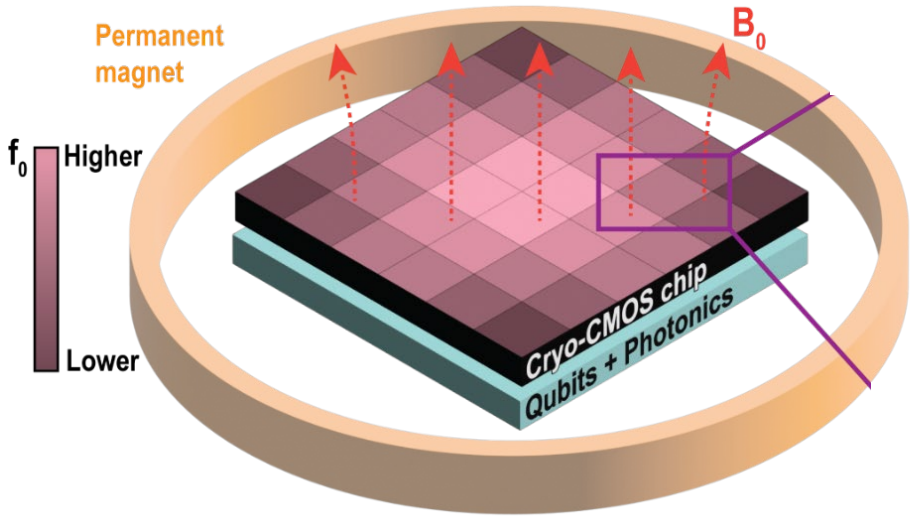




[Enthoven ISSCC 2024]

DC driver for diamond qubits

- **Inhomogeneous field to be corrected locally**
- **Challenges**
  - Large current (>12 mA)
  - Fine resolution (<8µA step)
  - Low power (< 1 mW)



[Enthoven ISSCC 2024]

DC driver for diamond qubits

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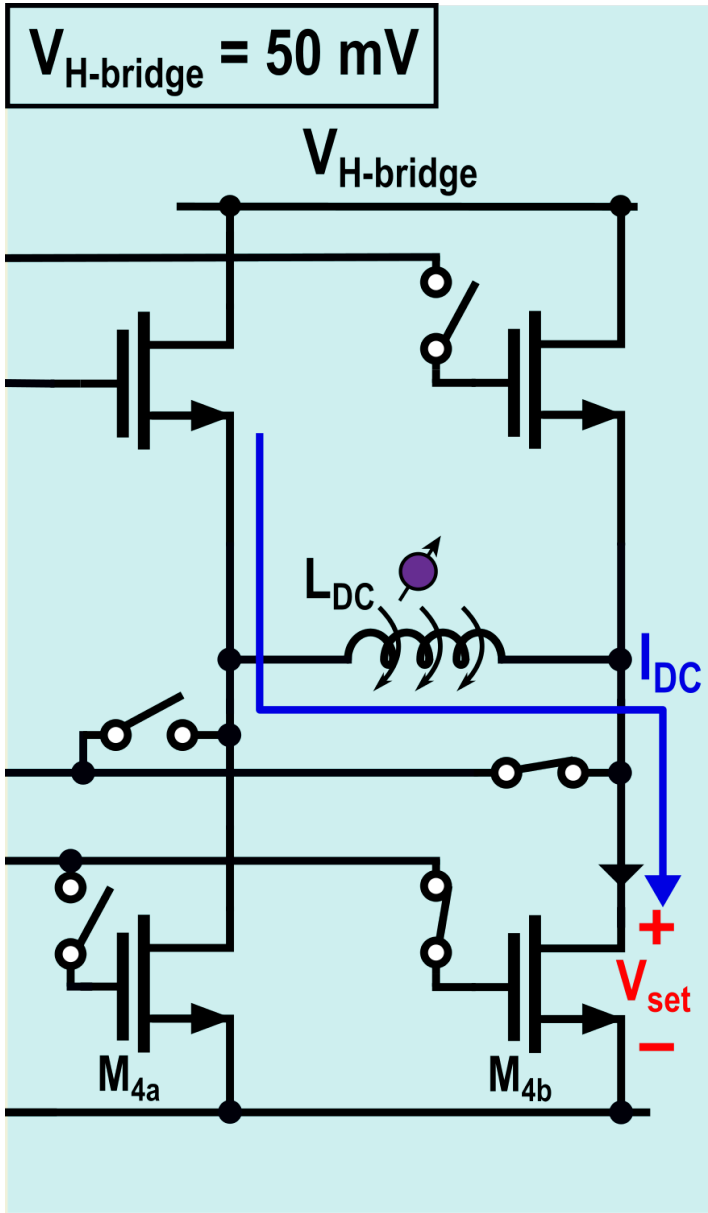
- **Challenges**
  - Large current (>12 mA)
  - Fine resolution (<8µA step)
  - Low power (< 1 mW)
- **Solution:** triode-based H-bridge
  - **Low V-drop ⇒ poor supply rejection**



[Enthoven ISSCC 2024]

DC driver for diamond qubits

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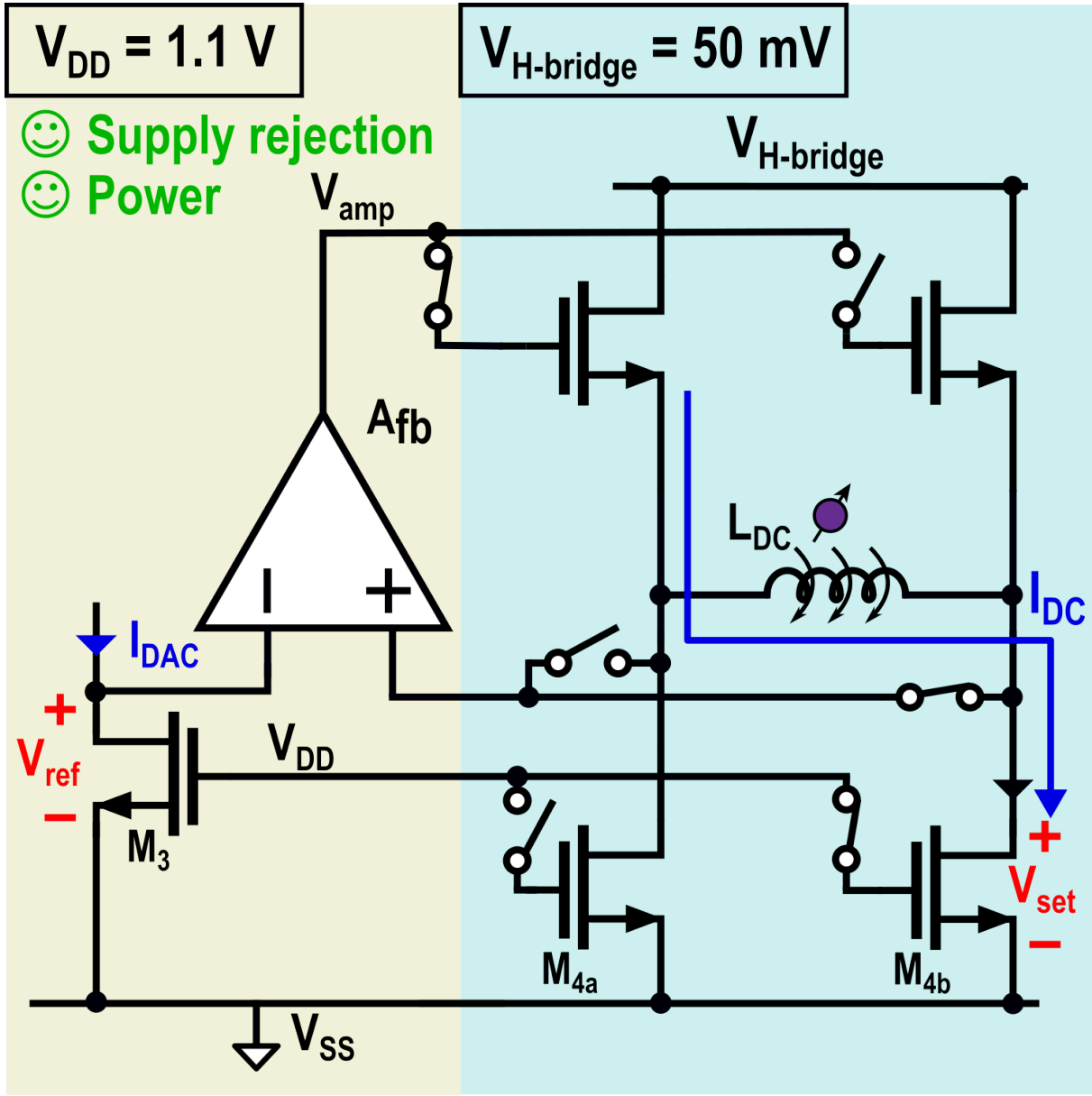
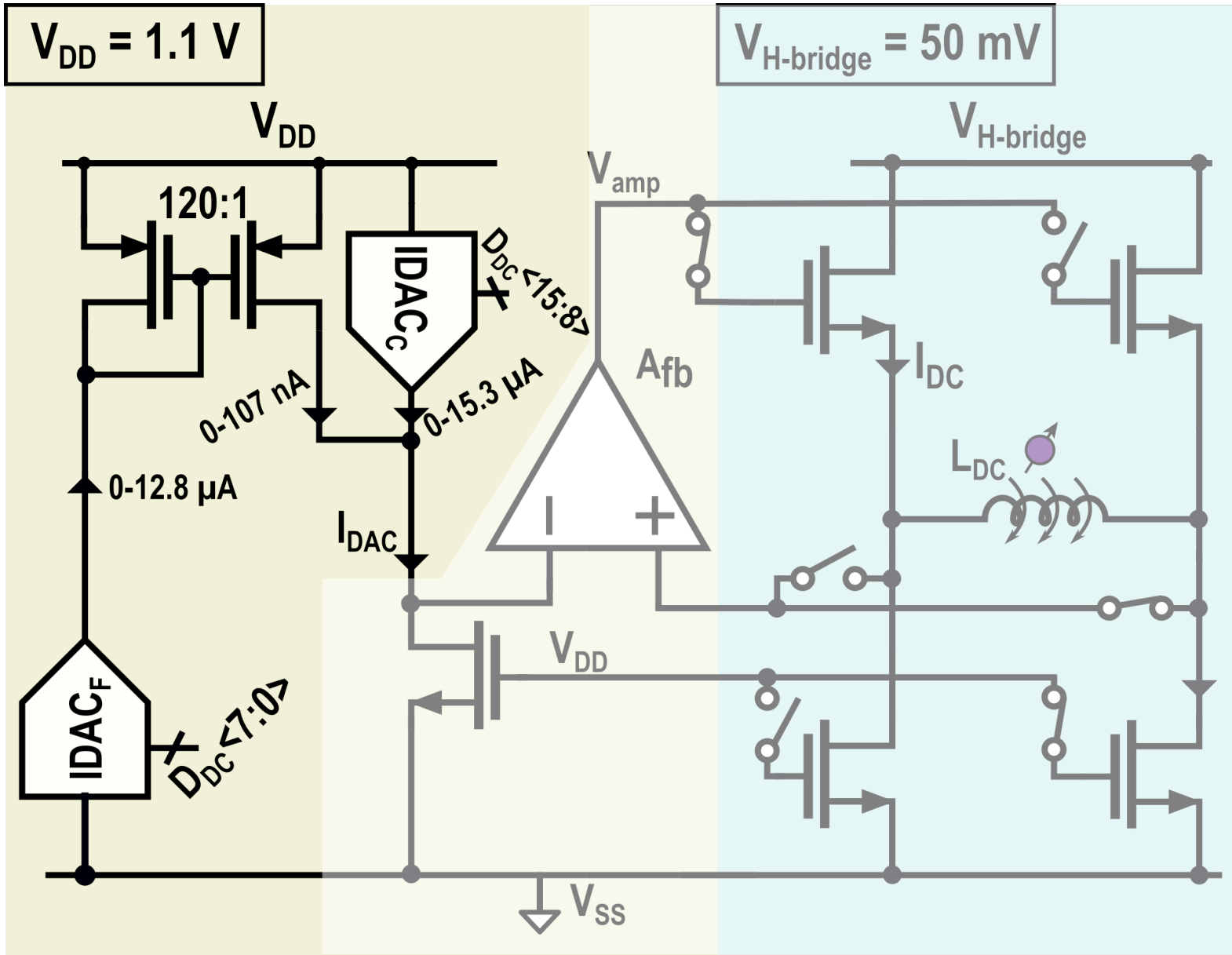
- **Solution:** triode-based H-bridge
  - Low V-drop
  - **Loop-regulated PSRR**



[Enthoven ISSCC 2024]

DC driver for diamond qubits

- **Inhomogeneous field to be corrected locally**
- **Challenges**
  - Large current (>12 mA)
  - Fine resolution (<8µA step)
  - Low power (< 1 mW)
- **Solution:** triode-based H-bridge
  - Low V-drop
  - Loop-regulated PSRR
  - **Fine/coarse DAC**



[Enthoven ISSCC 2024]

DC driver for diamond qubits

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  - Large current (>12 mA)
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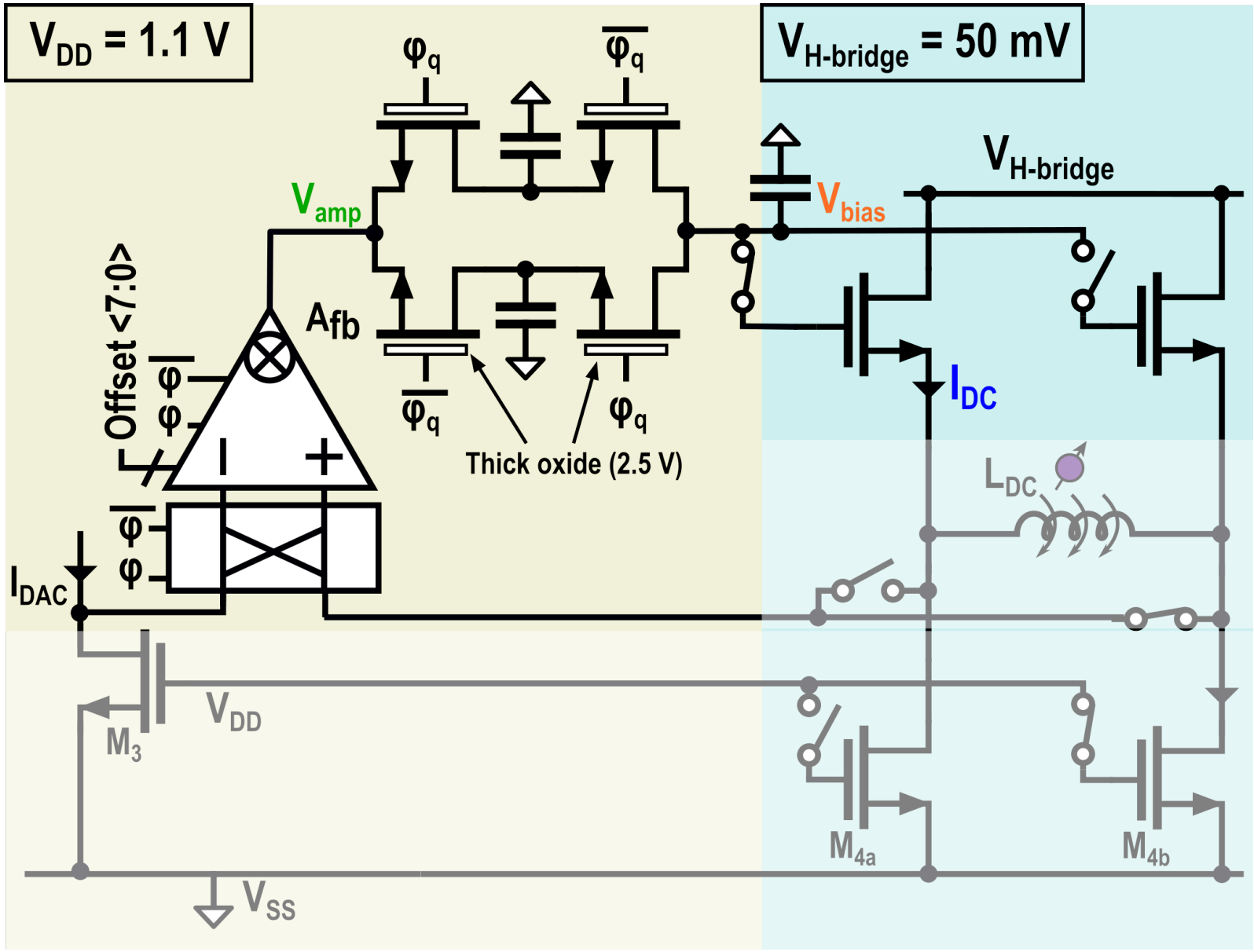
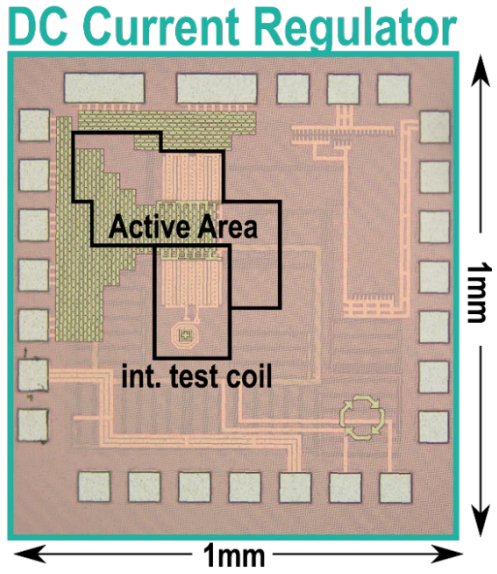
- **Solution:** triode-based H-bridge
  - Low V-drop
  - Loop-regulated PSRR
  - Fine/coarse DAC
  - **Chopping/trimming**

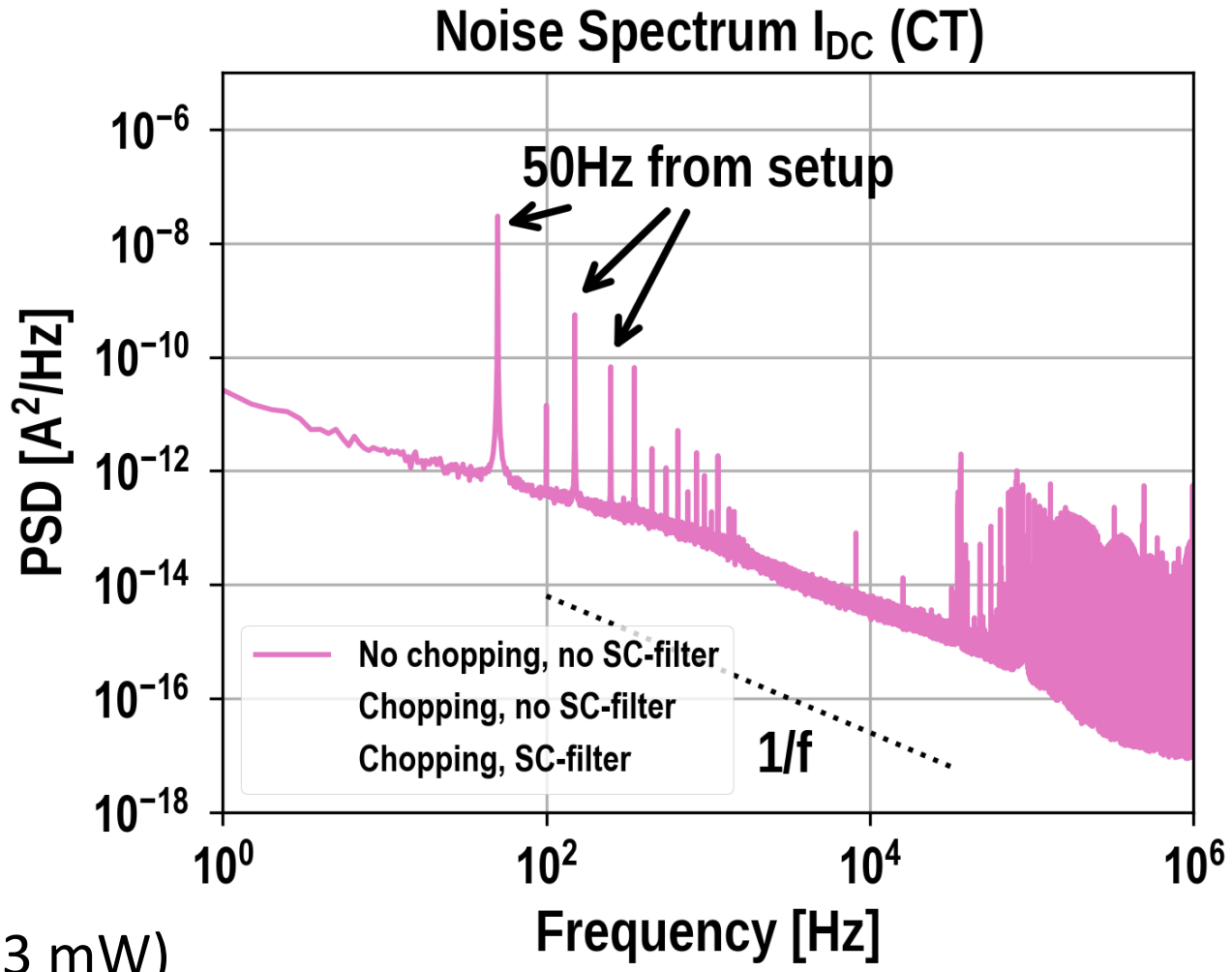


[Enthoven ISSCC 2024]

DC driver for diamond qubits



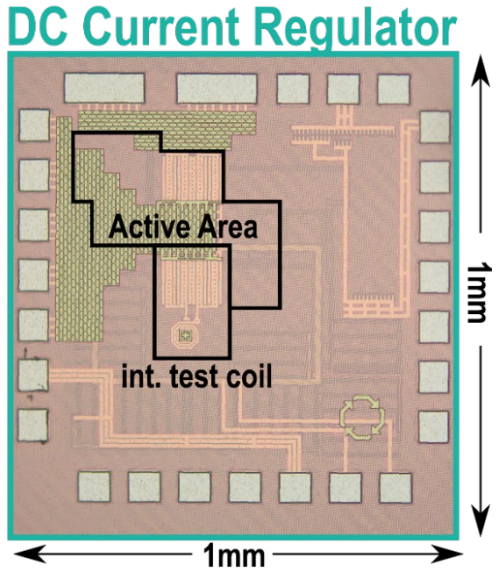
Fabricated in
40-nm CMOS



- **Results**
  - ±12mA with 50-mV supply
  - Regulation better than 18 µA/V
  - P=0.9 mW (P_{bridge}=0.6 mw, P_{VDD}=0.3 mW)

[Enthoven ISSCC 2024]

DC driver for diamond qubits



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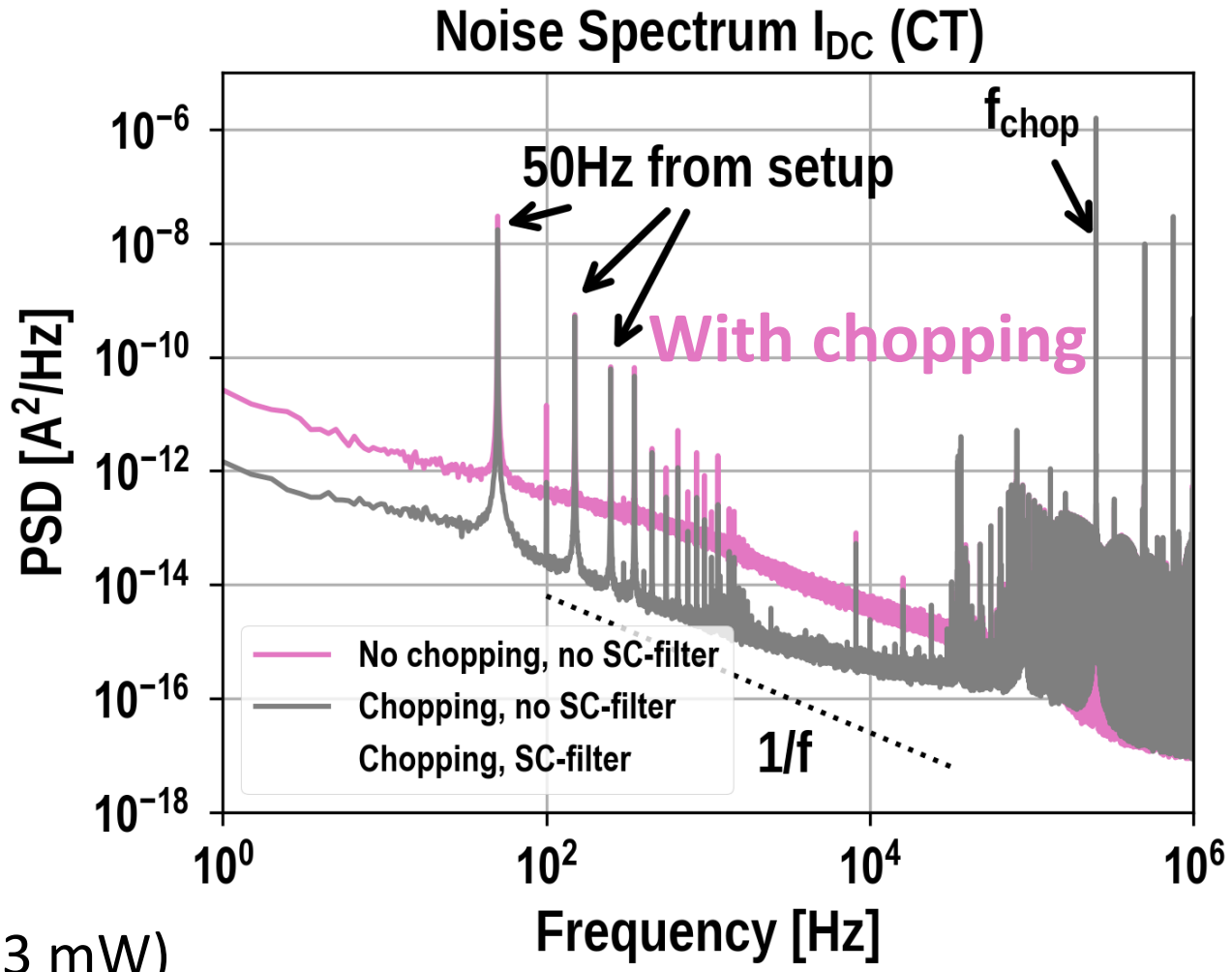

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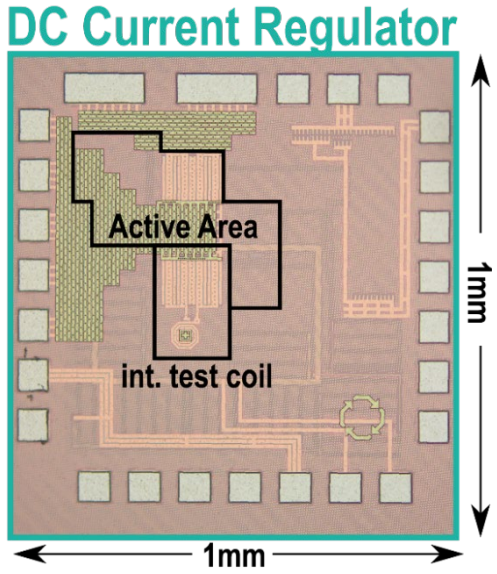

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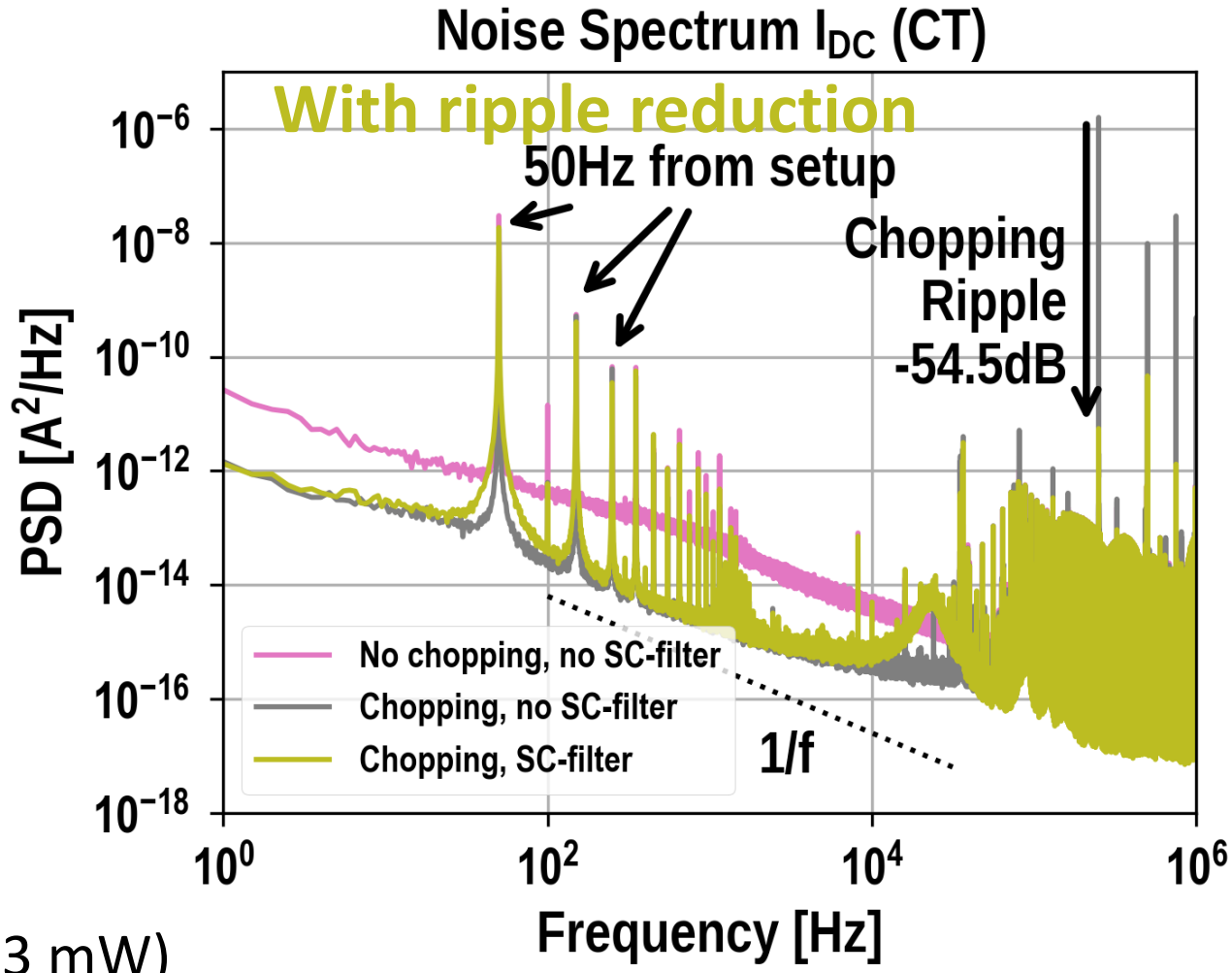

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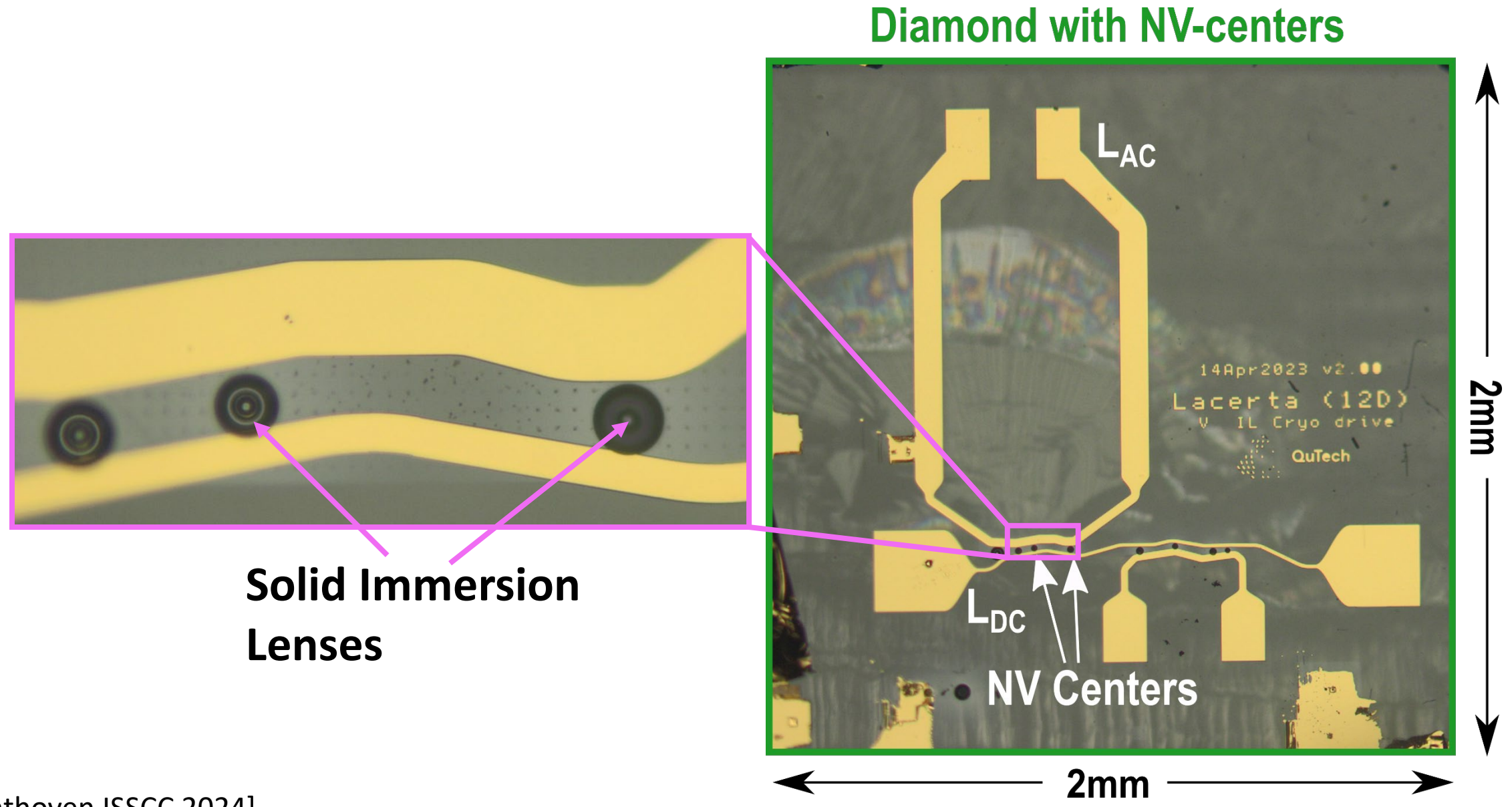
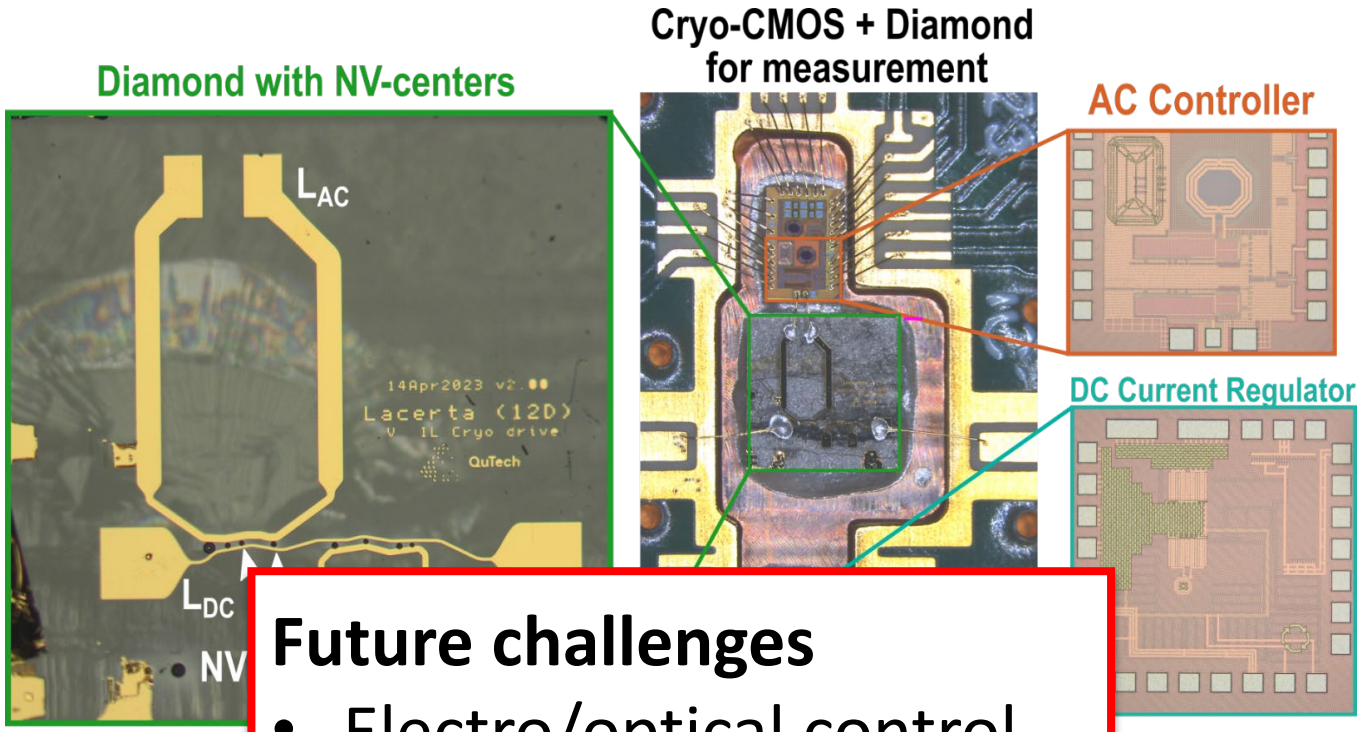
[Enthoven ISSCC 2024]

Qubit sample



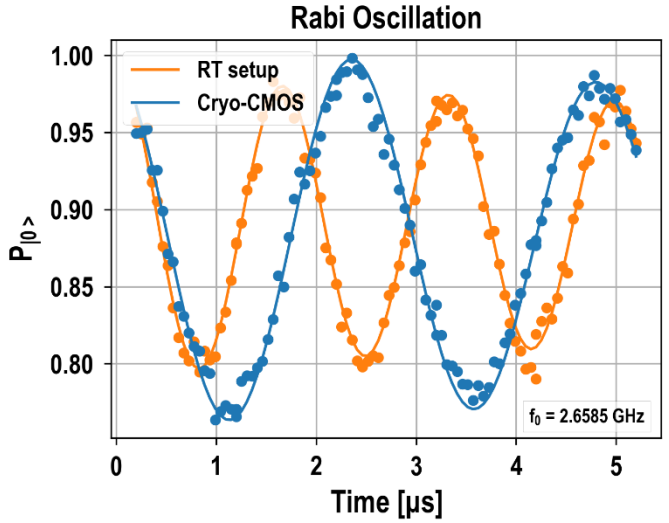
[Enthoven ISSCC 2024]

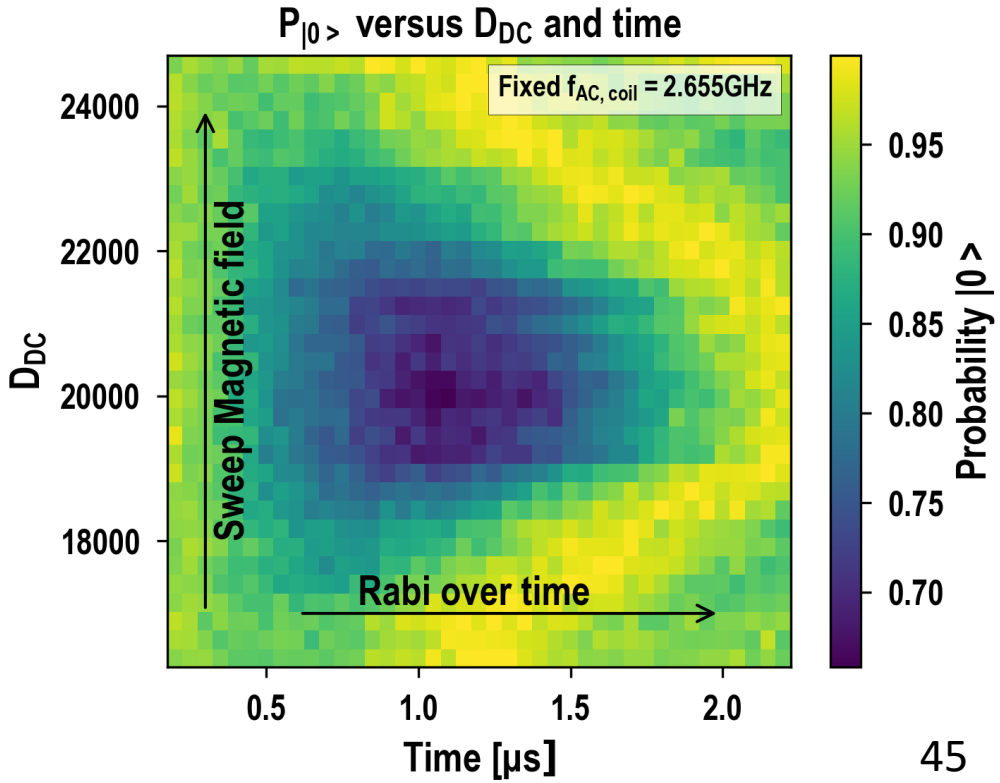
Cryo-CMOS for diamond qubits



Future challenges

- Electro/optical control
- Hybrid co-integration
- Thermal management





[Enthoven ISSCC 2024]

FUJITSU

Take-aways

- Spin qubit + cryo-CMOS = promising for scalable quantum computers
- Spin qubits in semiconductors
  - High-temperature operation + pulse-based control
  - *Monolithic integration!*
  - **Challenges: efficient cryo-CMOS pulsing; low-noise readout**
- Spin qubits in diamonds
  - High-temperature operation + remote entanglement
  - *Modular architecture with moderate footprint!*
  - **Challenges: optical control; co-integration; thermal management**
- Digital back-end
  - Decoding, control, high-speed data communication, …
- Cryo-CMOS as enabler of large-scale QCs…

  … but ample space (and need!) for innovation and research!

Acknowledgments

Looking for a PhD or postdoc position?
Contact me at f.sebastiano@tudelft.nl

M.Babaie, L.Vandersypen, M.Veldhorst,
G. Scappucci, T. Taminiau & their teams

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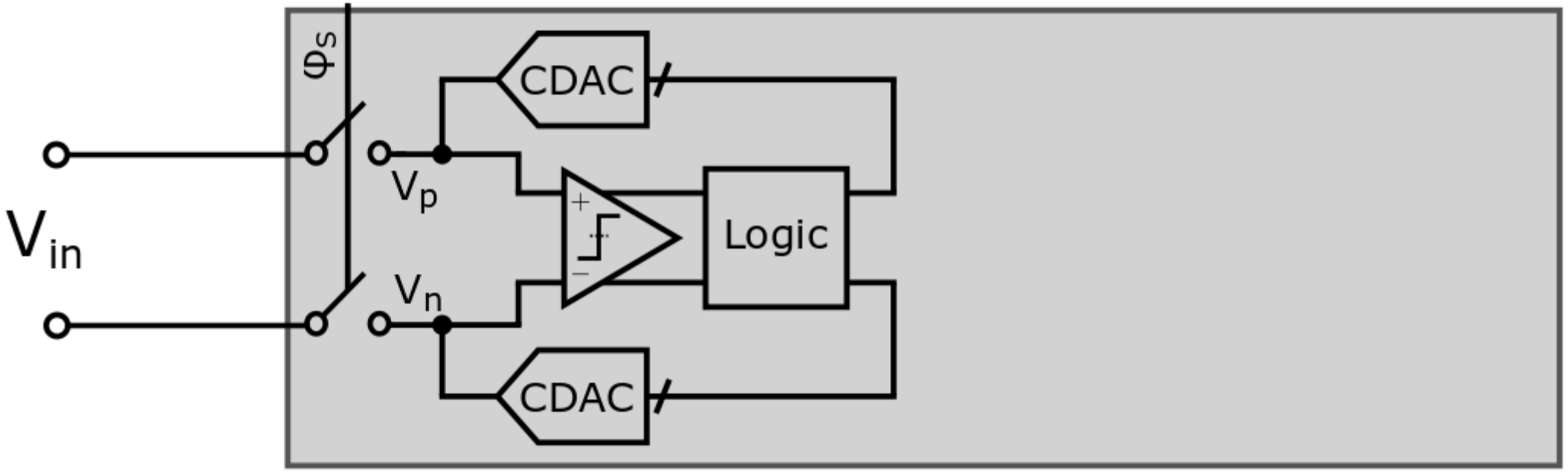
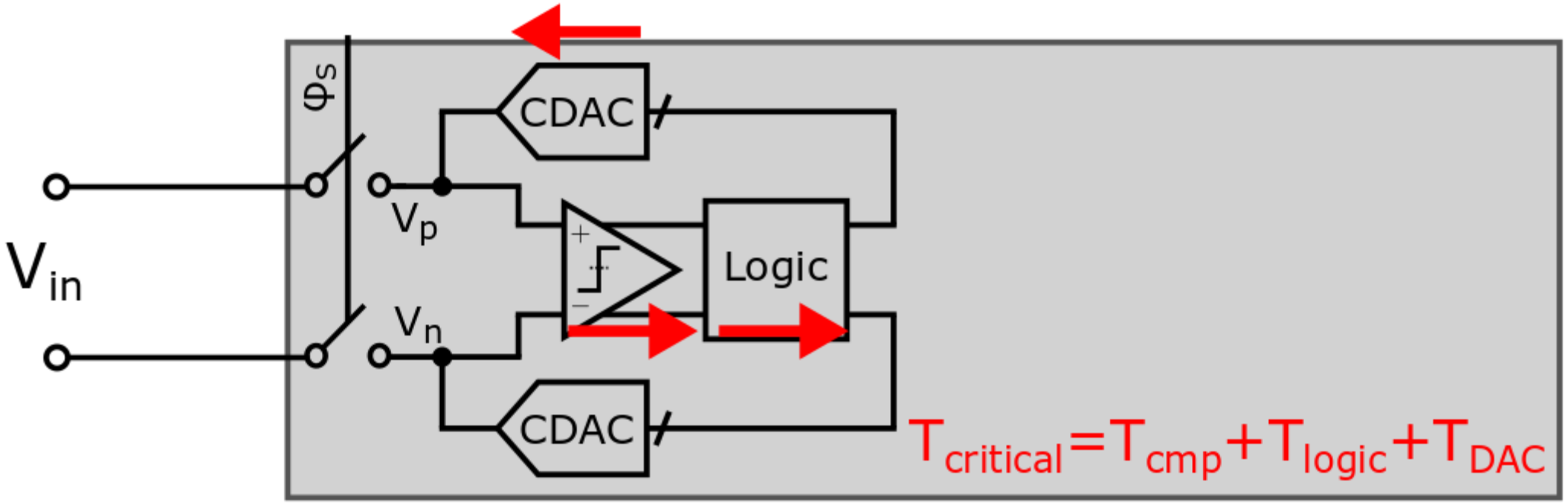
ADC architecture: SAR

- Power efficient
- Mostly digital operation



ADC architecture: loop-unrolled

- Speed of SAR limited by critical loop!

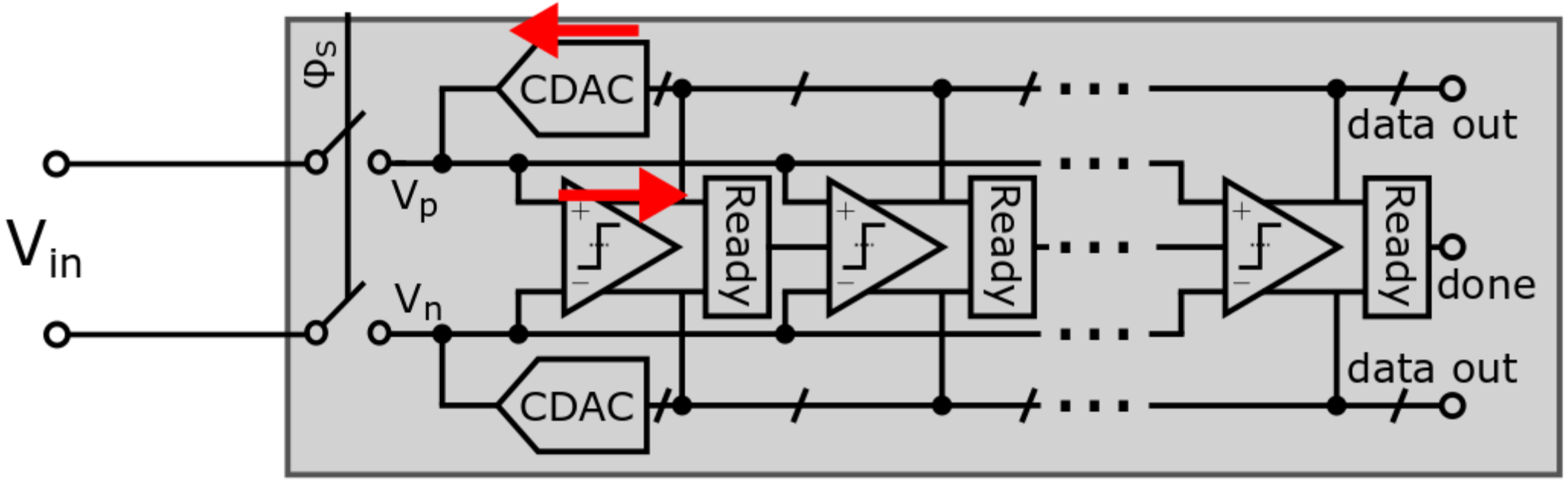


ADC architecture: loop-unrolled

- Unrolled loop speeds up conversion
- Inherently asynchronous
- Problem: Comparator offsets cause distortion

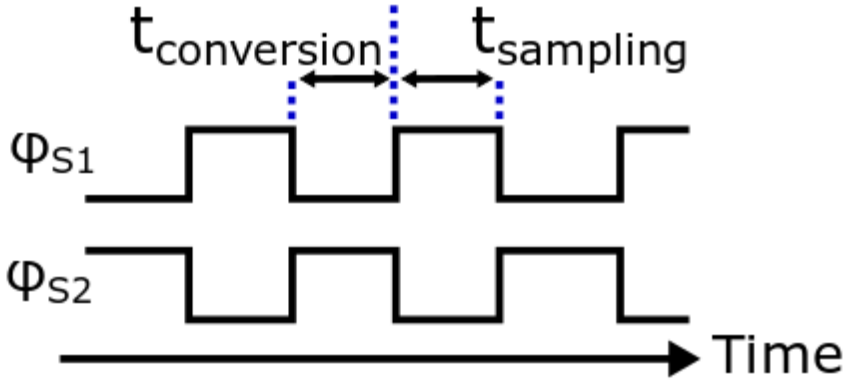
$T_{critical} = T_{cmp} + T_{DAC}$

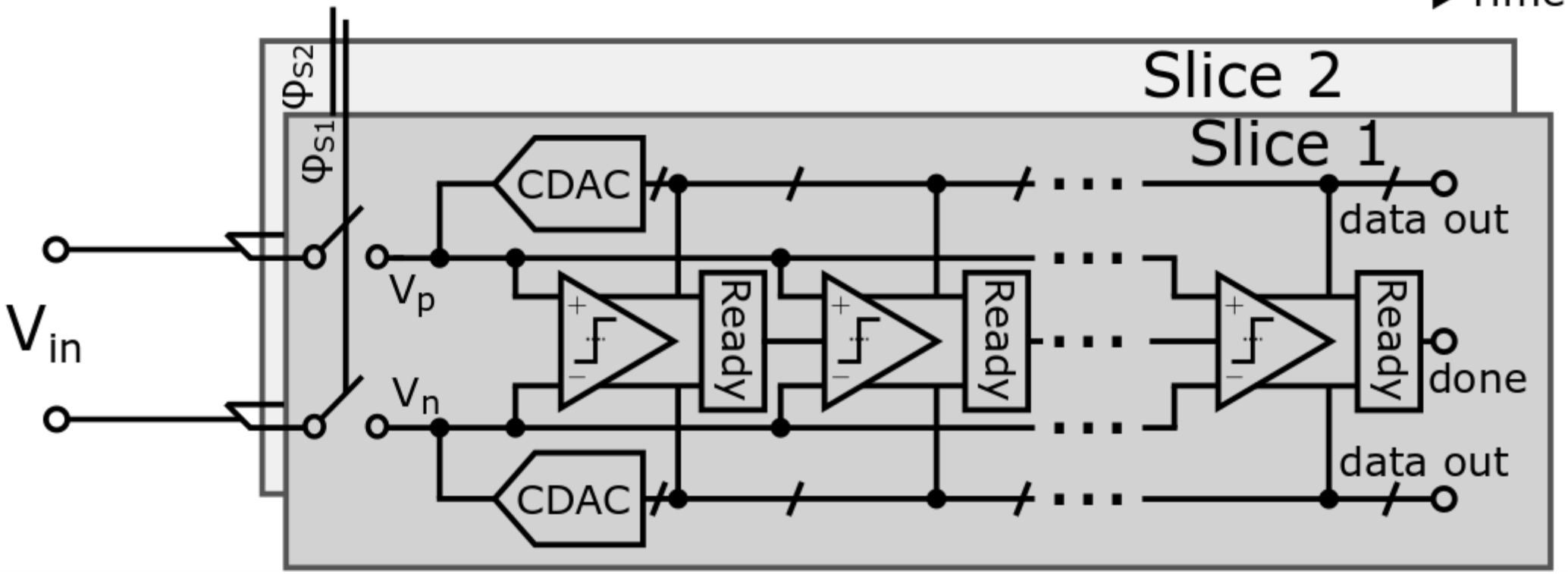
[Jiang, 2012]



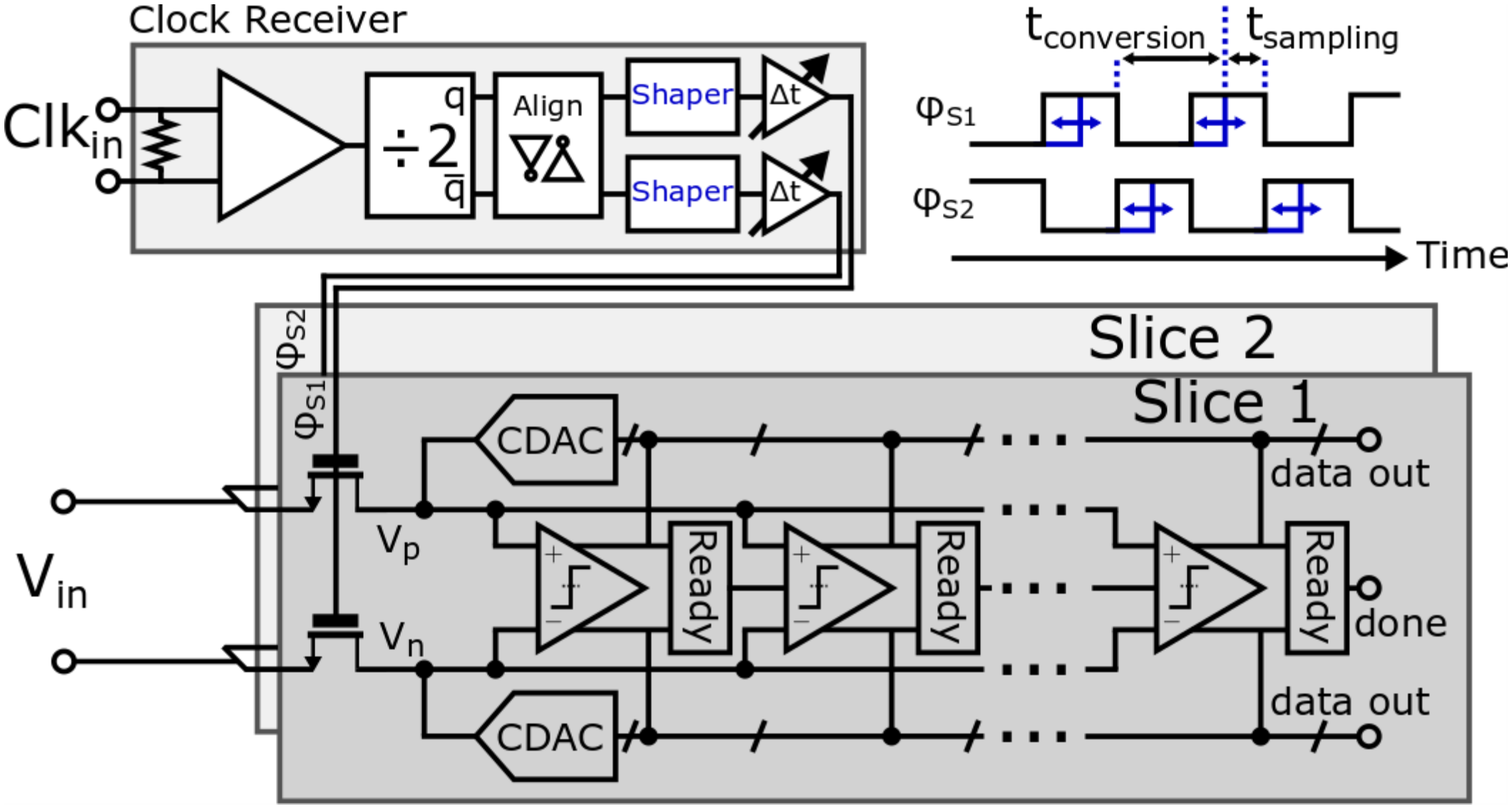
ADC architecture: time interleaved

- Speedup by factor of two
- Switch more linear than necessary

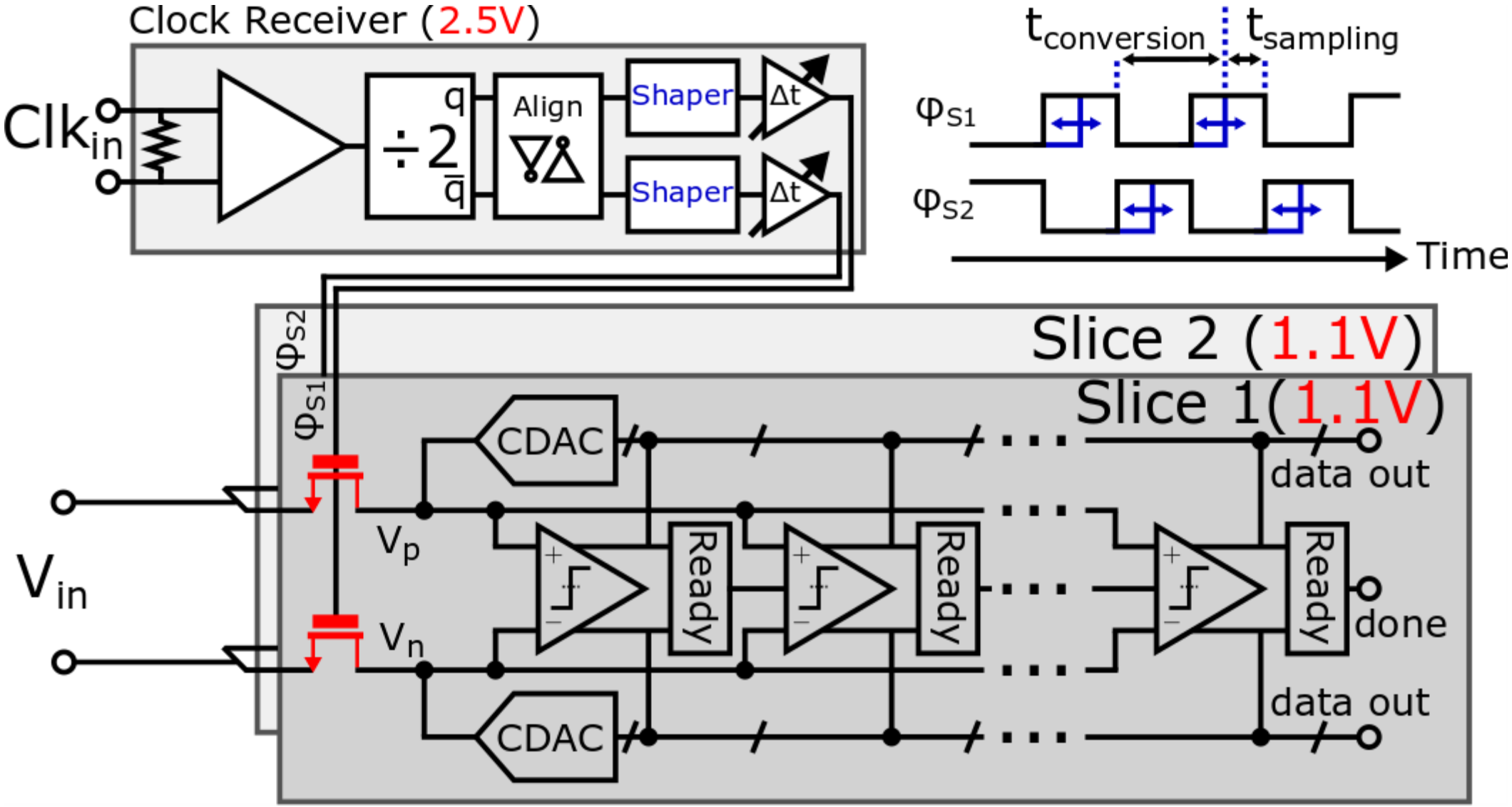




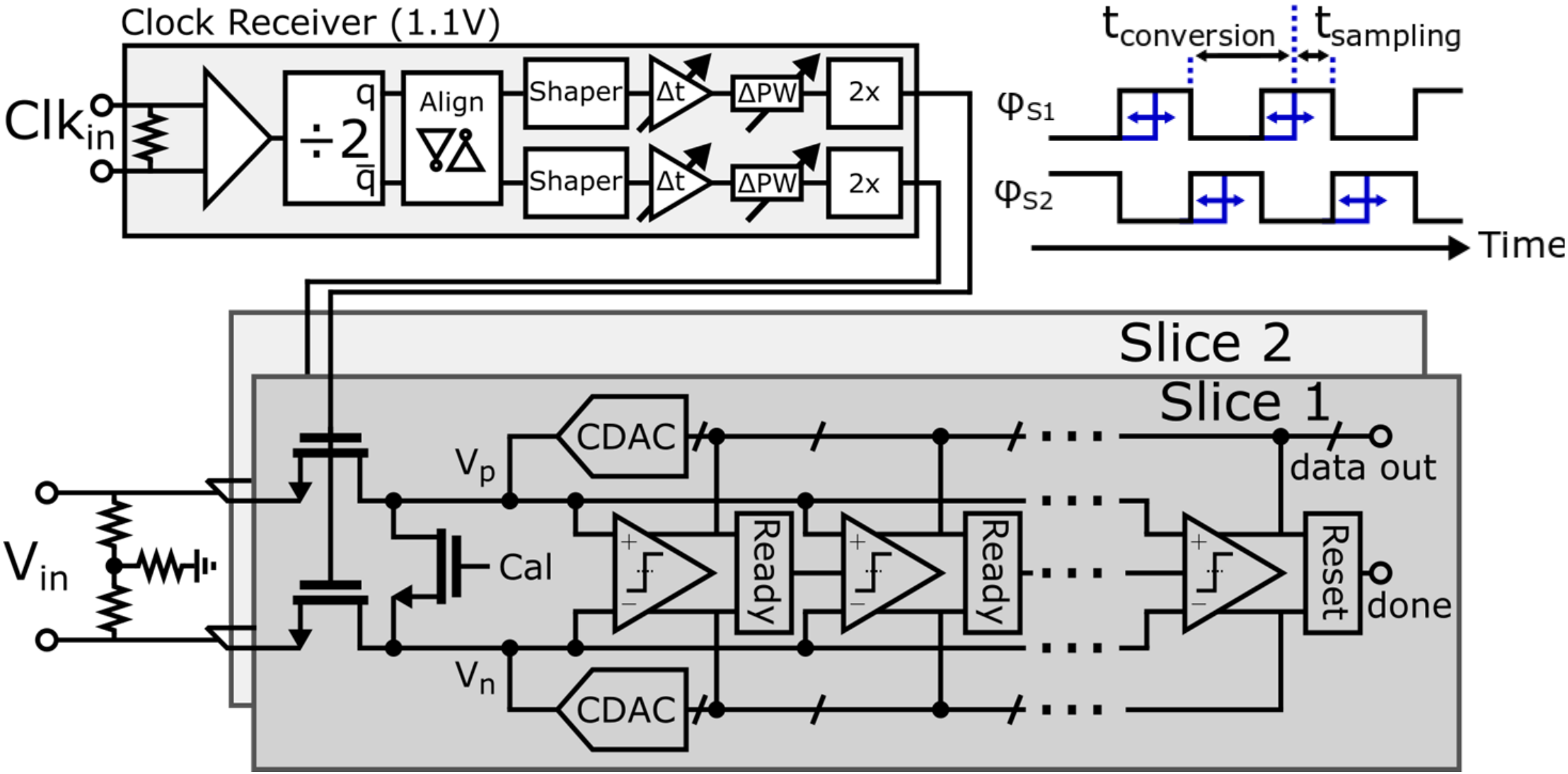
ADC architecture: frontend



ADC architecture: frontend



ADC architecture: frontend

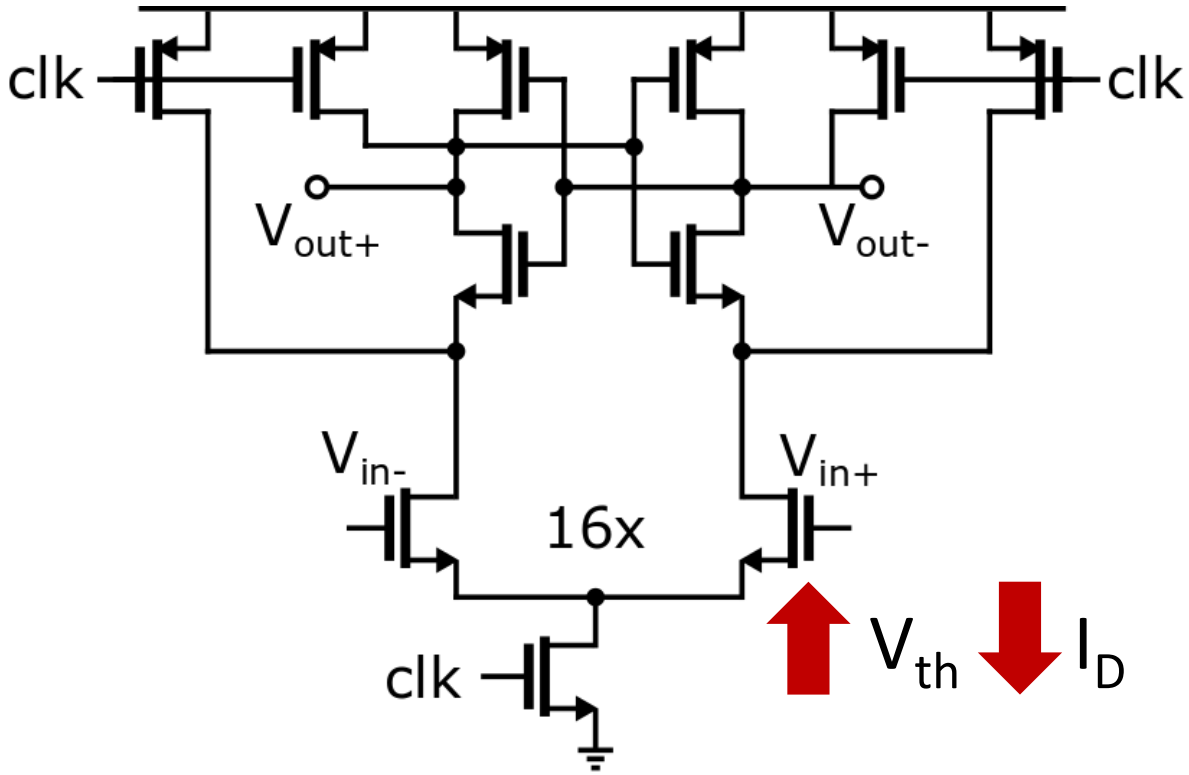


[ISSCC 2021, ESSCIRC 2022]

Comparator design

Challenge: V_{th} increase

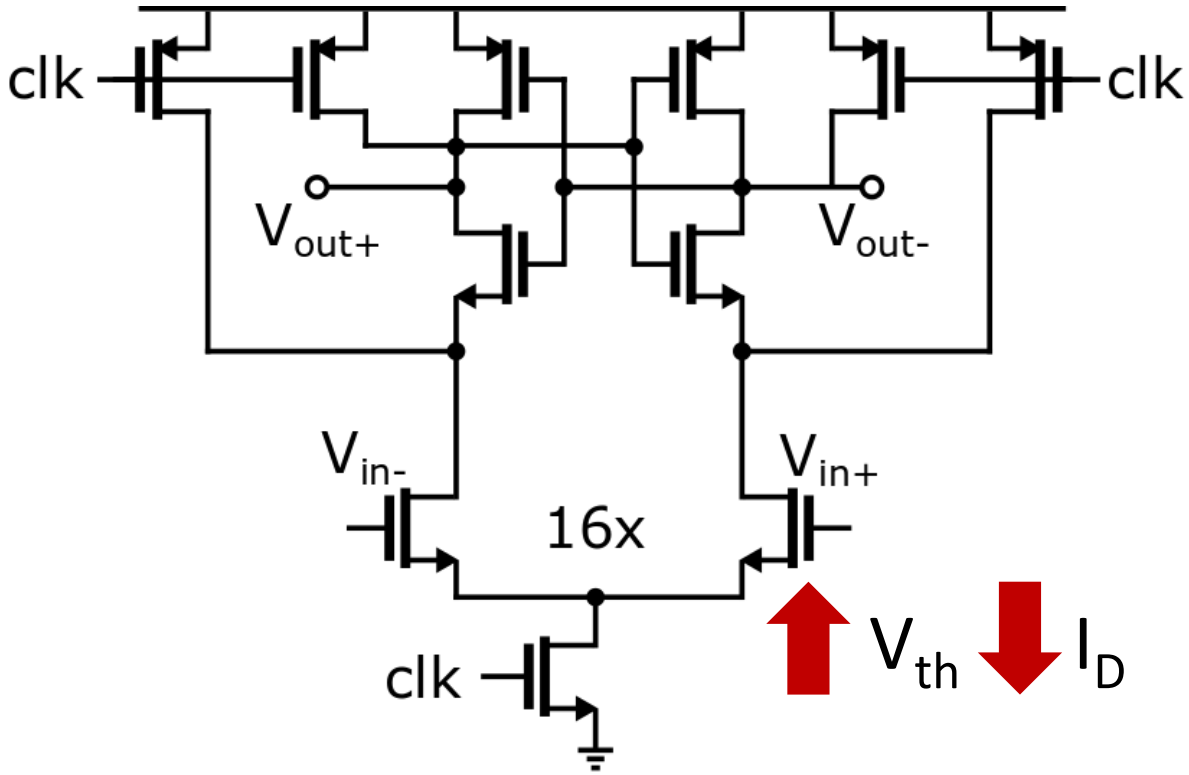
- Strong-ARM comparator
  - Energy efficient
  - Fast
- Speed degrades at higher V_{th}



Comparator design

Challenge: V_{th} increase

- Strong-ARM comparator
  - Energy efficient
  - Fast
- Speed degrades at higher V_{th}
- Possible solution: raise CM
- Issue: limiting input swing

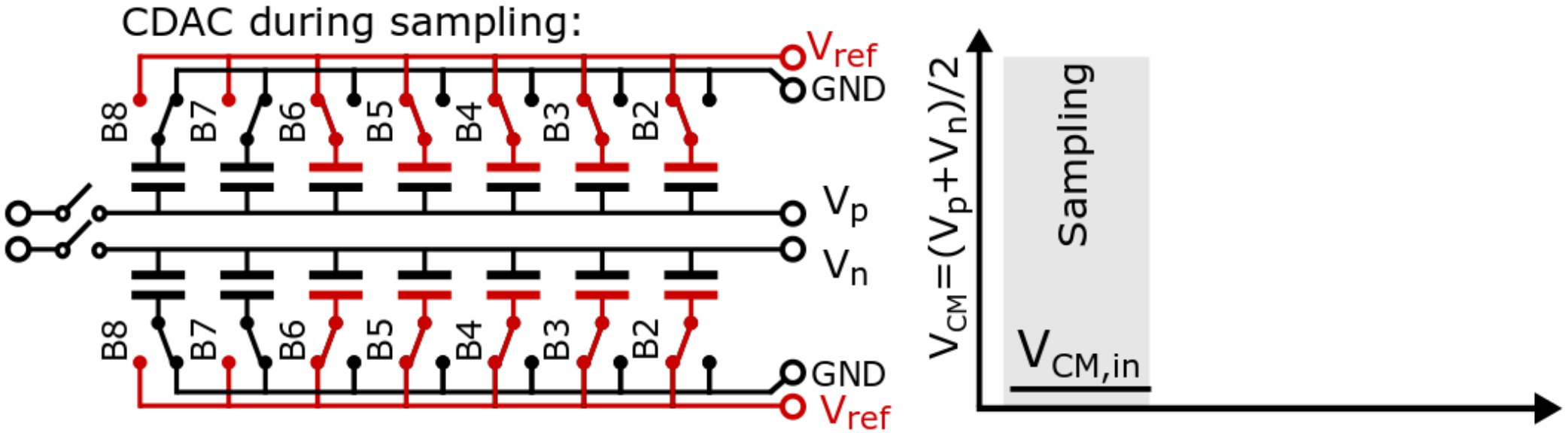


IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 56 Sept 2024. Keynote presentation given at WOLTE-16 2024, June 2024, Cagliari, Italy.

Common mode switching scheme

Solution: adapted V_{CM}

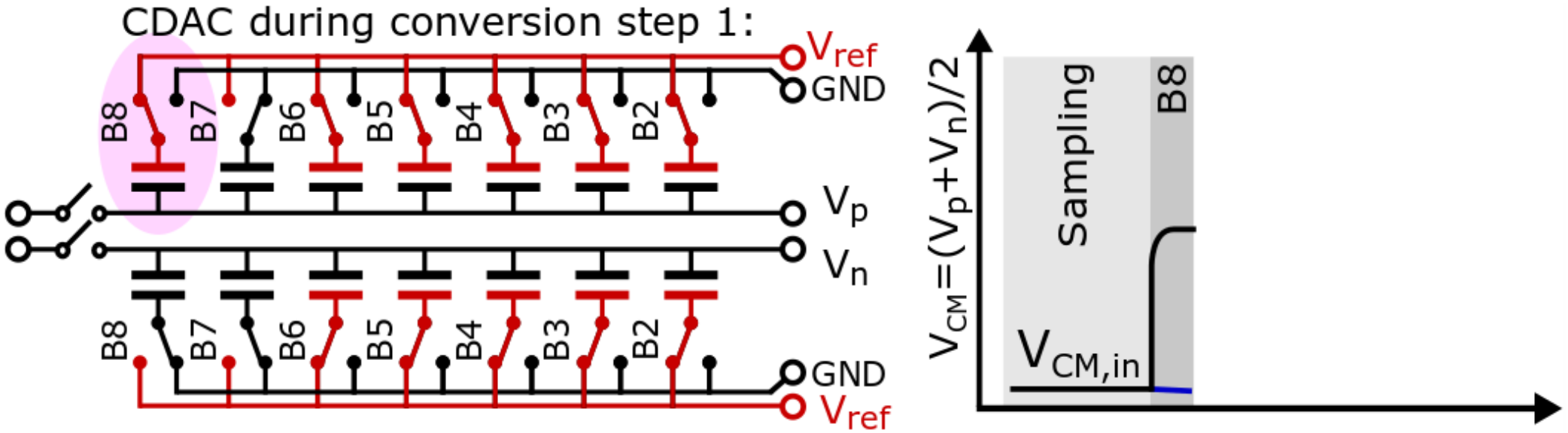
- Input: mid-rail common mode for large-swing core-VDD driver



Common mode switching scheme

Solution: adapted V_{CM}

- Input: mid-rail common mode for large-swing core-VDD driver
- First two bits: V_{CM} up



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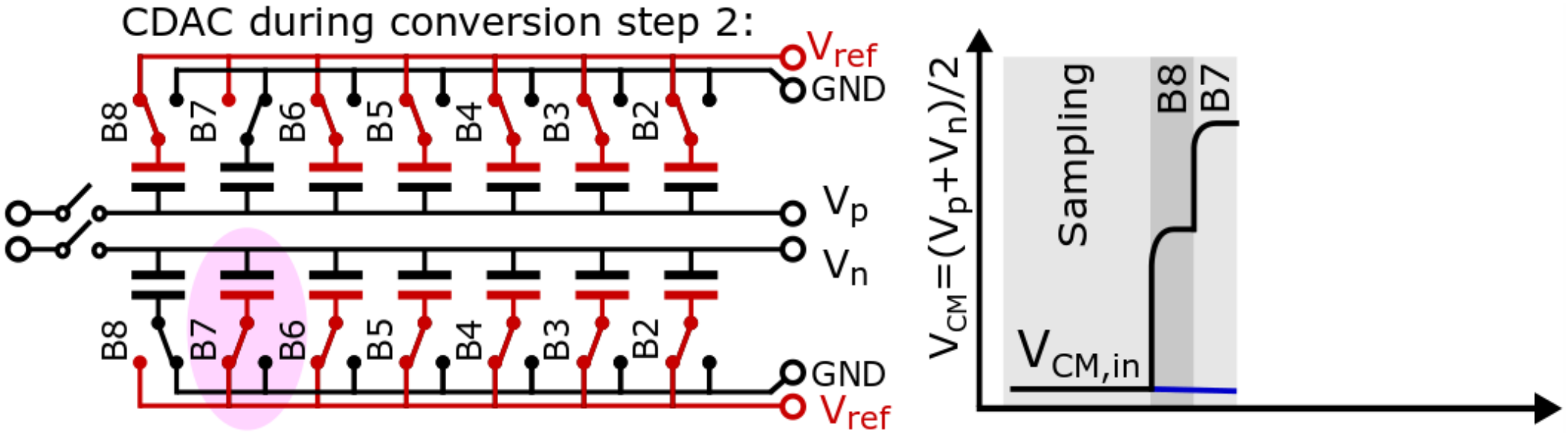
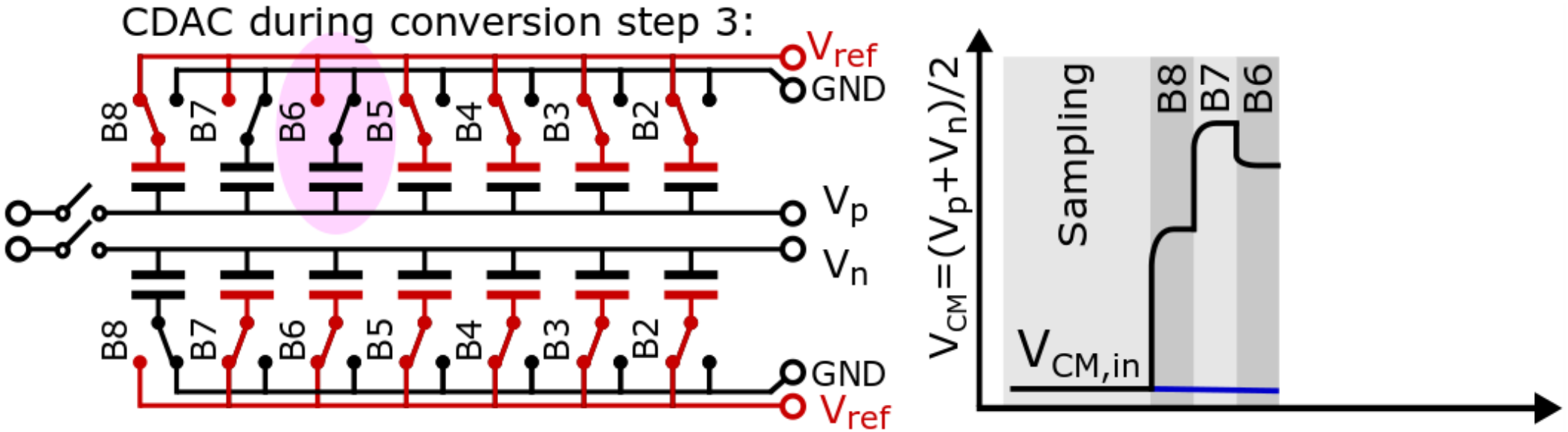


Common mode switching scheme

Solution: adapted V_{CM}

- Input: mid-rail common mode for large-swing core-VDD driver
- First two bits: V_{CM} up
- Rest of bits: V_{CM} down



IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 56 Sept 2024. Keynote presentation given at WOLTE-16 2024, June 2024, Cagliari, Italy.

Common mode switching scheme

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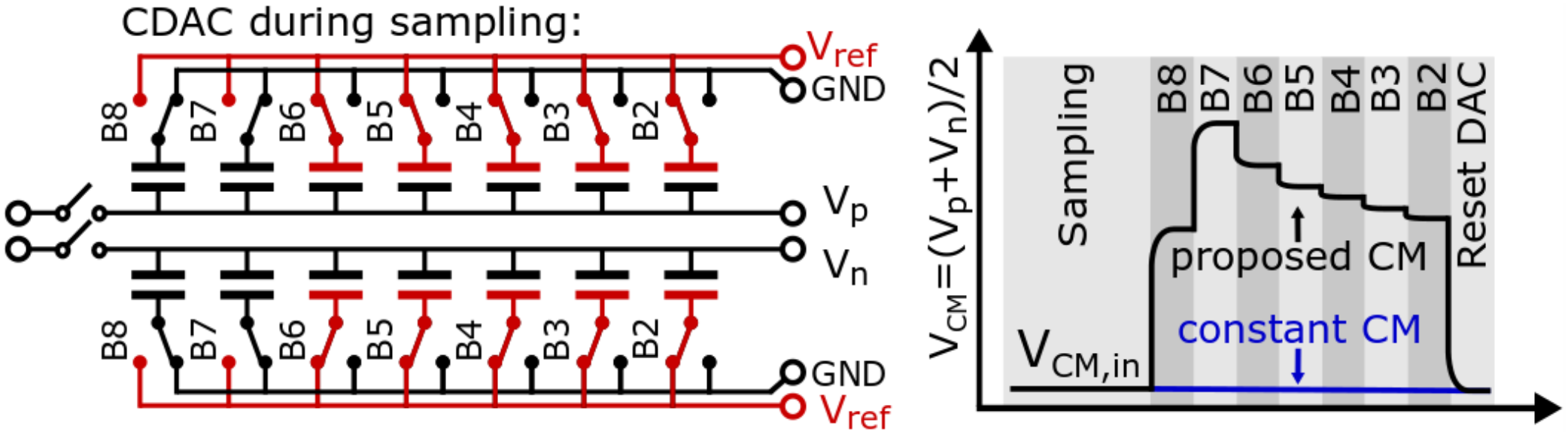
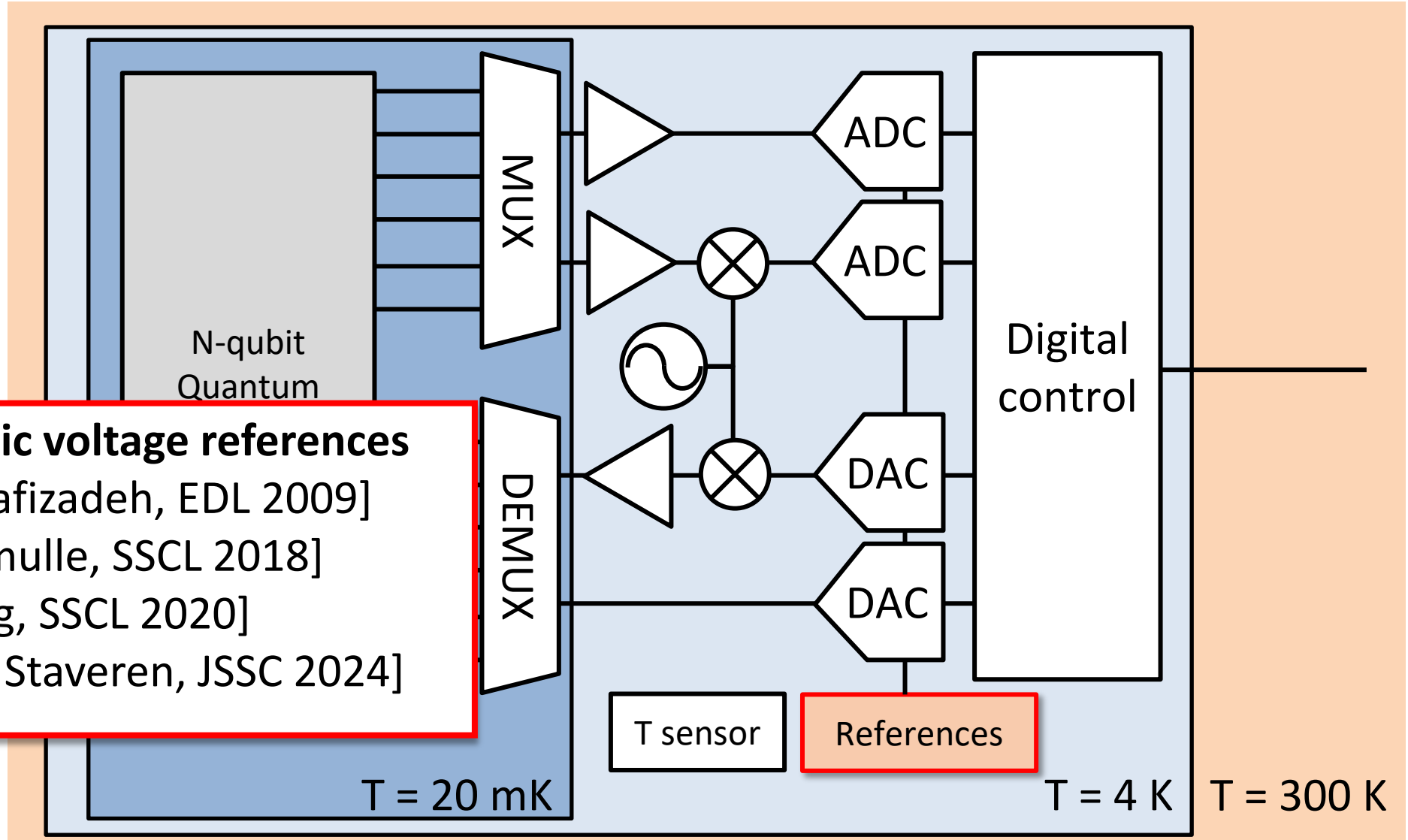


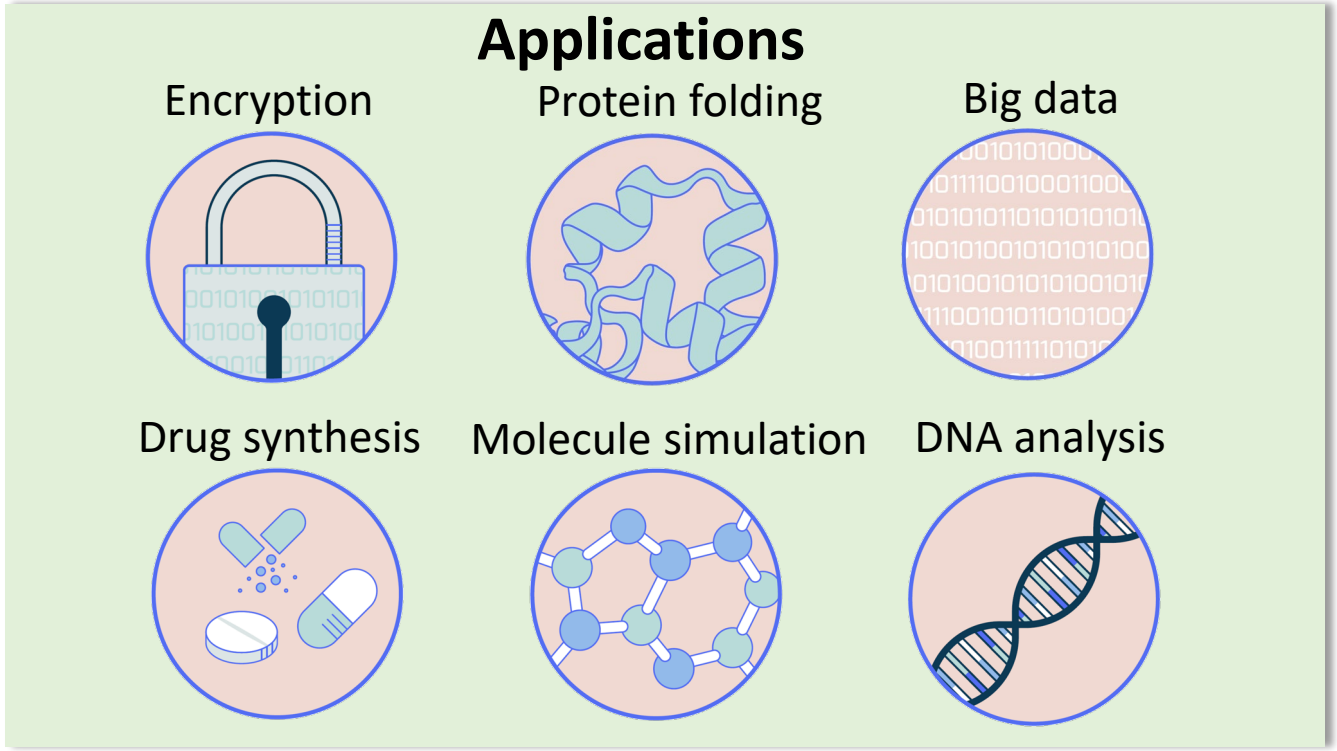
The Cryo-CMOS interface



Cryogenic voltage references

- [Najafizadeh, EDL 2009]
- [Homulle, SSCL 2018]
- [Yang, SSCL 2020]
- [van Staveren, JSSC 2024]

A practical quantum computer



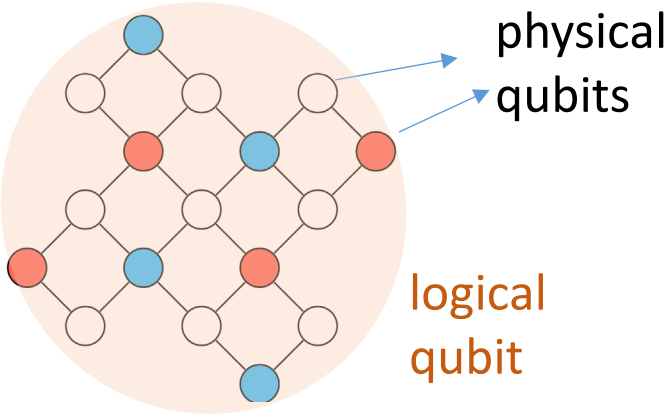
Noisy qubit

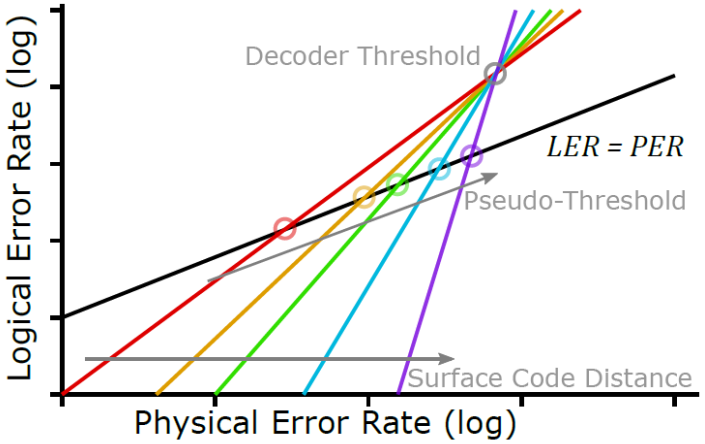
~~Ideal qubit~~

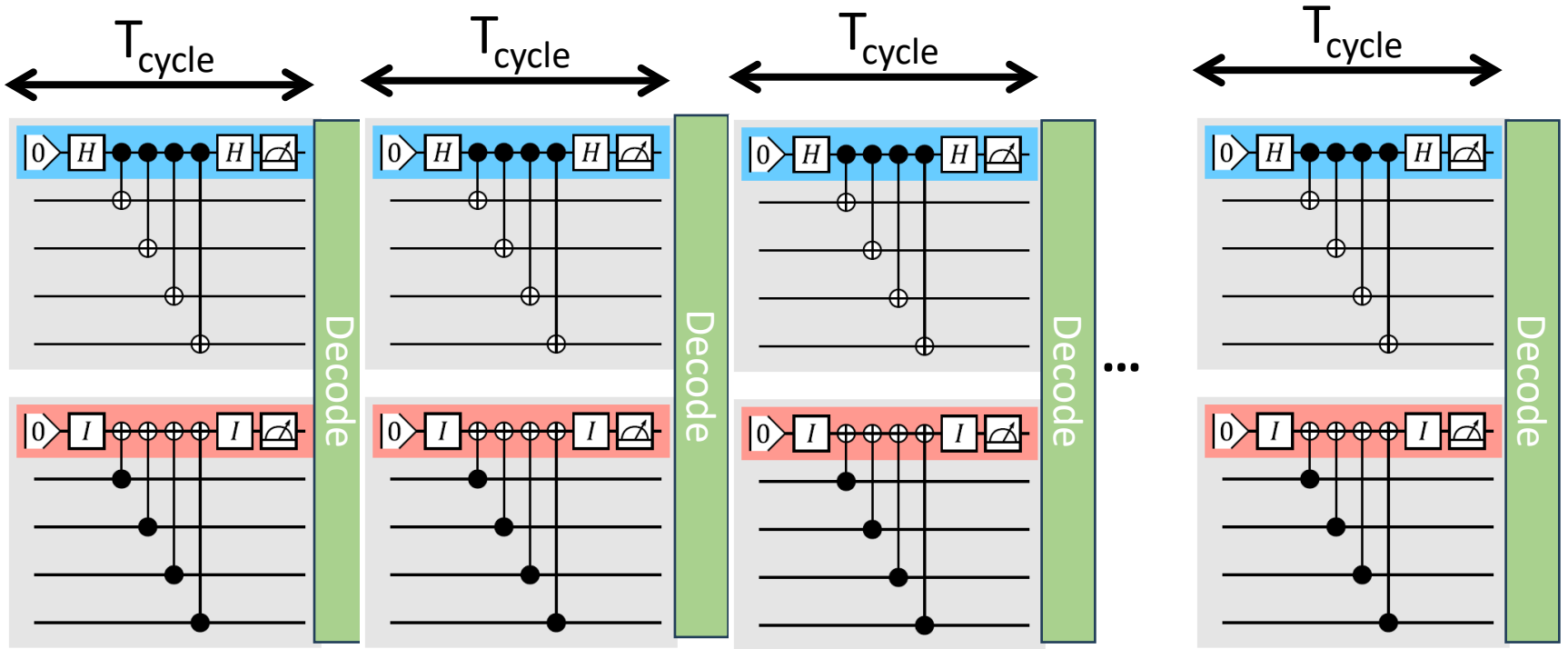
Decoherence, gate errors, measurement errors, …

Quantity to make up for quality

Surface code







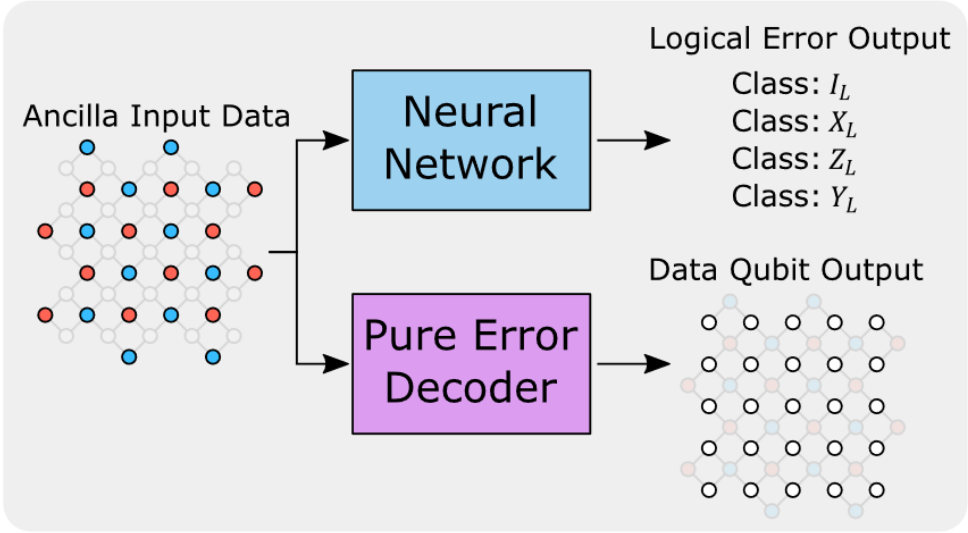
Future decoder requirements

- To factor a 2kb integer
- 22M physical qubits
- Processing time < 1 μs

Data rate > 10.3 Tbit/sec

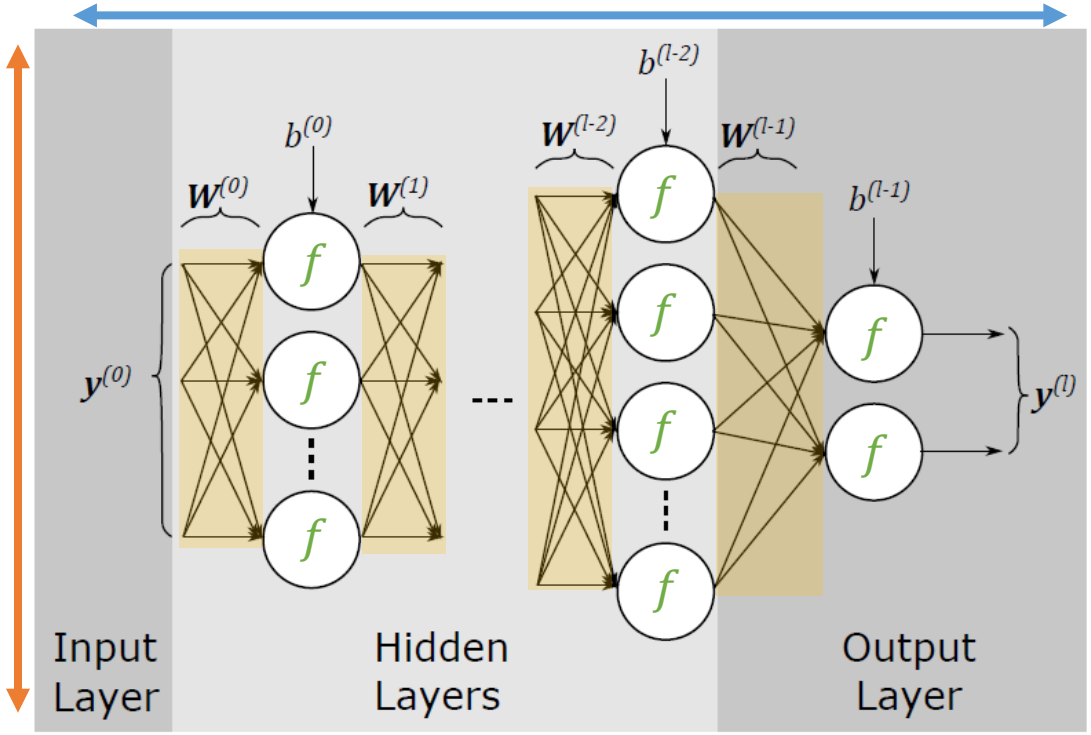
A promising HW decoder

Decoders based on Neural Networks



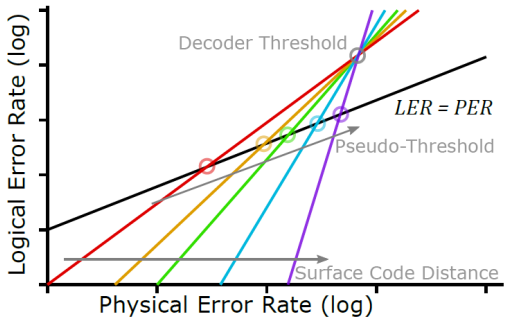
Architecture exploration

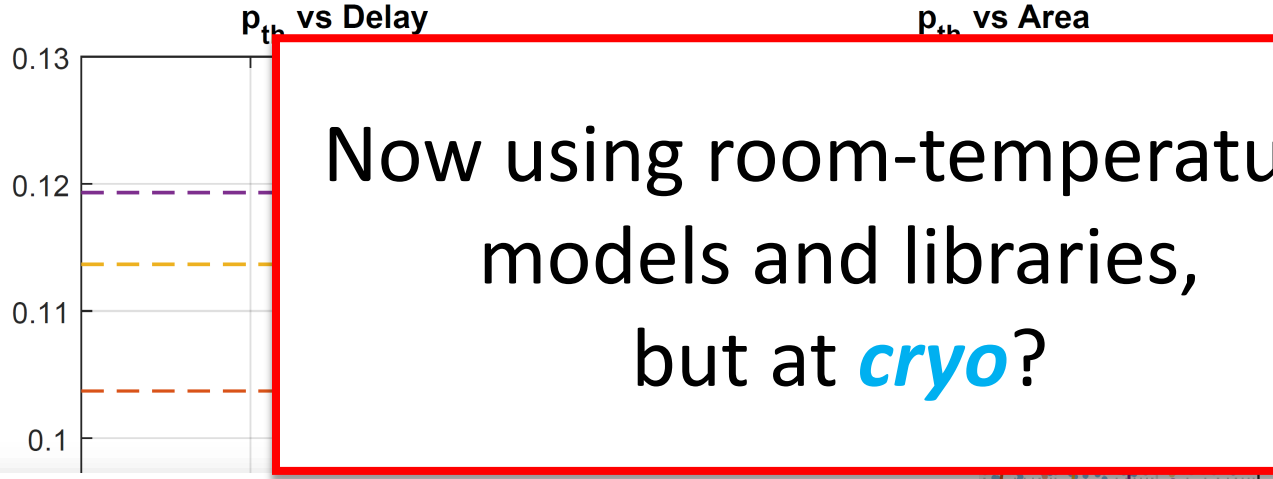
- Number of Layers
  - 2 Layers
- Layer sizes
  - Larger: more power
- Transfer functions
- Quantization



[Overwater et al., TQE 2022]

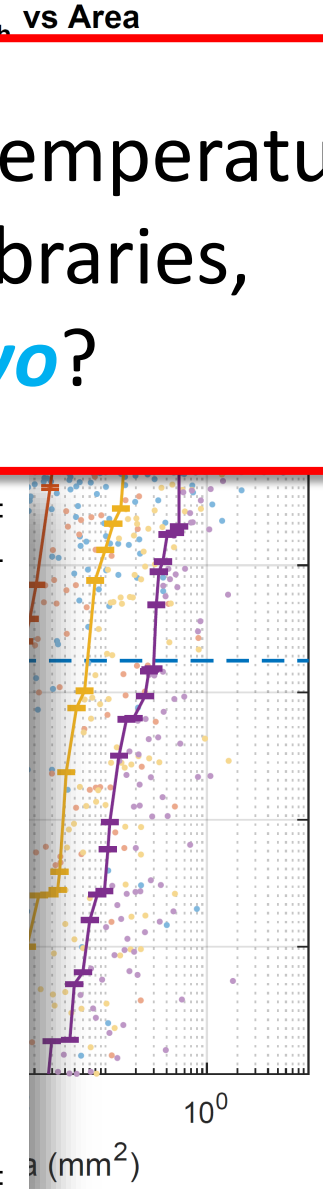
Digital Hardware QEC decoder

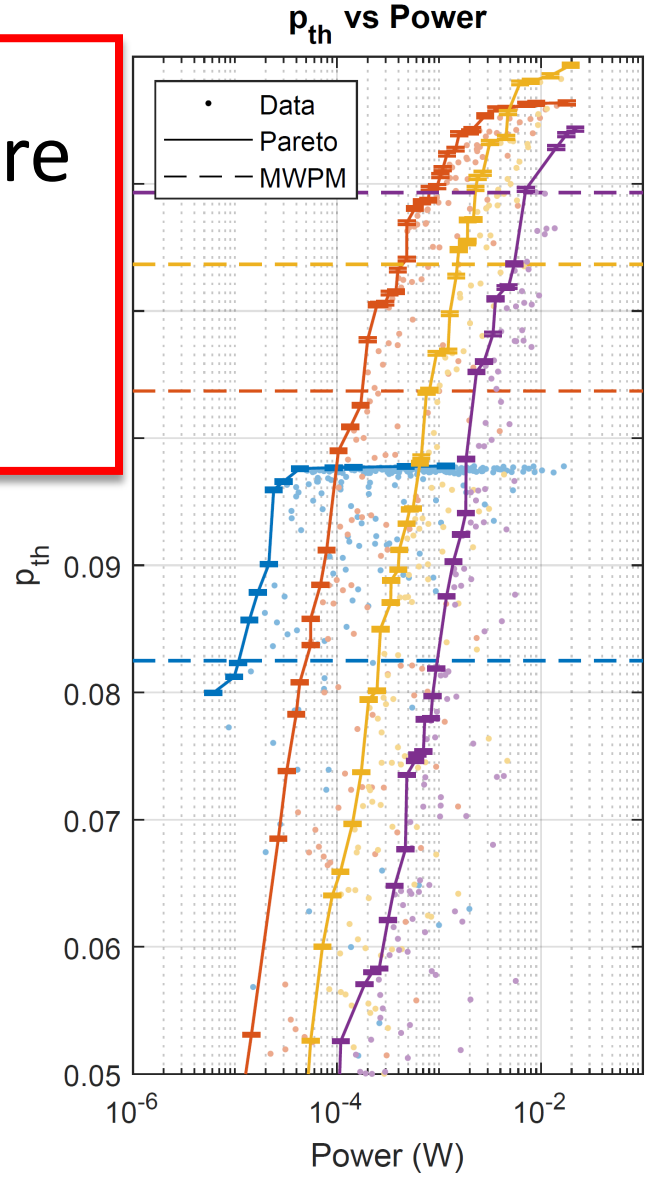




Now using room-temperature models and libraries, but at ***cryo***?

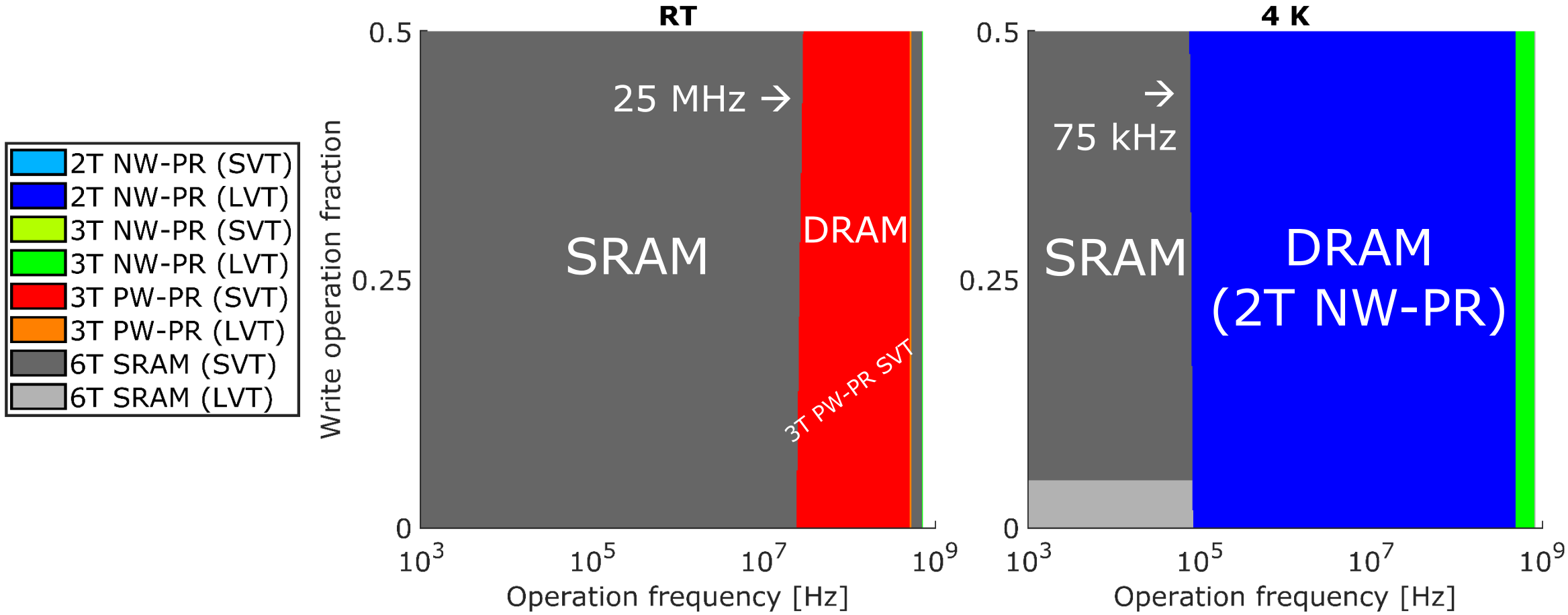
	Distance	3	3	5
Layer 1	Size	8	16	64
Layer 2	Size	4	4	64
	Bits	3	5	4
	p_{th}	0.0823	0.0976	0.1037
	Slope	1.8641	1.8868	2.6641
FPGA	Delay	17.9 ns	71.9 ns	87.6 ns
	Area	351 LUT	2942 LUT	44670 LUT
	Power	< 1 mW	6 mW	132 mW
ASIC	Delay	7.3 ns	12.3 ns	14.3 ns
	Area	0.0031 mm^2	0.0114 mm^2	0.3937 mm^2
	Power	10.7 μW	43.2 μW	1.0 mW





[Overwater et al., TQE 2022]

Memory Benchmark

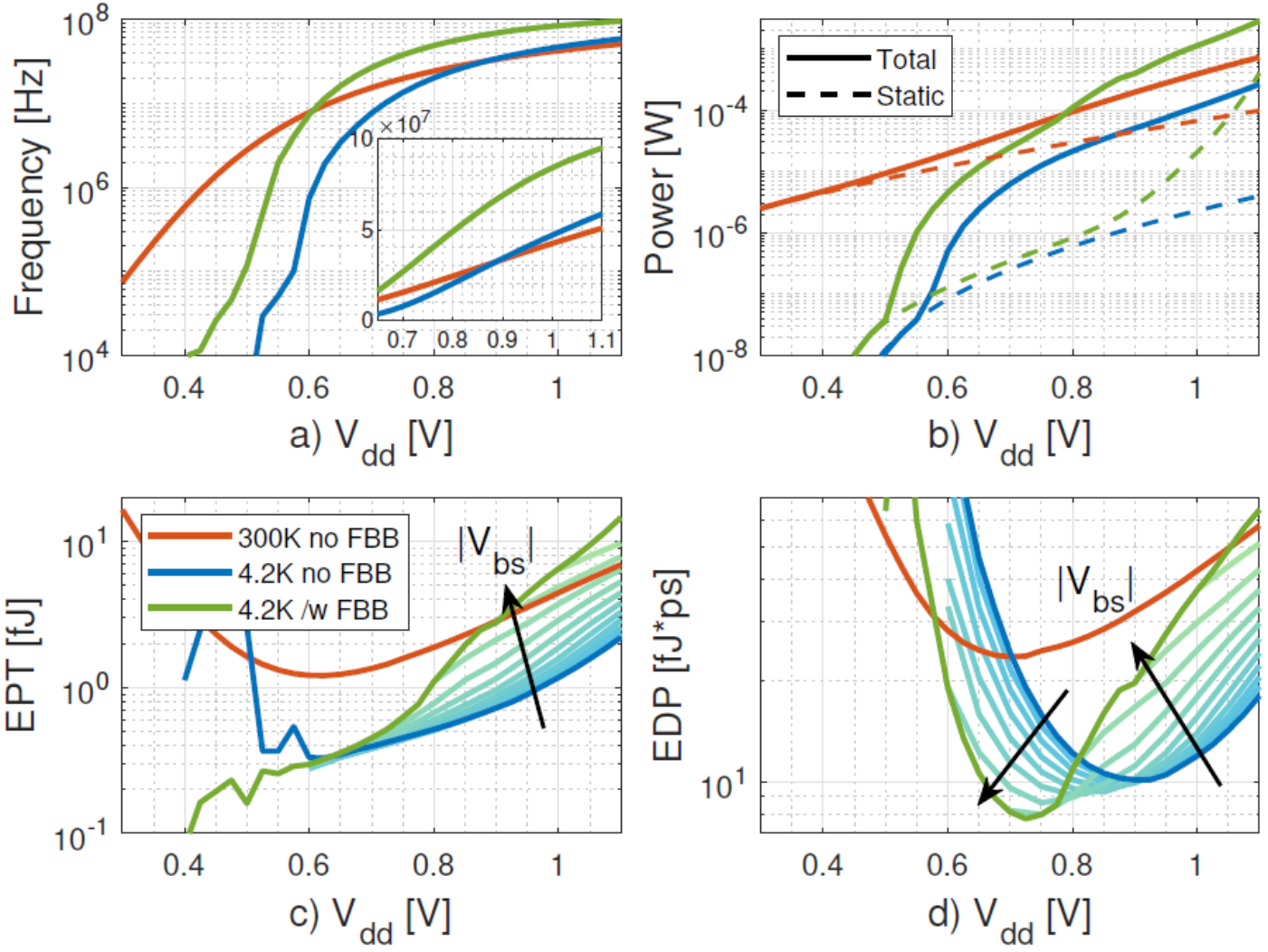


- Some DRAM designs do not work
- DRAM more widely applicable

[Damsteegt, JSSC 2024]

Cryogenic–aware FBB – Digital logic

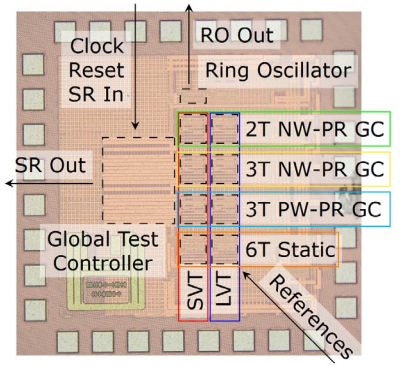
- LVT D1 inverter RO (N = 1025)
- Compared to
  - no BB and V_{dd} = 1.1 V
- High-speed design
  - $V_{dd} = 1.1$ V and full BB
  - Speed → x 1.62
  - Power dominated by short-circuit
- Low-power design
  - $V_{dd} = 0.725$ V and full BB
  - Speed → 1/1.82
  - EPT → 1/4.24
  - EDP → 1/2.33

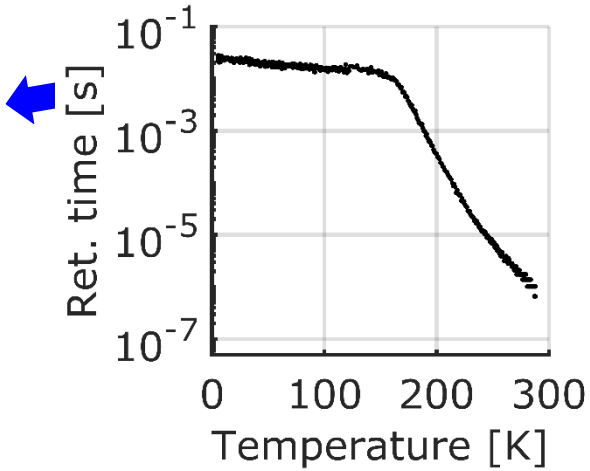


[Overwater et al., EDL 2023]

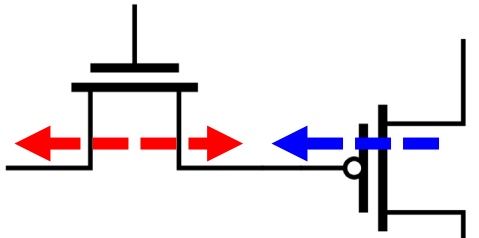
DRAM Retention time (LVT)

40-nm CMOS





NW subth. leakage

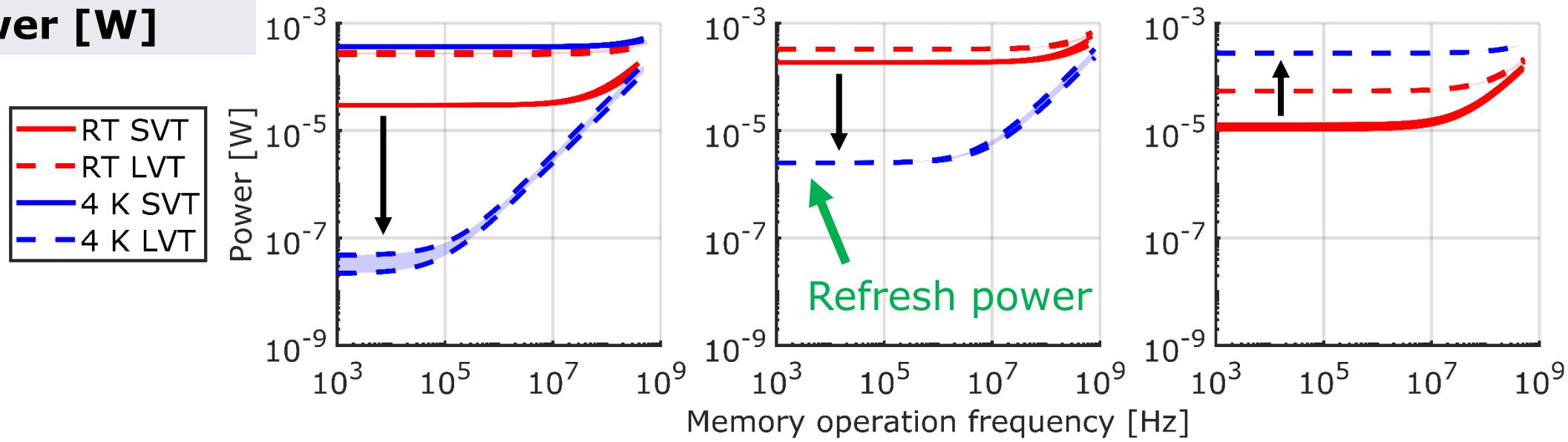


PR gate leakage

[Damsteegt, JSSC 2024]

DRAM performance

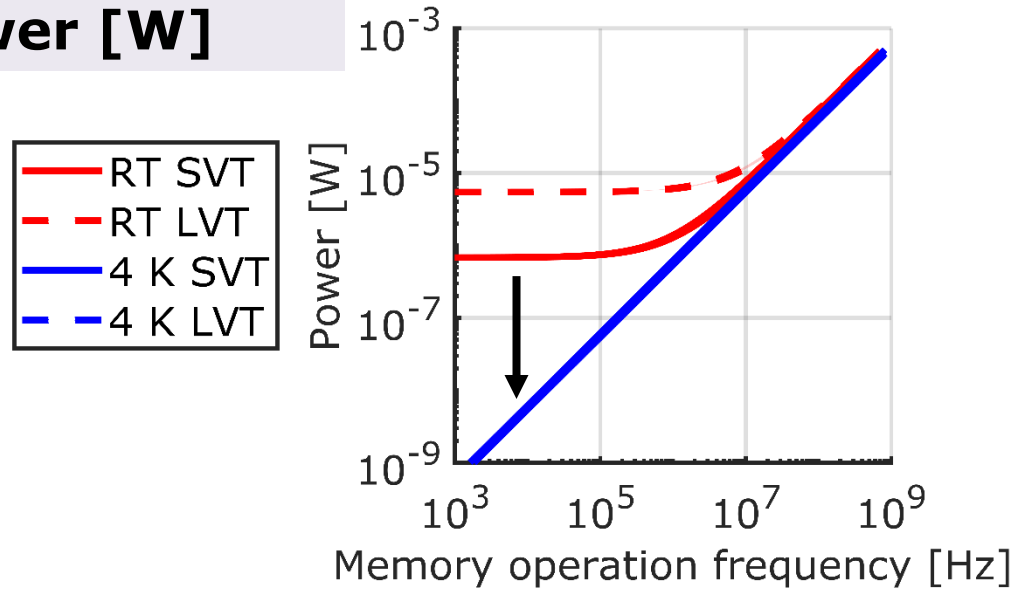
Cell type		2T NW-PR		3T NW-PR		3T PW-PR	
		SVT	LVT	SVT	LVT	SVT	LVT
Cell size [µm²]		0.184		0.242		0.254	
Latency [ns]	RT						
	4 K						
Power [W]							

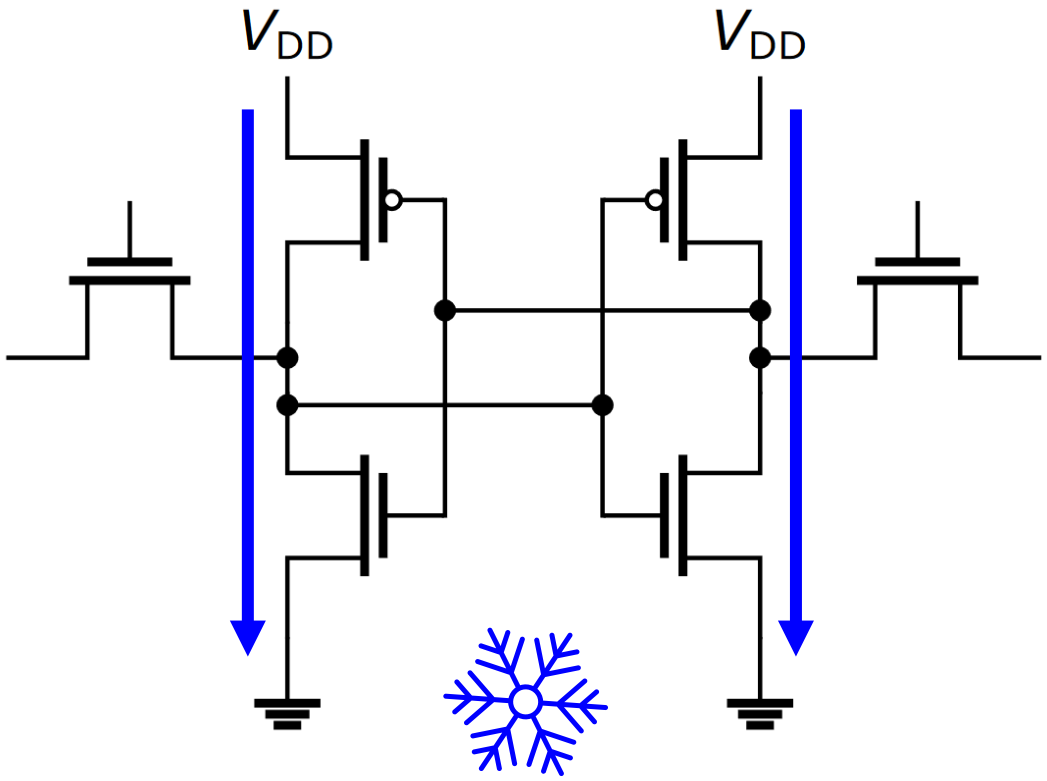


[Damsteegt, JSSC 2024]

SRAM performance

Cell type		6T SRAM	
		SVT	LVT
Cell size [µm²]		0.435	
Latency [ns]	RT	1.42	1.40
	4 K	1.23	1.18
Power [W]			





[Damsteegt, JSSC 2024]