IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at the International Symposium on Superconductivity, Virtual, December 2, 2021.

34th International Symposium on Superconductivity (ISS 2021)
ED5-1-INV

Recent Progress in Adiabatic Quantum-Flux-Parametron Logic

N. Takeuchi[1,2], C. L. Ayala[2], C. Olivia[3], N. Yoshikawa[2]
[1]Nat'l Inst. of Advanced Industrial Sci. & Tech. (AIST)
[2]Yokohama National University
[3]Tokyo City University

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Outline

- **Introduction to AQFP logic**
  - Adiabatic switching
  - Design methodology
- **Recent progress in AQFP logic**
  - Microprocessor
  - Single-photon image sensor
  - Stochastic electronics

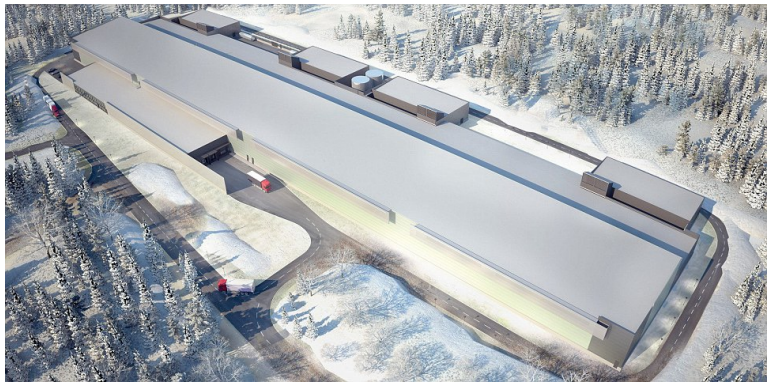
IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Outline

- **Introduction to AQFP logic**
  - Adiabatic switching
  - Design methodology
- **Recent progress in AQFP logic**
  - Microprocessor
  - Single-photon image sensor
  - Stochastic electronics

Background

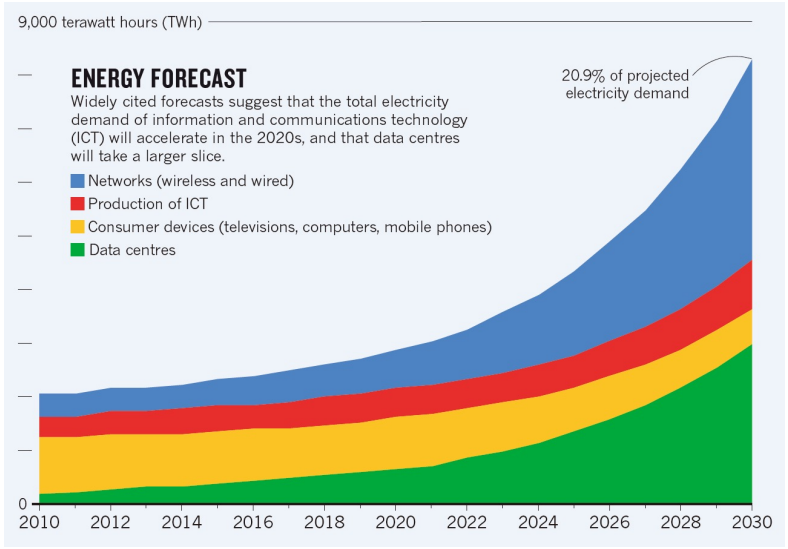
Facebook data center in Sweden



- Performance: 27–51 PFLOPS
- Power: 84 MW avg (120 MW max)
- cf. Amagase dam: 92 MW (#4 in Kyoto)

D. S. Holmes, ISS 2013.

Energy forecast



N. Jones, Nature **561**, 163 (2018).

- Rising power demand for ICT due to IoT, AI, Society 5.0, etc.
- Expected to reach 20.9% of global total power by 2030
- Extremely low-power computing systems required for future ICT

Adiabatic quantum-flux-parametron (AQFP)

Operating principle

- Powered by the ac excitation current I_x
- J_1 and J_2 generate the signal current I_s.
- Underdamped high-J_c junctions used for low-energy op.

Advantages

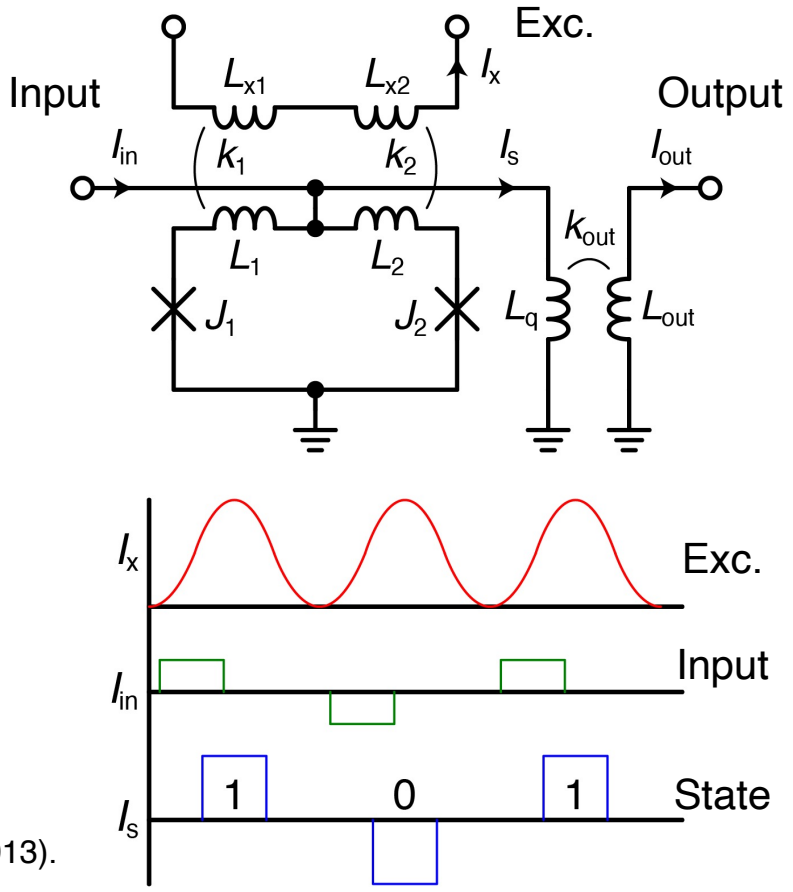
✓ Low energy dissipation
- Zero static power
- Adiabatic switching (~10^{-21} J)

✓ High sensitivity (GZ < ~1 μA)

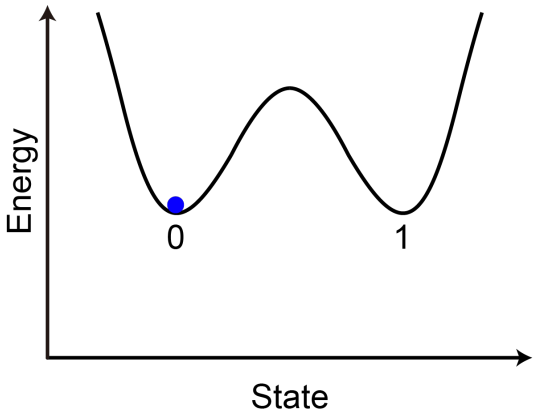
✓ Low-current drive (~ mA)

Original QFP: M. Hosoya et al., IEEE TAS. **1** (1991).
AQFP: N. Takeuchi et al., Supercond. Sci. Tech. **26** (2013).

Basic gate

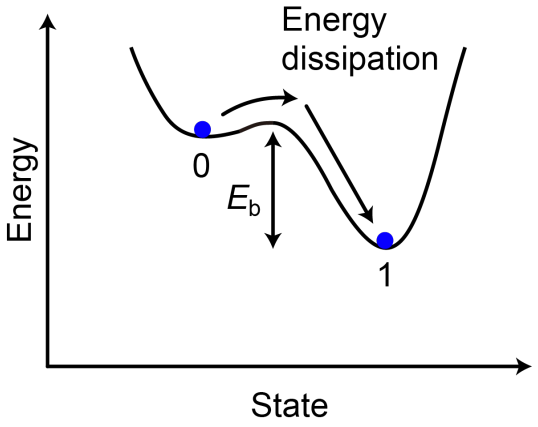


Non-adiabatic vs. adiabatic switching

Non-adiabatic switching	
Logic	CMOS, RSFQ etc.
Potential change while logic state switches	
Reversible?	
Work by a power supply	
Energy dissipation	

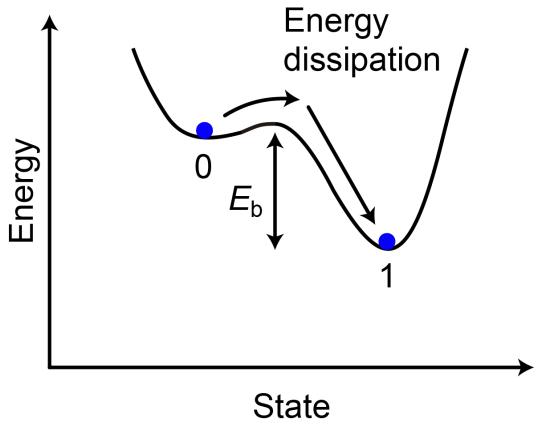
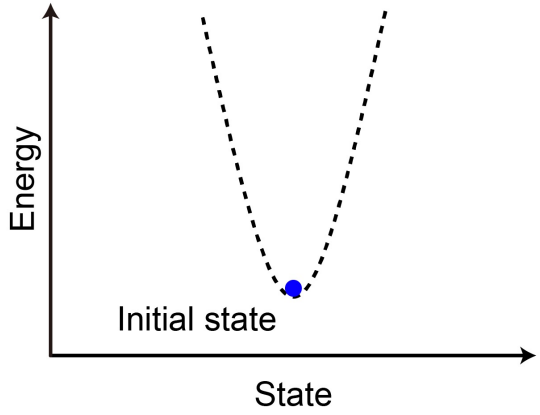
R. W. Keyes, Proc. IEEE **69** (1981).
V. V. Zhirnov et al., Proc. IEEE **9** (2003).

Non-adiabatic vs. adiabatic switching

Non-adiabatic switching	
Logic	CMOS, RSFQ etc.
Potential change while logic state switches	
Reversible?	No
Work by a power supply	Totally dissipated
Energy dissipation	$= E_b$ ($>> k_B T$)

R. W. Keyes, Proc. IEEE **69** (1981).
V. V. Zhirnov et al., Proc. IEEE **9** (2003).

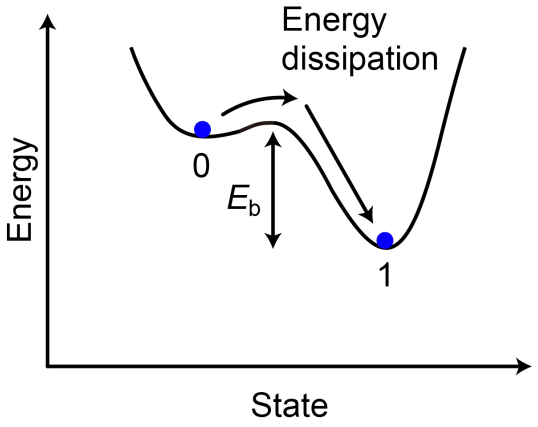
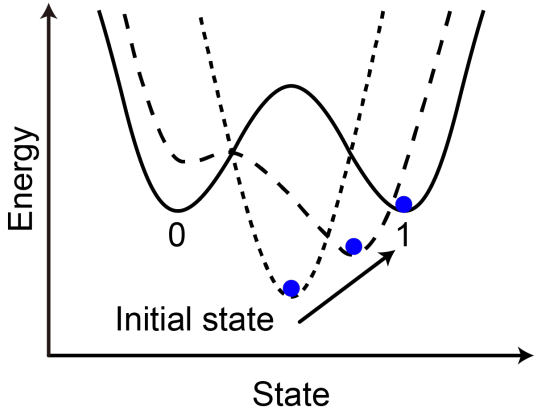
Non-adiabatic vs. adiabatic switching

	Non-adiabatic switching	Adiabatic switching
Logic	CMOS, RSFQ etc.	AQFP, nSQUID, PQ etc.
Potential change while logic state switches		
Reversible?	No	
Work by a power supply	Totally dissipated	
Energy dissipation	$= E_b$ ($>> k_B T$)	

R. W. Keyes et al., IBM J. Res. Dev. **14** (1970).
K. Likharev, IEEE Trans. Magn. **13** (1977).

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Non-adiabatic vs. adiabatic switching

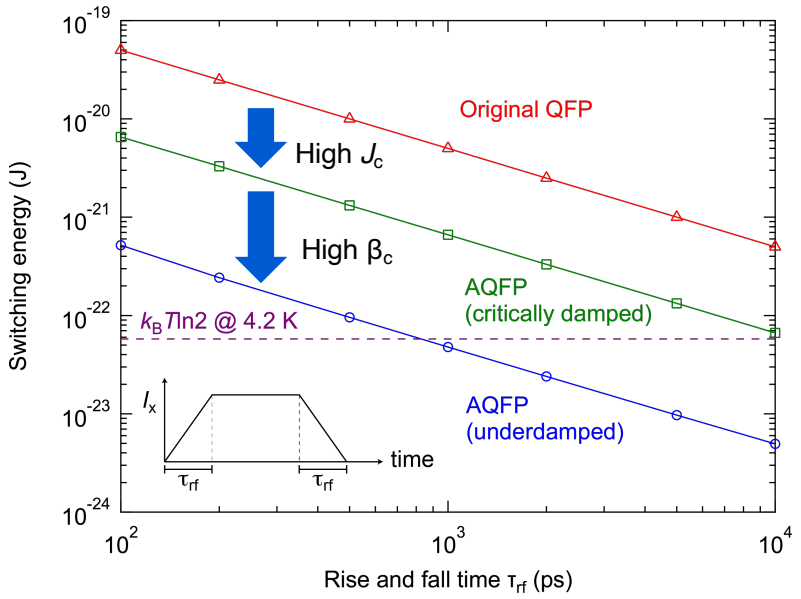
	Non-adiabatic switching	Adiabatic switching
Logic	CMOS, RSFQ etc.	AQFP, nSQUID, PQ etc.
Potential change while logic state switches		
Reversible?	No	Yes
Work by a power supply	Totally dissipated	Not dissipated @ quasi-static
Energy dissipation	$= E_b$ ($>> k_B T$)	$<< E_b$

R. W. Keyes et al., IBM J. Res. Dev. **14** (1970).
K. Likharev, IEEE Trans. Magn. **13** (1977).

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Switching energy of an AQFP gate

Numerical simulation



N. Takeuchi et al., Phys. Rev. Appl. **4** (2015).

Analytical estimation

$$E_{sw} \propto I_c \Phi_0 \frac{\left(\sqrt{\beta_c J_c}\right)^{-1}}{\tau_{rf}}$$

Characteristic time

Energy scale

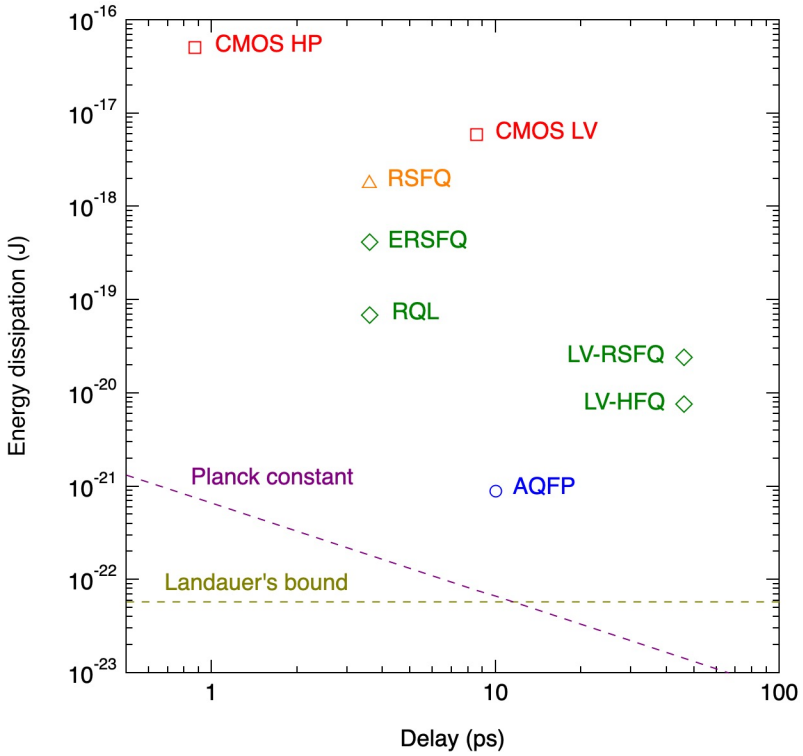
Duration time

τ_{rf}: Rise time of excitation current
β_c: McCumber parameter
I_c: Critical current of junctions
J_c: Critical current density

Switching energy can fall below $k_B T \ln 2$ by lowering frequencies and/or increasing β_c of JJs.

Energy and delay comparison

Basic gate: Energy vs. delay



Energy-delay product (EDP)

Logic	EDP (J·s)
CMOS HP	4.4×10^{-29}
RSFQ	6.3×10^{-30}
AQFP	9.0×10^{-33} ($= 14h$)

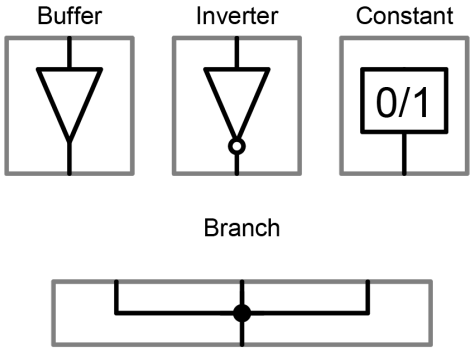
- CMOS: Inverter, AQFP: Buffer, others: JTL
- I_c = 50 μA for all supercond. devices
- Delay of RSFQ, ERSFQ, RQL: 3.6 ps
- ERSFQ: $2I_c\Phi_0 \times 2$ JJs [Mukhanov, IEEE TAS **21** (2011)]
- RQL: $0.33I_c\Phi_0 \times 2$ JJs [Herr, JAP **109** (2011)]
- LV-HFQ, LV-RSFQ: Li, SuST **34** (2021)
- AQFP: Takeuchi, APL **115** (2019)

AQFP operates with an extremely small EDP.

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Minimal logic-gate design

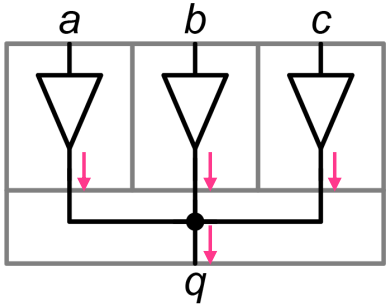
Building blocks (sub-cells)



- Gate design based on majority logic: $q = ab + bc + ca$
- Logic gates designed by placing four types of building blocks: buffer, inverter, constant, branch

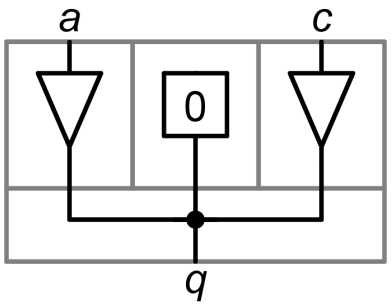
N. Takeuchi et al., J. Appl. Phys. **117** (2015).

Majority (MAJ)



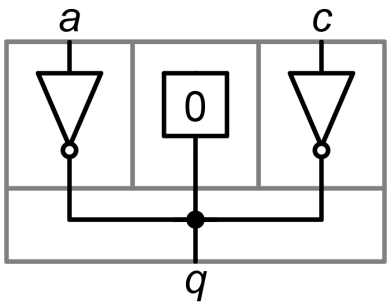
q = MAJ(a, b, c)
= ab+bc+ca

AND



q = MAJ(a, 0, c)
= ac

NOR

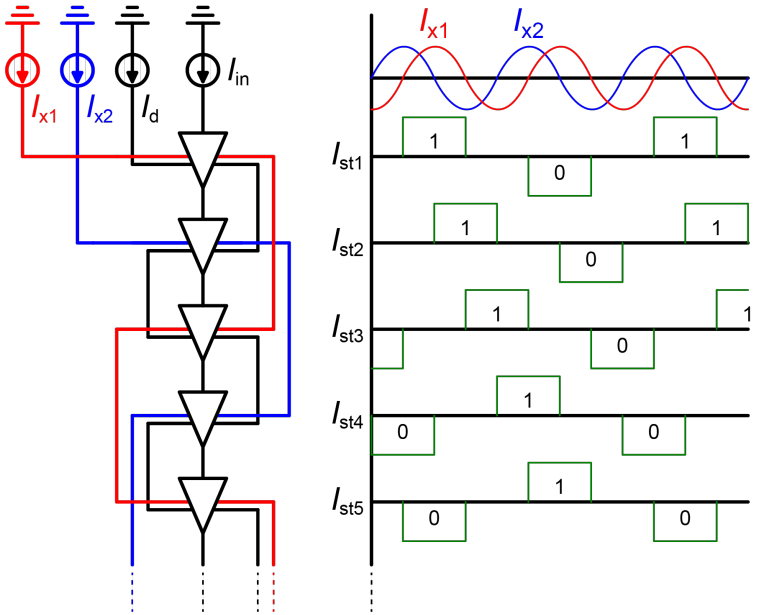


q = MAJ($\bar{a}$, 0, $\bar{c}$)
= $\bar{a}\bar{c}$ = $\overline{(a+c)}$

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Clocking schemes

Four-phase clocking

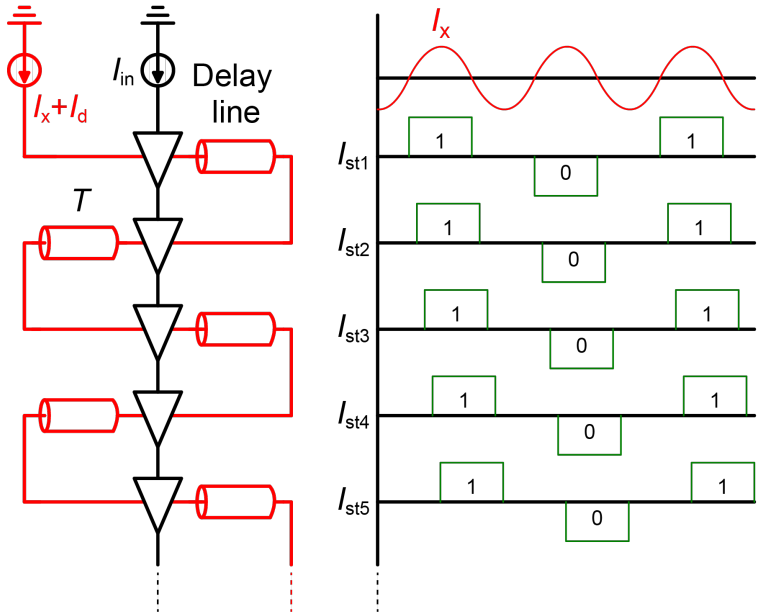


× Latency: 1/4 clock cycle per gate

✓ Arbitrary clock frequency

W. Hioe et al., IEEE TAS **5** (1995).
N. Takeuchi et al., Supercond. Sci. Tech. **30** (2017).

Delay-line clocking



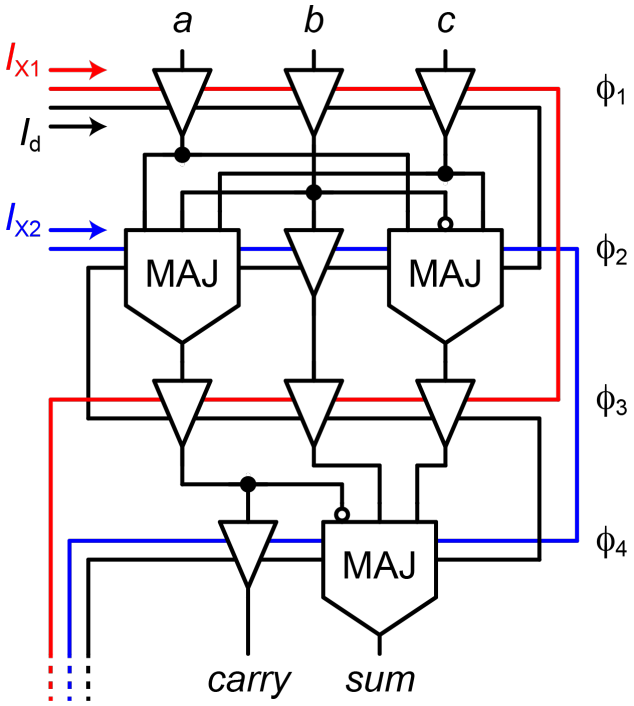
✓ Latency: arbitrary T per gate

× Do not operate at low frequency

N. Takeuchi et al., Appl. Phys. Lett. **115** (2019).

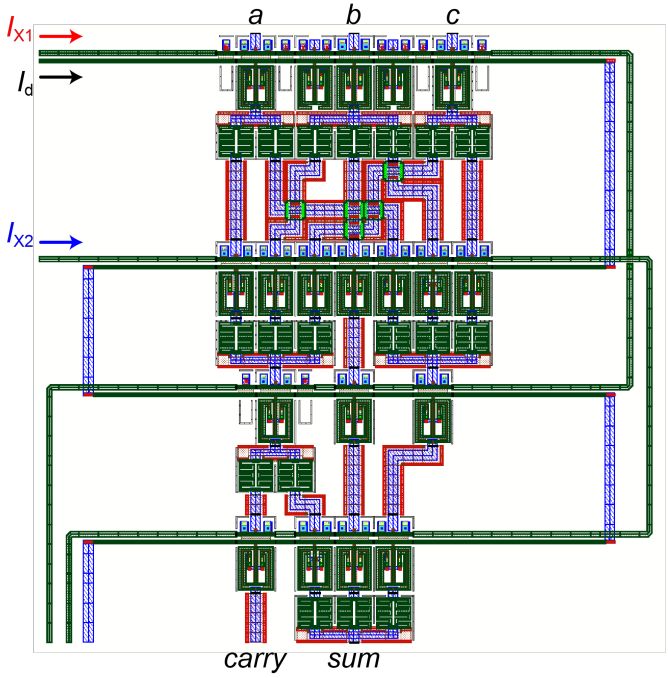
Circuit design example: Full adder

Schematic diagram



Additional buffers inserted for phase adjustment and multiple fanouts

Layout



Excitation lines designed to be 50 Ω using InductEx

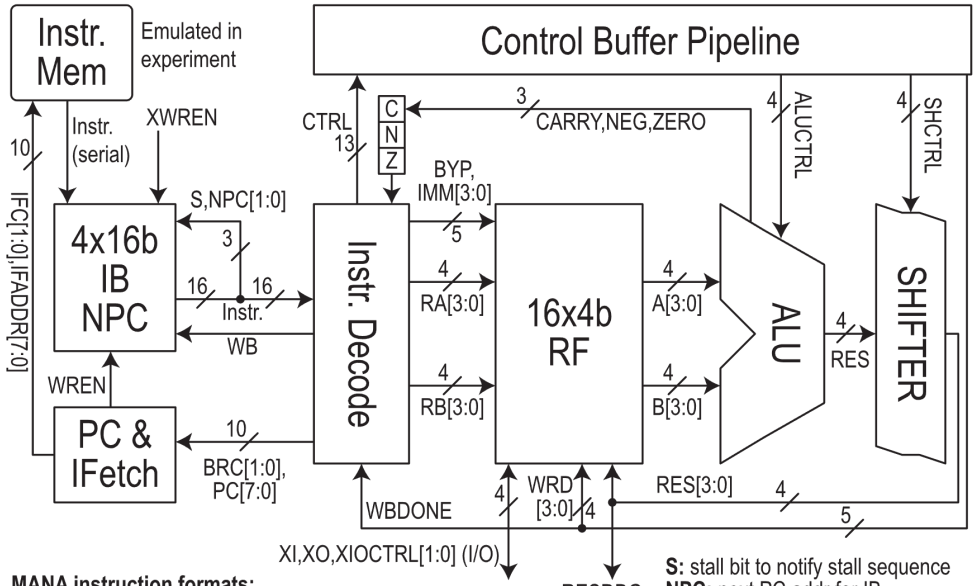
IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Outline

- Introduction to AQFP logic
  - Adiabatic switching
  - Design methodology
- **Recent progress in AQFP logic**
  - Microprocessor
  - Single-photon image sensor
  - Stochastic electronics

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

MANA microarchitecture



MANA instruction formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
S	NPC			OPCODE				IMM				RB				Immediate format
S	NPC			OPCODE				BRC/JMP ADDR								Branch/jump format
S	NPC			OPCODE				RA				RB				ALU format
S	NPC			OPCODE				SOP		AMT		RB				Shifter format
S	NPC			OPCODE				MEM								Memory access format

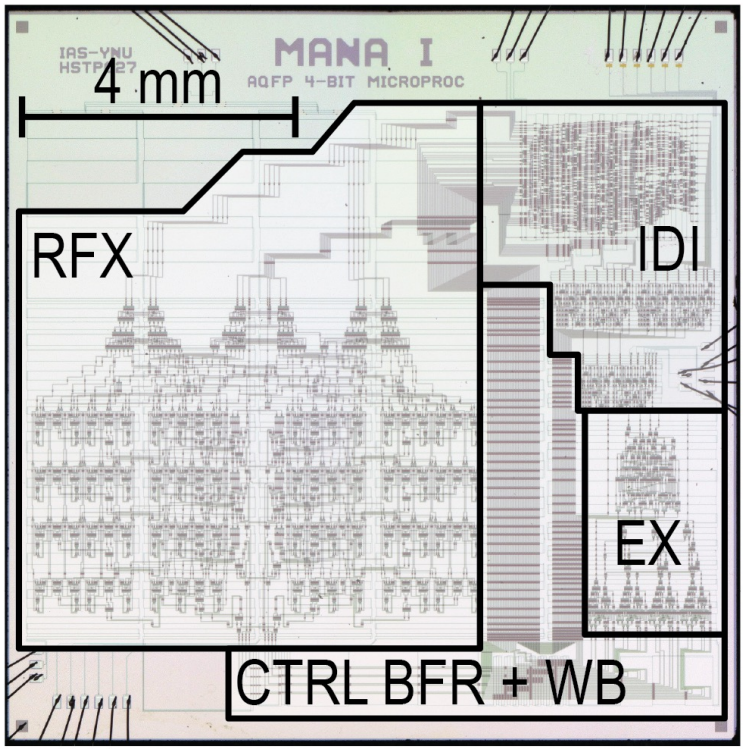
S: stall bit to notify stall sequence
NPC: next PC addr for IB
OPCODE: opcode of instr.
IMM: immediate value
BRC/JMP: branch/jump addr.
RA: reg. A addr.
RB: reg. B addr. (also destination)
SOP,AMT: shift opcode and amount
MEM: Mem. addr. for data.

MANA – Monolithic Adiabatic iNtegration Architecture

- **Goal:** Demonstrate AQFP can do both logic and memory
- RISC-like datapath + dataflow-like control
- In-order, single-issue
- 4-bit data word size
- 16-bit instr. word
- Program branching
- 21,460 JJs in 1 x 1 cm^2 chip
- 30 fJ/op at RT @ 5 GHz
- 4-phase 5 GHz clock
- Latency: 108 clock phases or 27 cycles (5.4 ns @ 5 GHz)

Instruction Buffer, Decode, and Issue (IDI)	Register File with external I/O (RFX)	ALU-Shifter (EX)	Ctrl buffer, routing, write-back (WB)
5,596 JJs	**8,142 JJs**	**2,238 JJs**	**5,484 JJs**
8 cycles (32 phases)	**8 cycles (32 phases)**	**9 cycles (36 phases)**	**17 cycles (68 phases) overlapped**
			2 cycles (8 phases) write-back

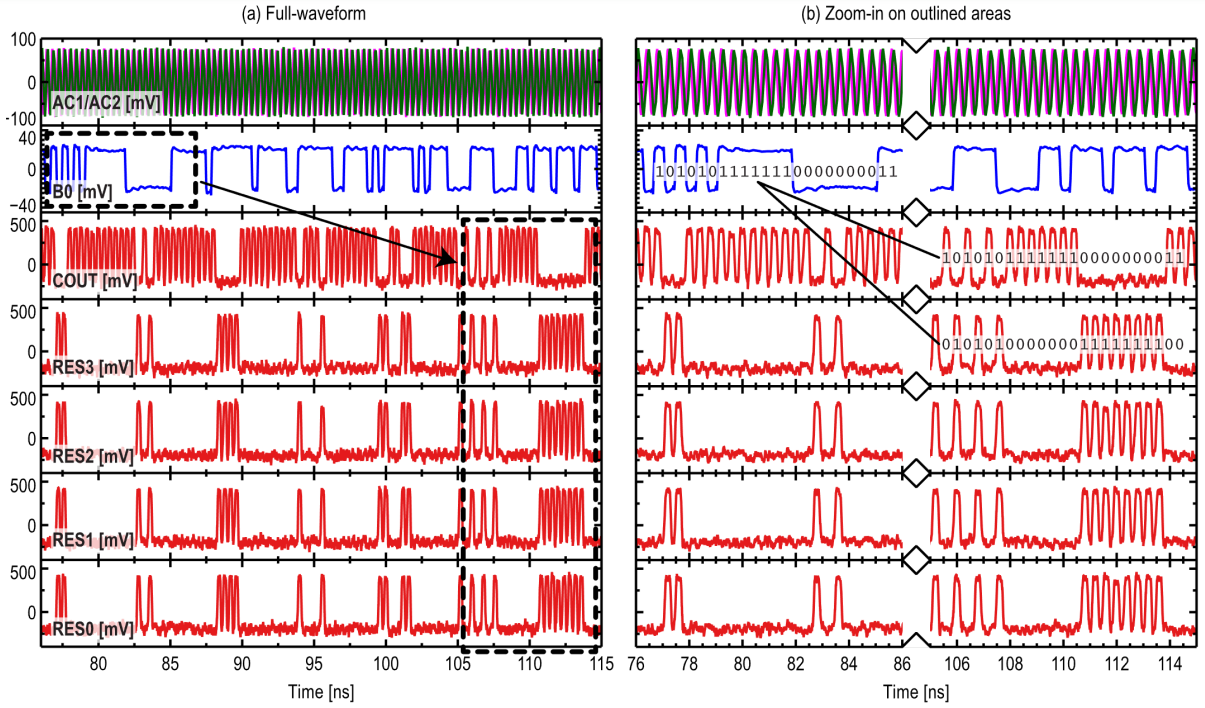
MANA prototype chip



- MANA prototype chip
  - Nb/AlO_x/Nb 10 kA/cm^2 technology
  - All stages integrated together by hand
  - 1 cm x 1 cm
  - Unoptimized clock network
  - Wire-bonded
  - 21,460 JJs
  - Latency: 27 cycles (5.4 ns @ 5 GHz)
- Experiment
  - Low-speed testing
  - 4x16-bit instruction blocks manually loaded to IB of IDI serially
  - 4-bit debug output tapped from WB data

C. L. Ayala et al., in VLSI 2020.
C. L. Ayala et al., IEEE J. Solid-St. Circ. **56** (2021).

MANA high-speed test



Critical carry-propagate high-speed test pattern (1111 + 0001)

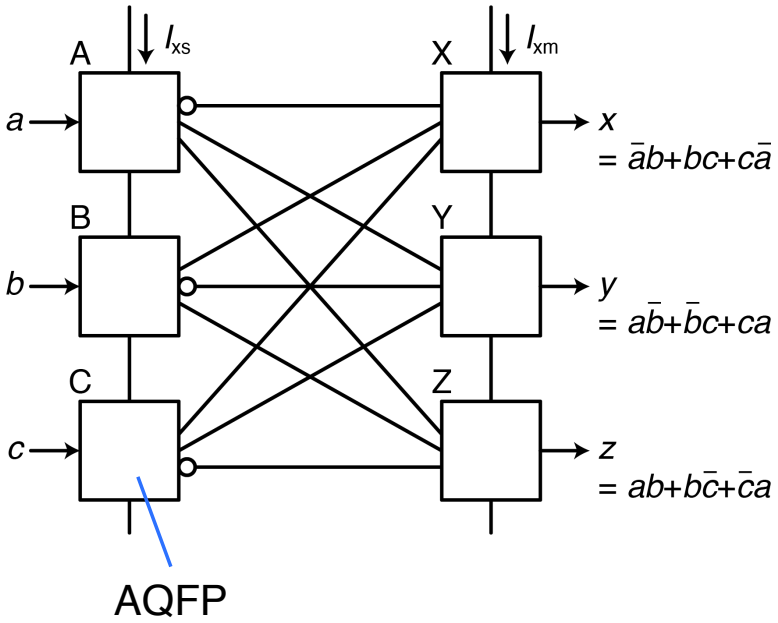
- B[0] high-speed pseudo-random inp
- B[3:1] fixed to '0'
- A[3:0] fixed to '1'

High-speed 2.5 GHz (T=400 ps) test

- Expected outputs: COUT←B[0]; RES[3:0]←!B[0]
- 1 GHz ~ 2.5 GHz operated successfully
- 3 GHz operation unstable
  - Fall-time of output too slow, may need to improve output interface or experimental setup

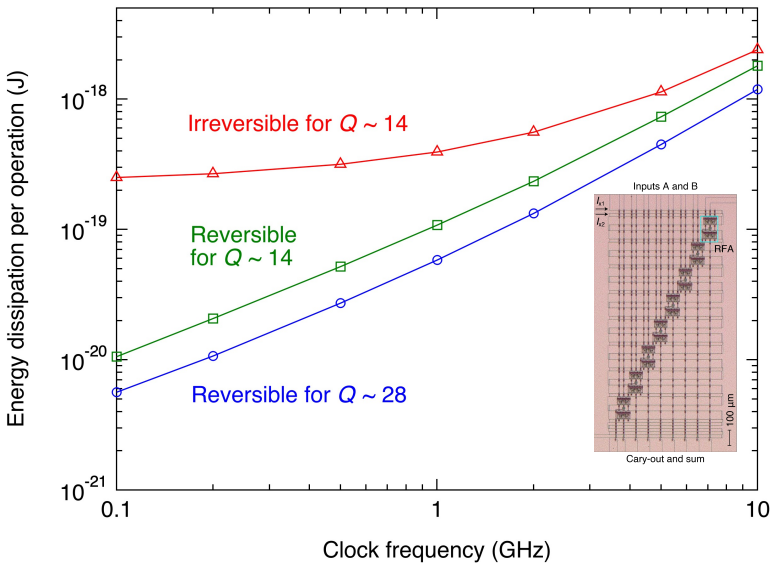
Reversible computing using AQFP

Reversible QFP (RQFP)



N. Takeuchi et al., Sci Rep. **7** (2017)

Reversible vs. irreversible 8-bit adders



N. Takeuchi et al. ASC 2020.

- Reversible circuits can be designed using RQFP gates.
- Dissipation further decreases: –73% @ 1 GHz, –96% @ 100 MHz

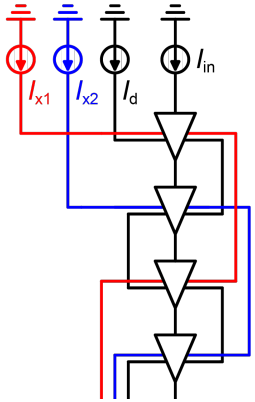
IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Outline

- Introduction to AQFP logic
  - Adiabatic switching
  - Design methodology
- **Recent progress in AQFP logic**
  - Microprocessor
  - Single-photon image sensor
  - Stochastic electronics

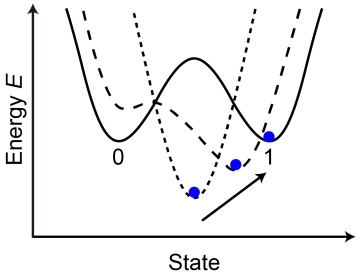
Features for detector applications

Low-current operation



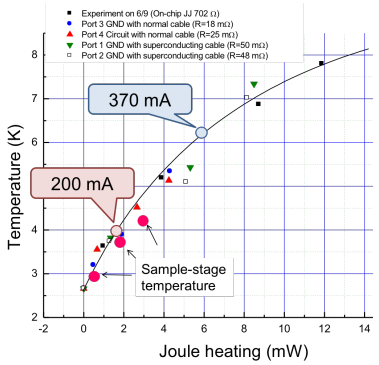
- ✓ AC flux bias
- ✓ Many gates can couple to a few common bias lines.
- ✓ Total bias current (2–3 mA) does not increase w/ gate #.

High sensitivity



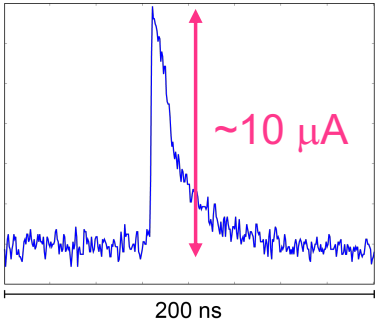
- ✓ Adiabatic switching
- ✓ Can switch to the correct state w/ small input current
- ✓ Demonstrated a ~50 nA sensitivity

N. Takeuchi et al., IEEE TAS **31** (2021).



- Total supply current limited in a compact cryocooler
- Max. supply current: ~200 mA @ 0.1-W GM cooler

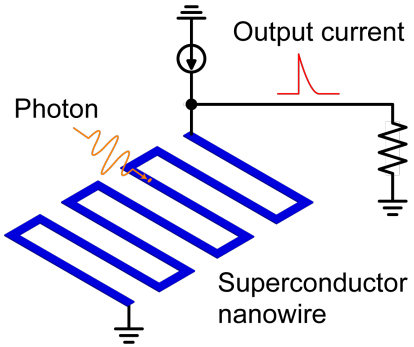
H. Terai et al., ASC2014.



- Sensitivity required for NbTiN SSPDs: ~10 μA
- WSi-SSPD: ~1 μA
- TES: less than 1 μA
- cf. Sensitivity of SFQ circ.: 1–10 μA

Single-photon image sensor

Superconducting nanowire single-photon detector (SSPD)

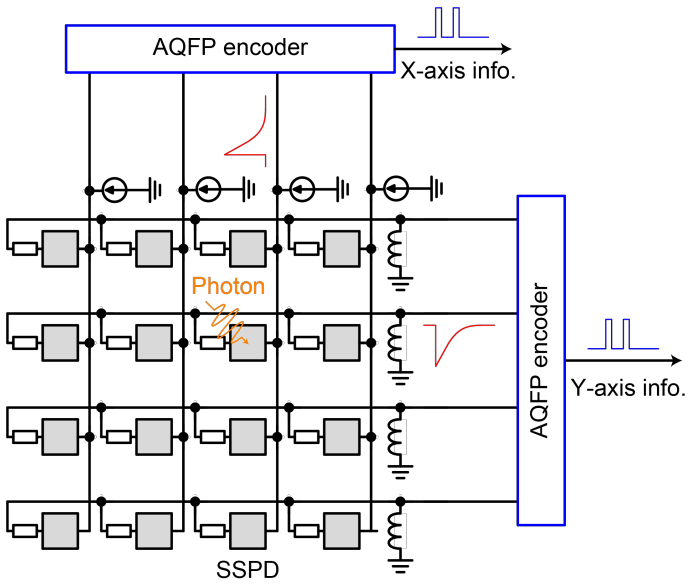


- ✓ High efficiency
- ✓ High count rate
- ✓ Low timing jitter
- ✓ Low dark count
- ✓ Wide spectral range

Original paper: G. N. Gol'tsman et al., Appl. Phys. Lett. **79** (2001).

- Single pixel technology matured; multi-pixel array under development
- Efficient readout scheme required

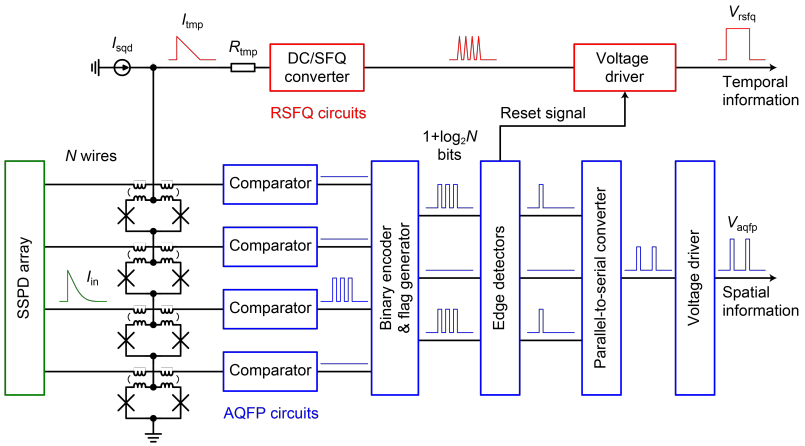
Single-photon image sensor using SSPDs and AQFP



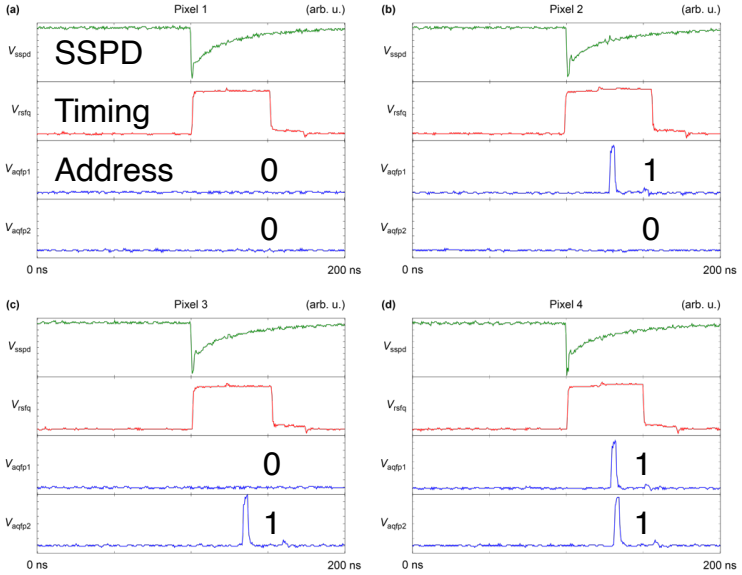
- ✓ AQFP used as an interface for SSPDs to reduce cable #
- ✓ Reduces heat inflow via cables

SSPD array demonstrated using AQFP

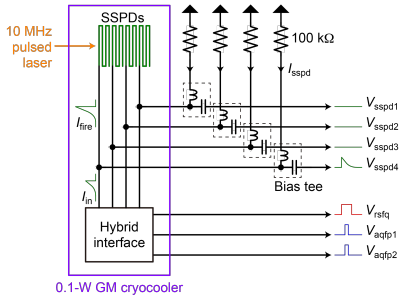
AQFP/RSFQ hybrid interface

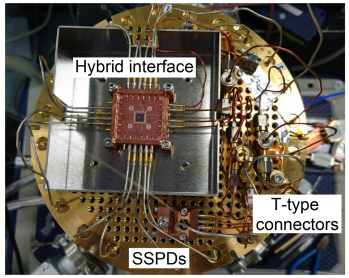


Measurement waveform



Setup using a 0.1-W GM cooler





- Demonstrated a 4-px SSPD array using an AQFP/RSFQ interface
- All pixels read out with low error rates and low timing jitters

N. Takeuchi et al., Opt. Express **28** (2020).

IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

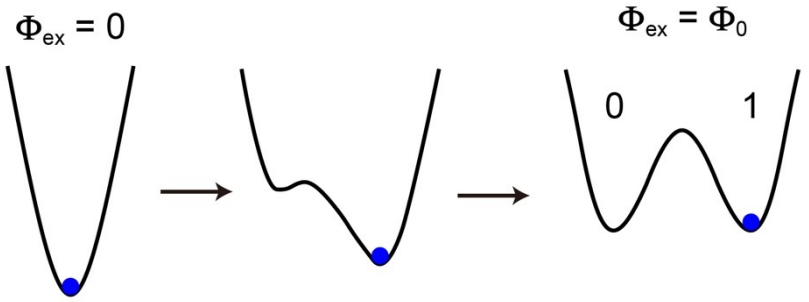
Outline

- Introduction to AQFP logic
  - Adiabatic switching
  - Design methodology
- **Recent progress in AQFP logic**
  - Microprocessor
  - Single-photon image sensor
  - Stochastic electronics

Stochastic operation using thermal noise

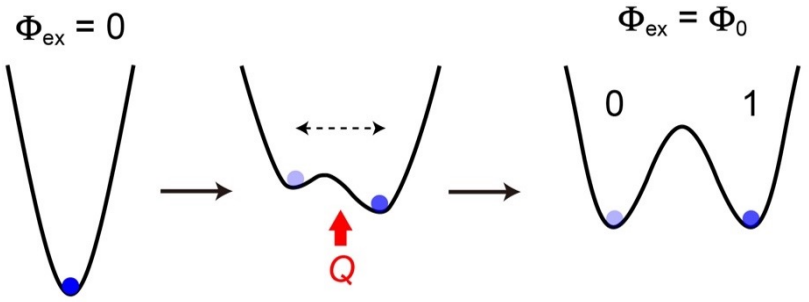
For large input,

- Logic state switches deterministically.
- Entropy change: $\Delta S = 0$



For small input,

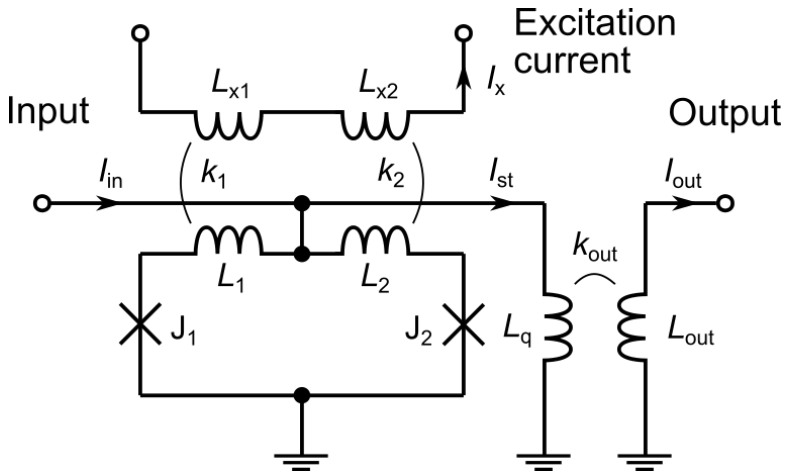
- Logic state switches stochastically.
- Entropy change: $\Delta S = \beta Q > 0$



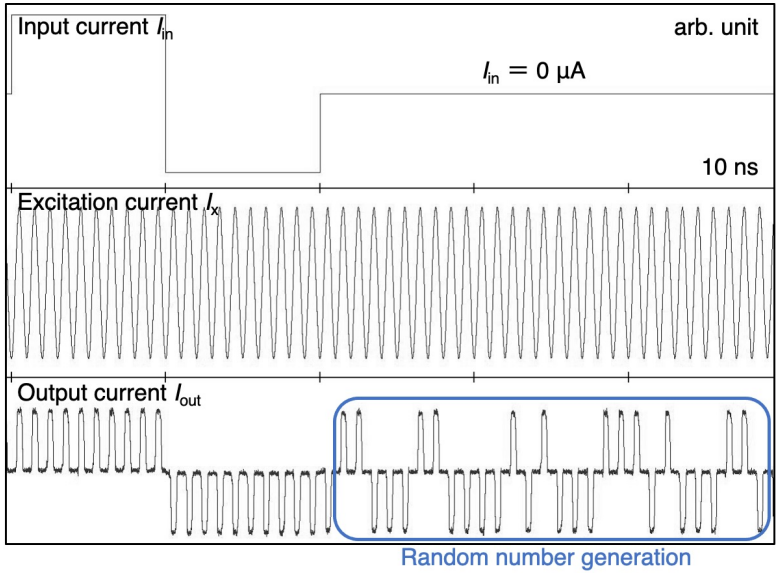
✓ Can implement stochastic logic operation via thermal fluctuations
✓ Entropy change ΔS can be controlled by input current amplitude.

Random number generator

AQFP buffer



Simulation

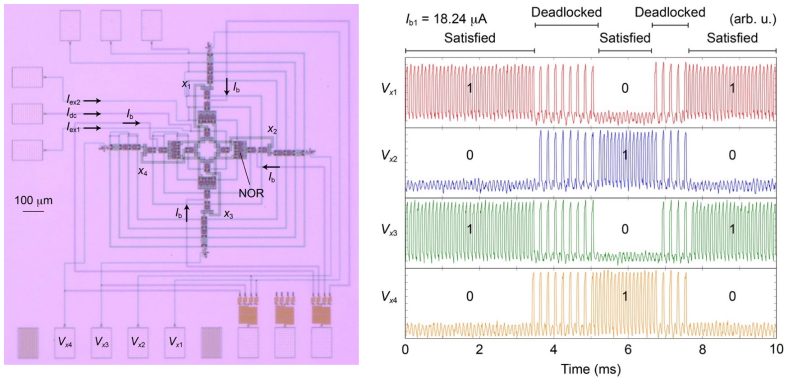


W. Luo et al., IEEE TAS **31** (2021).

An AQFP buffer can be used as a random number generator.

Stochastic local search (SLS) solver

AQFP-based SLS solver

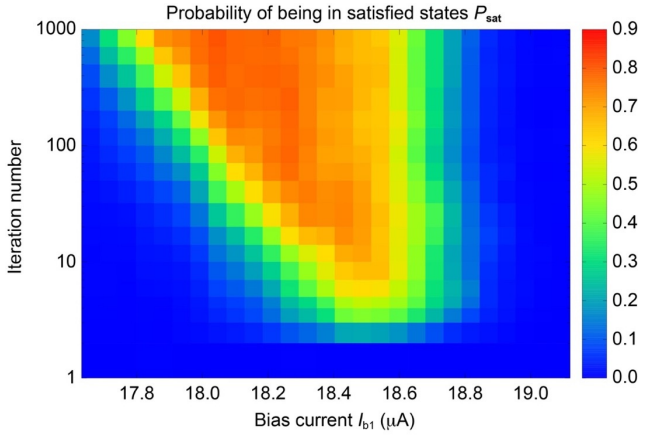


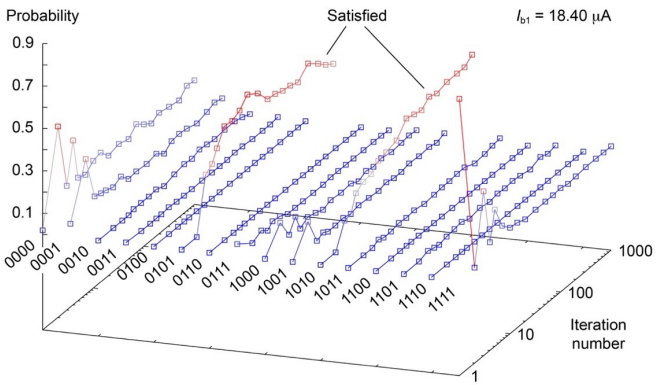
Find a vector $\mathbf{x} = (x_1, x_2, x_3, x_4)$ such that $x_i = \mathrm{NOR}(x_{i-1}, x_{i+1})$.

- Demonstrated SLS for a simple logical constraint sat. problem
- Solutions quickly found with moderate fluctuations

N. Takeuchi et al., Phys. Rev. Appl. **11** (2019).
M. Aono, Jpn. J. Appl. Phys. **59** (2020).

Solution-search speed meas.





IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), May 2022.
Invited presentation ED5-1-INV was given at The International Symposium on Superconductivity, Virtual, December 2, 2021.

Summary

- **AQFP: energy-efficient logic device**
  - ~10^{-21} J per gate at 5 GHz due to adiabatic switching
  - Majority logic, minimal design, ac flux biasing

- **Recent Progress in AQFP**
  - Microprocessor
    - 4-bit prototype demonstrated (ALU tested @ 2.5 GHz)
    - Reversible processor also being developed
  - Single-photon image sensor
    - 4-px system demonstrated
  - Stochastic electronics
    - Random number generator and SLS solver demonstrated

- For more details, see: N. Takeuchi et al., "Adiabatic Quantum-Flux-Parametron: A Tutorial Review," IEICE Trans. Electron., in press.
- Some of the slides were modified or omitted.

Acknowledgements

- The present study was supported by JSPS KAKENHI (Grants No. JP18H01493, No. JP18H05245, and No. JP19H05614).

- The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) at the National Institute of Advanced Industrial Science and Technology (AIST).

- The authors would like to thank C. J. Fourie for providing a 3D inductance extractor, InductEx. The authors would like to thank all the collaborators.