Progress Towards Superconductor Electronics Fabrication Process with Planarized NbN Layers

Sergey K. Tolpygo, Justin Mallek, Vladimir Bolkhovsky, Ravi Rastogi, Evan B. Golden, Terence J. Weir, Leonard M. Johnson, and Mark A. Gouker

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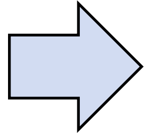
Outline

"All intelligent thoughts have already been thought; what is necessary is only to try to think them again"

Johann Wolfgang von Goethe



- Introduction
- Motivation: why we want NbN layers in the process stack
- Properties of NbN films
  - Critical currents of lines and vias
  - 1-NbN + 7-Nb-layer process SFQ5ee++
  - Inductance and mutual inductance of NbN inductors in the 9-metal-layer process (poster 1EPo2A-8 today)
- Why we do not want all NbN layers in the process stack
- Reconciliation of the requirements: Bilayer NbN/Nb inductors; see also Invited poster 2EPo2F-1 on Tuesday, 2:15 pm – 4:15 pm
- Conclusion

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Presentation 1EOr2C-01 given at Applied Superconductivity Conference, Honolulu, HI, USA, October 24, 2022.
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Tree of Superconductor Digital Electronics

- **SQUID – superconducting quantum interference device**
  - **dc SQUID – dc current, two-junction quantum interferometer (1964)**
  - **rf SQUID – single-junction quantum interferometer using rf excitation (1965)**
- **PQ − Parametric Quantron (1976)**
- **QFP – Quantum Flux Parametron (1985)**
- **RSFQ − Rapid Single Flux Quantum (1985)**
- **nSQUID – negative inductance SQUID (2003)**
- **RQL – Reciprocal Quantum Logic (2011)**
- **ERSFQ − Energy-efficient RSFQ (2011)**
- **AQFP – Adiabatic QFP (2012)**
- **DSFQ – Dynamic SFQ (2018)**

Use Transformers
RSFQ
ERSFQ
DSFQ
AQFP=PQ
QFP
RQL
nSQUID
dc-biased
ac-powered
Adiabatic
nonadiabatic
Adiabatic
dc-biased
ac-powered
Rapid Switching
Parametric Switching
SQUID

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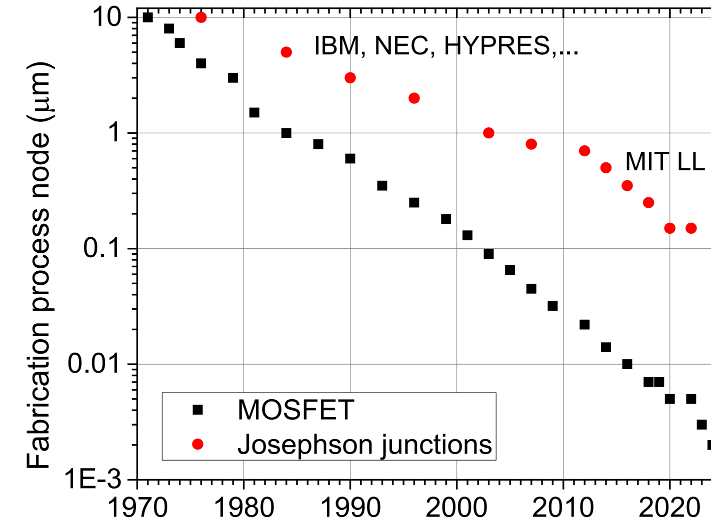
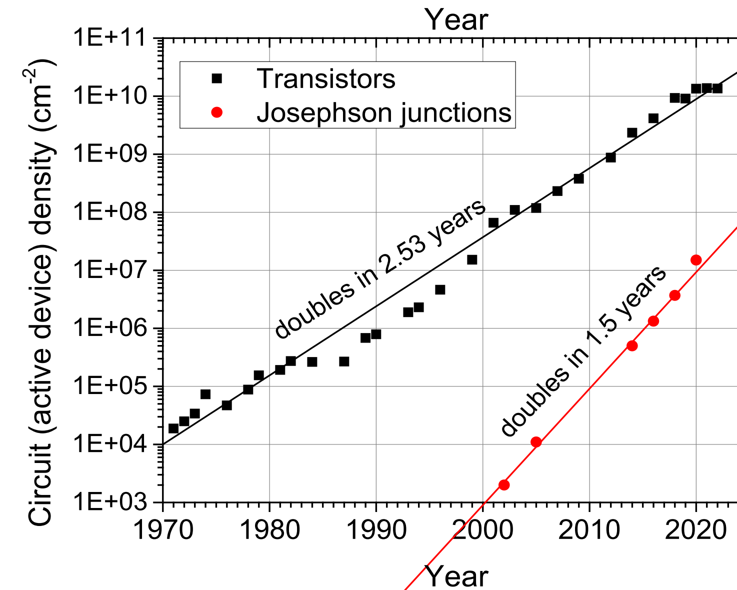
Introduction

- **Superconductor electronics (SCE) has demonstrated**
  - **The highest clock rates (up to ~ 750 GHz in simple devices and ~ 140 GHz in relatively complex circuits)**
  - **The lowest energy dissipation (down to ~ $5k_BT$ per bit)**
- **Main problem – low circuit (device) density and integration scale (device count) of SCE, resulting in low functionality**
  - **150 nm process node at LL vs 3 nm CMOS at TSMC**
  - **1000x lower circuit density of SCE than in CMOS**
- **Example: IARPA Supertools Program SFQ cell library**
  - **The maximum (E)RSFQ circuit density is $5{\cdot}10^5$ JJs/cm^2**
  - **The maximum AQFP circuit density is $4.6{\cdot}10^5$ JJs/cm^2 ($1.6{\cdot}10^5$ JJs/cm^2 in AIST, Japan cell library)**
  - **These densities are almost 5 orders of magnitude lower than in CMOS**





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Integration Scale Limiters

- The main cause of disparity between SCE and CMOS in integration scale is in information encoding
  - In CMOS, information encoded by a presence/absence of a static charge (voltage) on a capacitor
  - In SCE, information encoded by a presence /absence of circulating current (magnetic flux) in a superconducting loop, i.e. by moving charges
  - Obviously, moving charges always take more space than localized charge
- Factors limiting integration scale are related to flux (information) manipulation:
  - Minimal critical current of Josephson junctions (min area) is set by thermal fluctuations (bit errors)
  - Area occupied by superconducting inductors
  - Area occupied by ac excitation (clock) and flux bias transformers
  - Crosstalk between ac-driven power lines and logic cells
  - Critical current of superconducting wires and vias
- Increasing integration scale requires technology solutions commensurate with benefits
  - *E.g.*, do we ultimately need a 120-nm, or 65-nm, or 45 nm technology? (Certainly not 3-nm)
- Materials limitations and fabrication challenges

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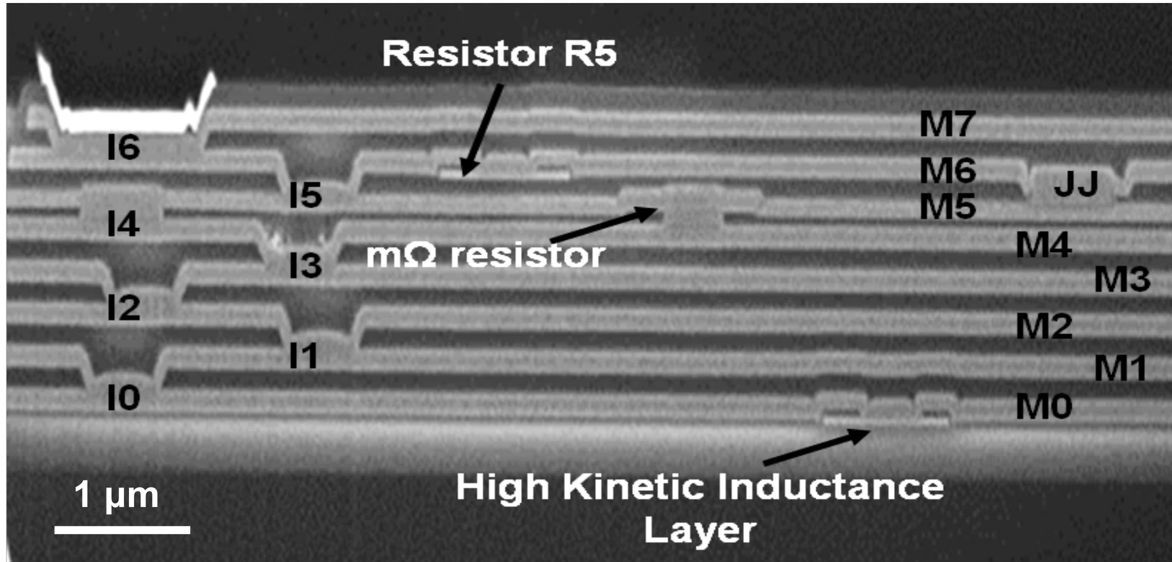
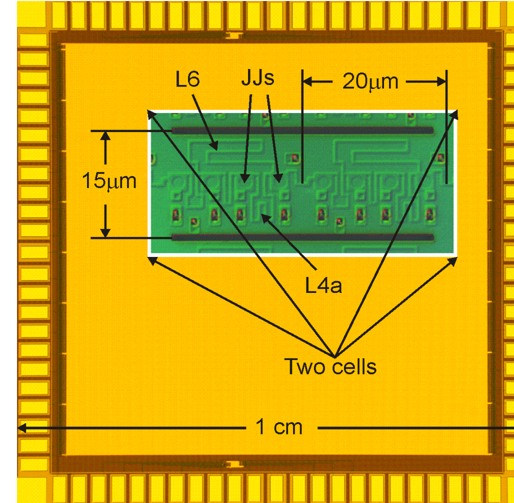
MIT LL Standard Fabrication Node SFQ5ee



Process Features

- 200-mm wafer size
- Junctions: Nb/AlO$_x$-Al/Nb; J_c = 0.1 and 0.2 mA/µm^2
- Min JJ size: 600 nm
- Superconducting layers: 9
  - 8 niobium wiring layers
  - 1 layer of Mo_2N (kinetic inductors for biasing)
  - Resistors: 2 Ω/sq or 6 Ω/sq; mΩ resistor is N/A
- Min inductor linewidth: 350 nm

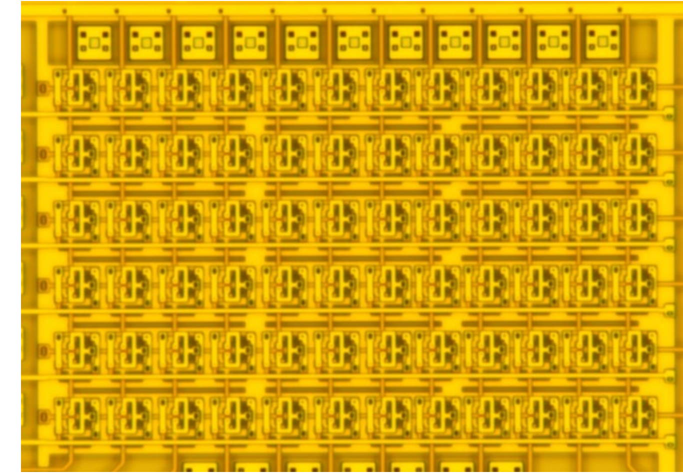
202 Kb Shift Register



- AC-biased shift register: 202,280 bits
- 809,120 shunted 1.25-µm^2 JJs
- Over 4 million inductors
- Circuit density: 1.33M JJs/cm^2
- Integration scale: ≈ Intel's Pentium II, 0.8-µm process, 3.1M transistors on 294 mm^2 chip in 1993

V.K. Semenov, Y.A. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, 1301409, June 2017

JJ RAM



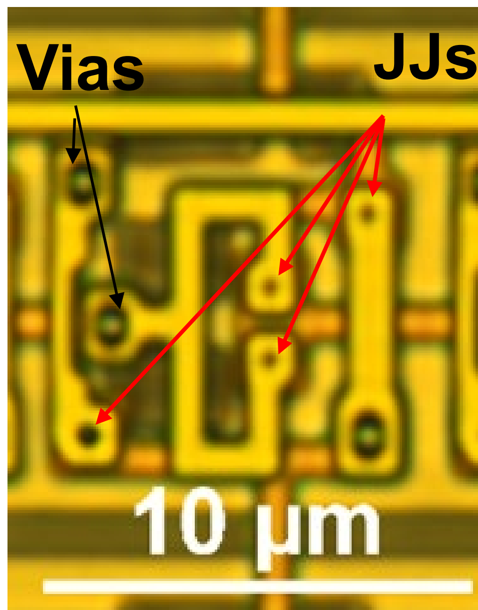
- Array pitch: 9 µm x 12 µm
- Circuits density: 3.7×10^6 JJ/cm^2 record density for SCE
- Functional density: 1 Mb/cm^2
- Technology: self-shunted JJs, *w* = 0.4 µm
  J_c = 0.6 mA/µm^2

V.K. Semenov, Y.A. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, 1302809, Aug. 2019

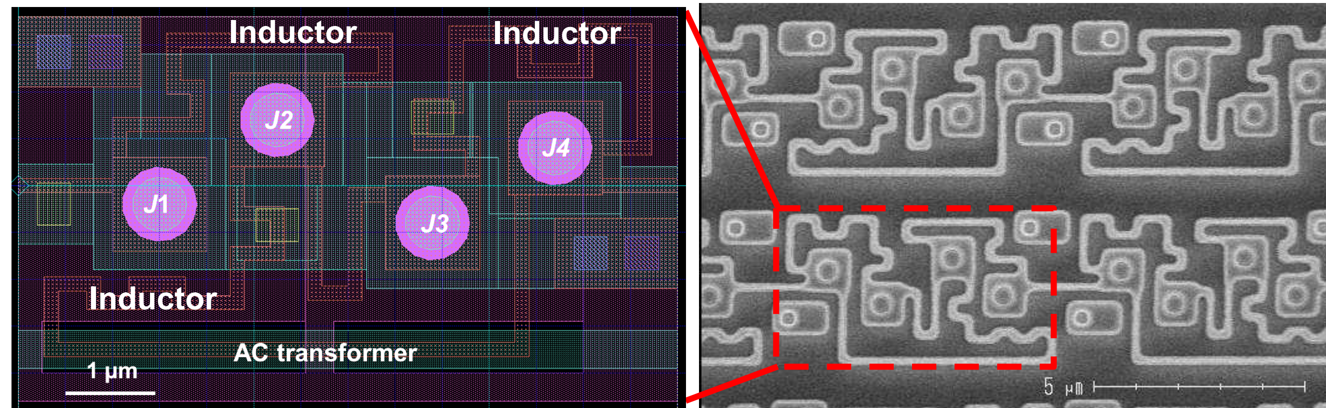
Density of Circuits With Self-Shunted Junctions

- J_c = 600 μA/μm²
- AC-clocked shift registers
  - Cell dimensions: 7 μm x 4 μm
  - Circuit density: 1.3·10⁷ JJ/cm²
  - 150-nm linewidth
  - 2x increase over the 250-nm process

JJ RAM Cell



Shift Register, 150-nm linewidth



Circuit Components in RAM (Shift Register) Cell	Occupied Area (%)
NDRO transformer wires, 0.4 μm linewidth	7.2
Write/Read transformer wires	5.4
Perforations in transformers ground planes for increasing mutual inductance	23 (11)
Flux trapping moats	4 (6)
Josephson junctions	3.5 (11)
Interlayer vias	3 (13)

Most of the circuit area is occupied by inductors and transformers, <11% by Josephson junctions

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Balancing Densities of Inductors and Junctions

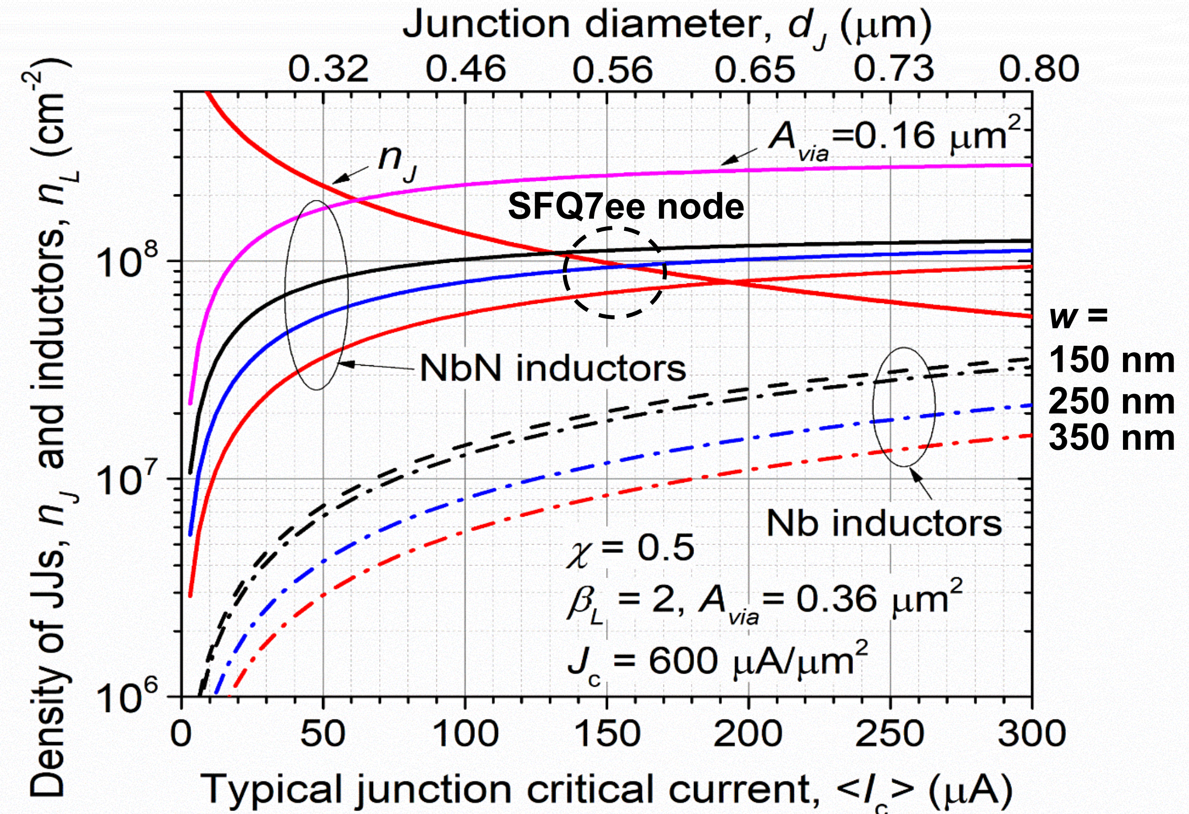
- At J_c ~ 600 μA/μm², Nb/Al-AlO$_x$/Nb junctions are self-shunted and do not require shunt resistors; JJ density:

$$n_J = \chi((\frac{4\langle I_c\rangle}{\pi J_c})^{\frac{1}{2}} + \delta)^{-2} \qquad (1)$$

- χ – fill-factor, <I_c> - critical current of JJs, δ – junction surround
- Density of inductors:

$$n_L = \chi(\frac{\beta_L \Phi_0}{2\pi\langle I_c\rangle\, L_L}(w+s) + A_{via})^{-1} \qquad (2)$$

- Densities of JJs and inductors need to be balanced: one JJ requires one inductor on average
- With Nb inductors, circuits are "starved": not enough inductors
- NbN kinetic inductors allow us to achieve 100 million devices per cm² (10x increase)
- I_c~ 50 μA requires $d \approx 0.3$ μm – the next challenge



Solid curves: NbN stripline inductors with w = 250 nm and thickness, from bottom to top, 200 nm, 100 nm, and 50 nm. The uppermost solid magenta curve corresponds to NbN striplines with w = 150 nm, t = 50 nm, and A_{via}=0.16 μm² in (2)

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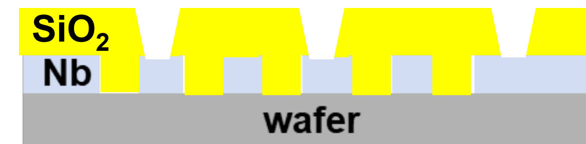
Motivation for Using NbN and Technical Goals

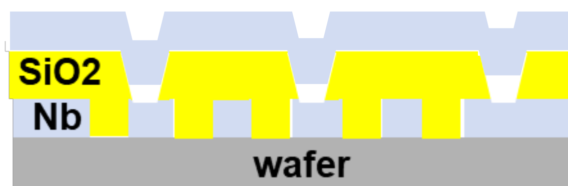
- **Increasing integration scale of SCE by 10x:**
  - **Reduce area of inductor − need 10x higher inductance per unit length than Nb inductors**
  - **Decrease min linewidth and spacing of superconducting wires**
  - **Decrease size of interlayer vias (350 nm now)**
- **Requires replacement of Nb by ? and development of damascene processing of superconducting materials**
- **Energy efficiency advantage of SCE over CMOS reaches ~100x if operating temperature of SCE is increased to ~10 K (may not be achievable)**
  - **Requires implementation of higher-T_c materials, *e.g.*, NbN and NbTiN in the layer stack**
    - **Conformal thin film deposition**
    - **High-density plasma etching**
    - **Chemical mechanical planarization (CMP)**

How processing is done now:

Nb deposition and pattering



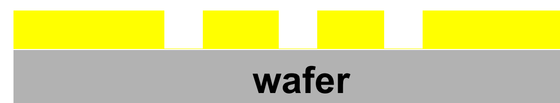
SiO_2 deposition and CMP



Via etch and Nb deposition

Narrow gaps between Nb wires cannot be filled by SiO_2 and high-aspect-ratio via cannot be filled by Nb deposition at low temp.

Our approach – replace Nb and use damascene processing



SiO_2 deposition and pattering trenches in dielectric

NbN or NbTiN conformal PECVD or PEALD and planarization using metal CMP

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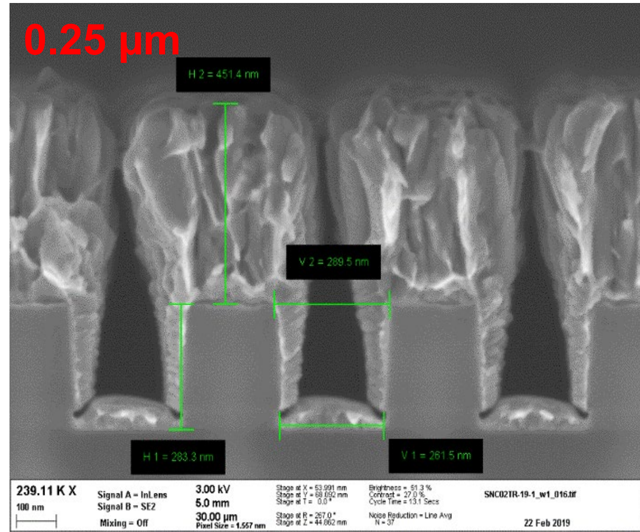
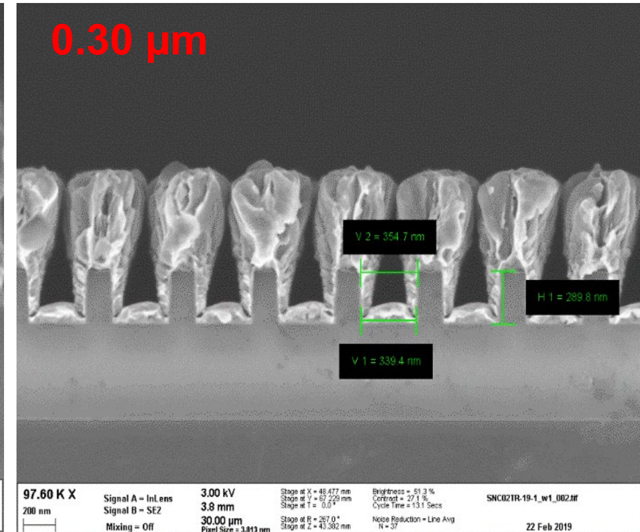
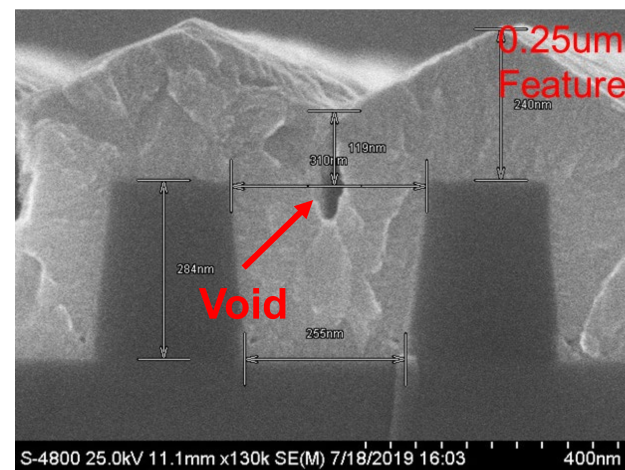
(Not) Filling Narrow Trenches by PVD

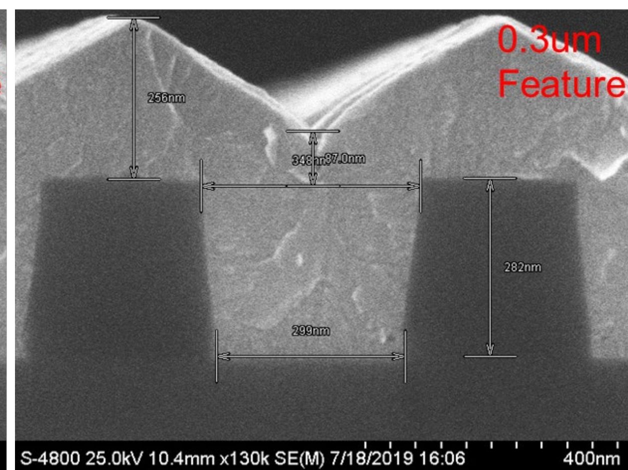
Nb Sputtering in Endura AMAT



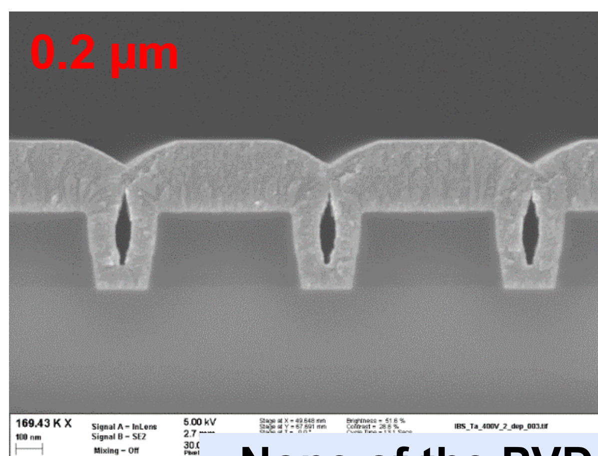


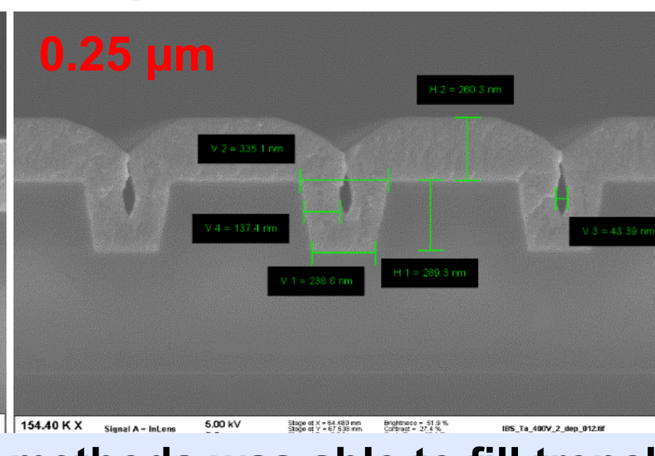
Ionized Metal Plasma, SIP EnCoRe Process (AMAT)



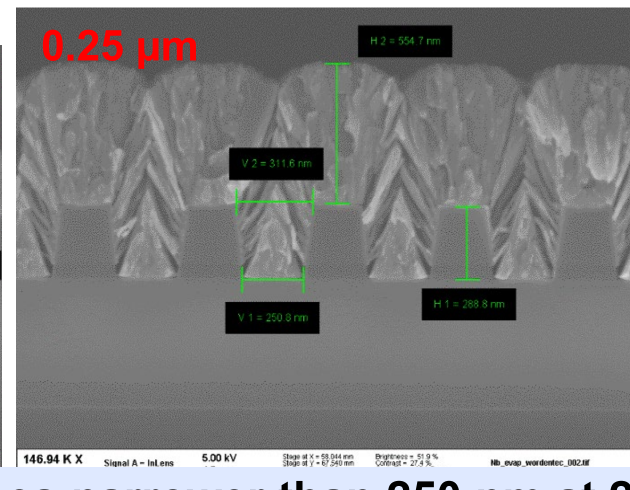


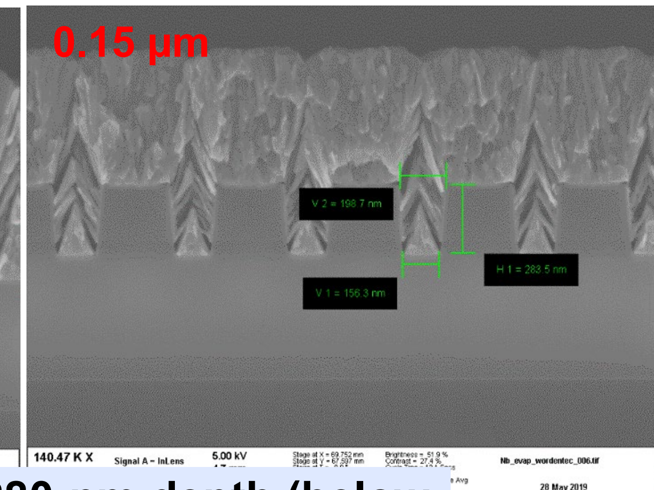
Ion Beam Assisted Deposition





Nb E-beam Evaporation

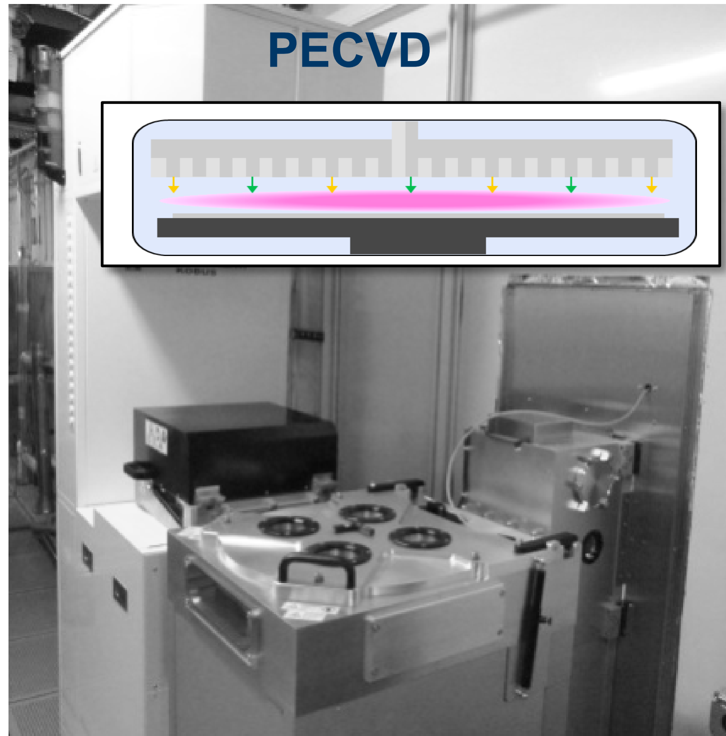


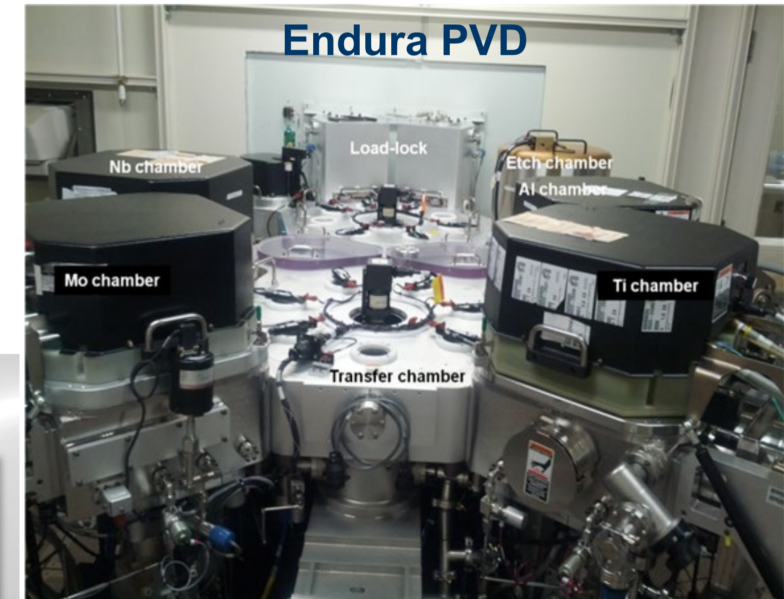


None of the PVD methods was able to fill trenches narrower than 250 nm at 280-nm depth (below 1:1.1 aspect ratio) with Nb at T<200 °C without voids and Nb degradation − need (PE)CVD

NbN and NbTiN Deposition: PVD and PECVD/ALD

- **Reactive sputtering for NbN planar films and filling low aspect ratio via, not for damascene**
  - **N_2/Ar gas, Nb target, magnetron sputtering**
  - **Deposition temperature: 20 °C – 400 °C**
- **Plasma-enhanced chemical vapor deposition (PECVD) for filling high aspect ratio structures and damascene processing**
  - **Utilizes volatile metal-organic precursors to produce highly conformal thin films**
  - **Two on-board precursors for deposition of TiN, NbN, and NbTiN**
  - **H_2, N_2, and NH_3 reactant gasses enable thermal and plasma-based deposition of high quality films**
  - **Uses high-frequency and low-frequency plasma, fast cycling valves and fast matching high frequency to enable ultra short deposition cycles**





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Critical Current of Wires: NbN vs Nb

- **Should be much larger than I_c of JJs, >>100 μA**
- **Fundamental limit to the superconductor critical current density is**

$$j_c^{GL} = \frac{2\sqrt{2}}{3\sqrt{3}} \frac{B_c}{\mu_0 \lambda},$$

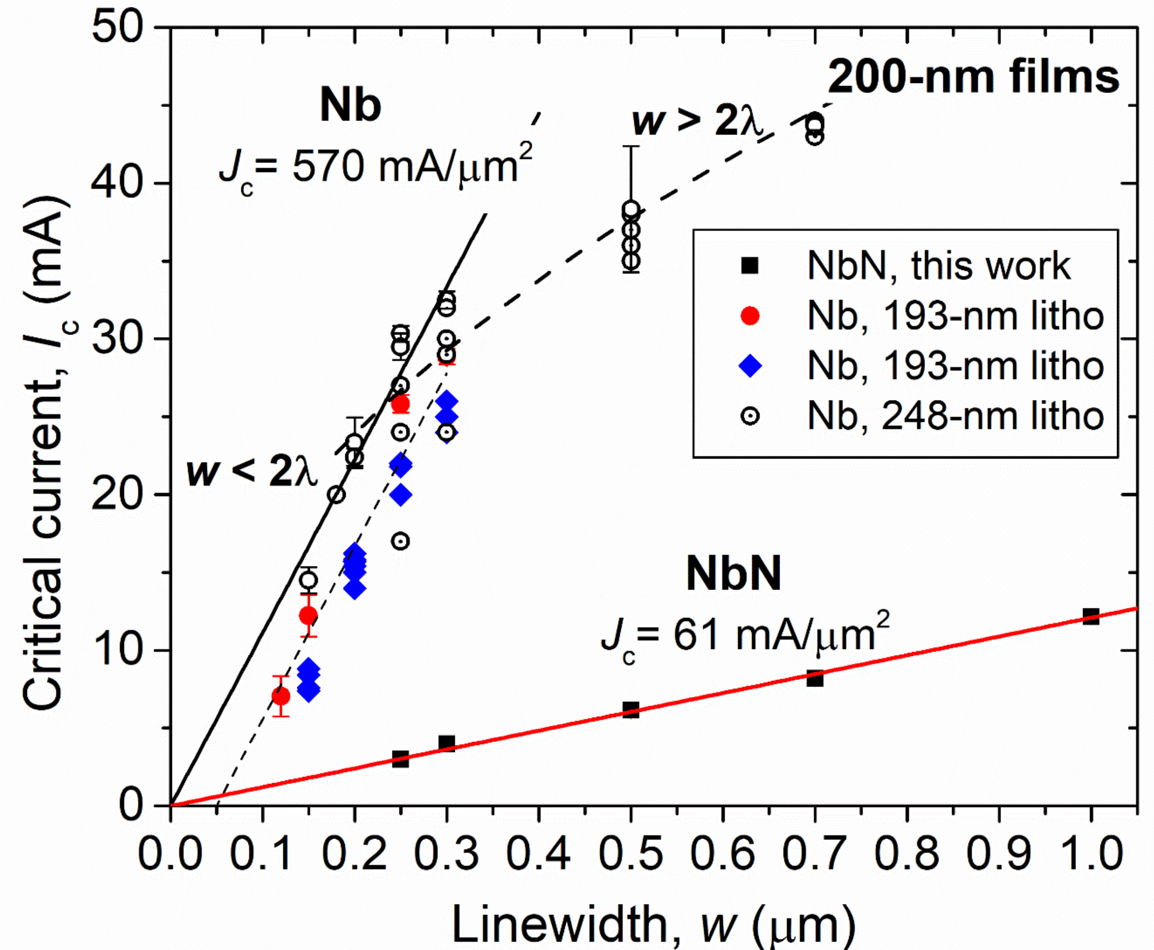
the so-called Ginzburg-Landau (pair-breaking) critical current; B_c - thermodynamic critical magnetic field, λ – penetration depth

- **For Nb: $B_c = 0.122$ T at 4.2 K, λ = 90 nm, giving**

$$j_c^{GL}(4.2\ \mathrm{K}) = 0.59\ \mathrm{A/\mu m^2}$$

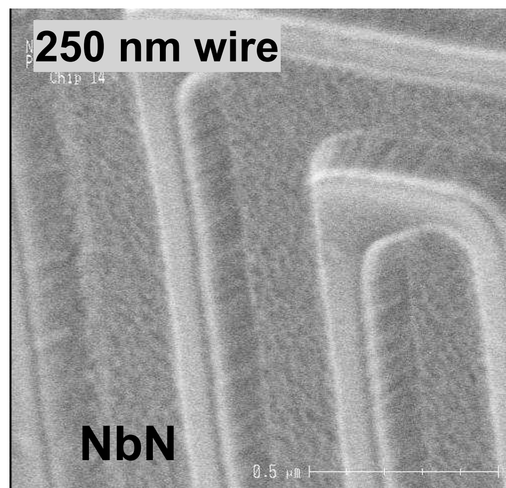
- **NbN: λ = 491 nm is 5.5× larger and j_c is about 9 times lower than in Nb films because of lower density of Cooper pairs and higher resistivity**

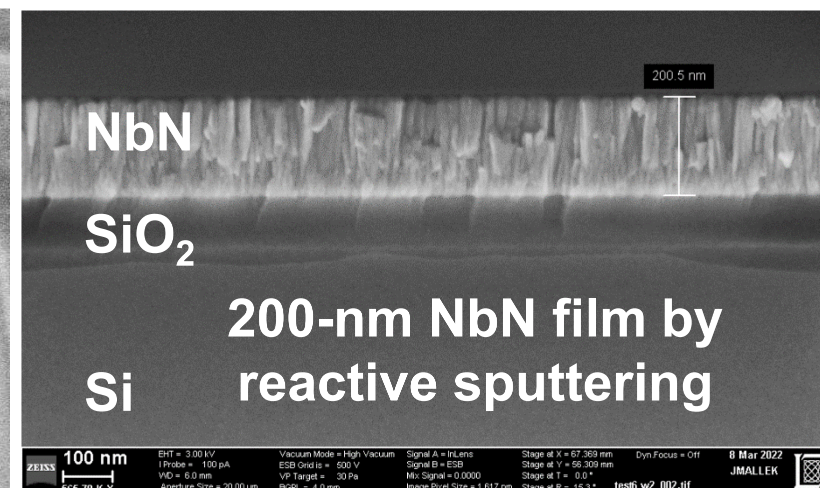
Critical current of superconductors is inversely proportional to their kinetic inductance



Characterization of Reactively Sputtered NbN Films

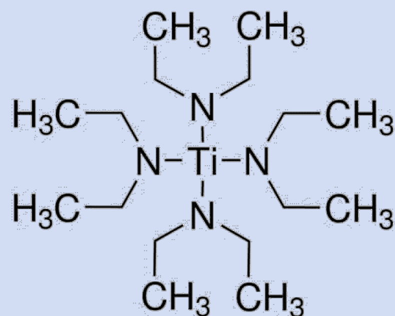
- T_c of PVD NbN films is up to 16.5 K
- Demonstrated superconducting vias and hundreds of 1800-via chains between two NbN layers (M1 and M2) and between NbN and Nb layers
- Investigated stability of NbN films and patterned films imbedded in SiO_2 up to 400 °C:
  - Critical temperature, T_c
  - Critical currents of patterned lines, I_c
  - Critical current of NbN vias
- Only minor degradation of NbN film have been detected at high deposition temperatures of SiO_2 using TEOS or SiH_4 PECVD
  - Similar Nb structures *would not be superconducting under the same conditions*
- Residual stress in NbN films was adjusted to compressive ~ −300 MPa

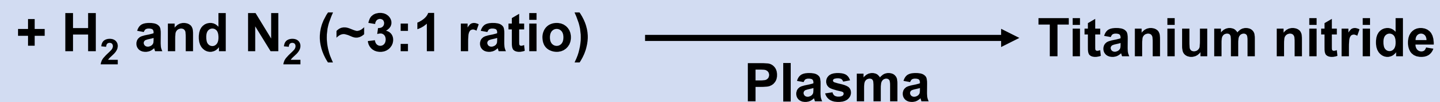




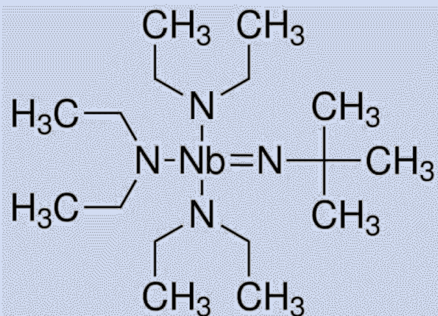
Parameter	SiO_2 deposition at 150 °C	SiO_2 deposition at 400 °C
T_c (K)	15.9	15.5
I_c of 0.7-µm wires (mA)	5.2	4.2
I_c of 0.7-µm vias (mA)	7.0	6.1

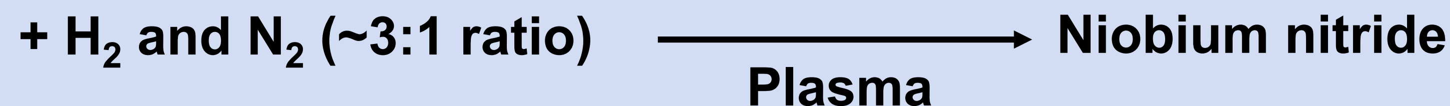
PECVD Process for TiN and NbN





Tetrakis(diethylamino)titanium(IV)
TDEAT





Tris(diethylamido)(tert-butylimido)niobium(V)
TBTDEN

Deposition temperature 150 °C − 400 °C

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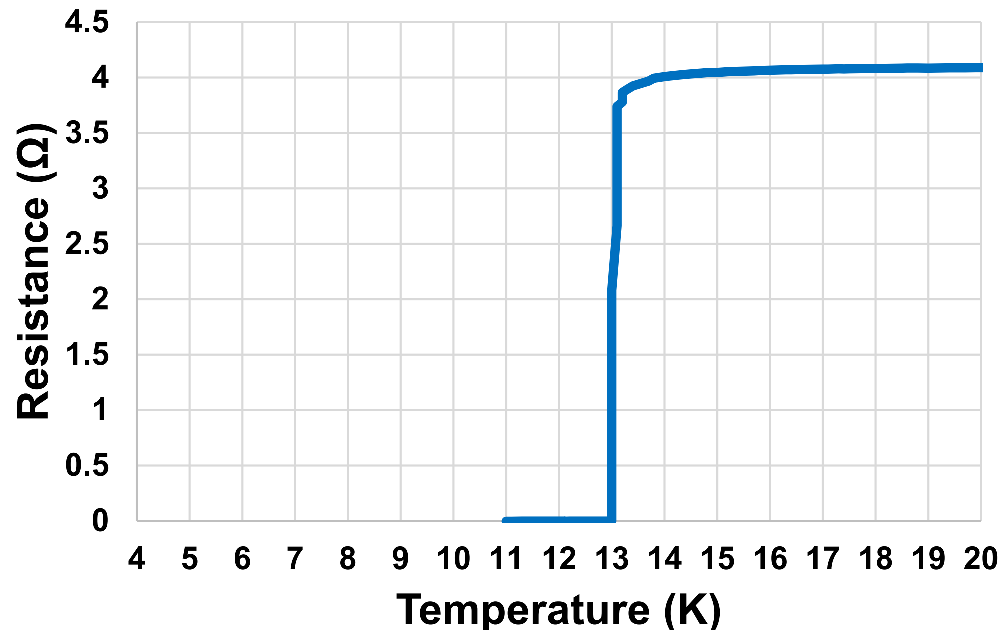
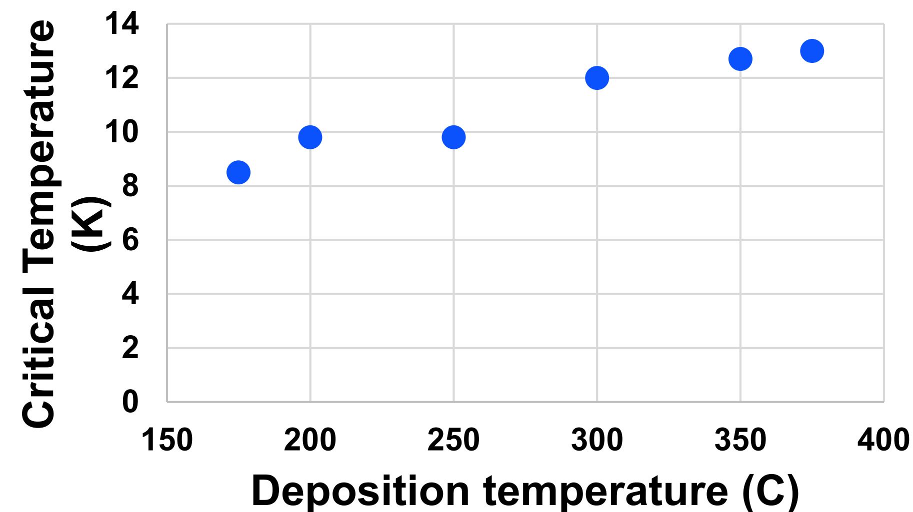
Superconducting Properties of PECVD NbN Films

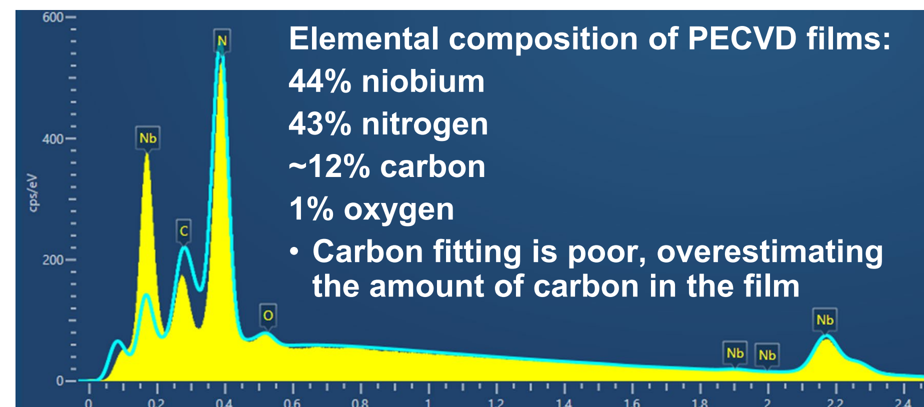
Superconducting transition of PECV-deposited NbN film



Critical temperatures of PECVD NbN films



- T_c of up to 13 K has been obtained in PECVD NbN films
- Up to 16.5 K using reactive sputtering
- $R(T)$ dependence in the range from T_c to 300 K indicates good quality of PECVD NbN



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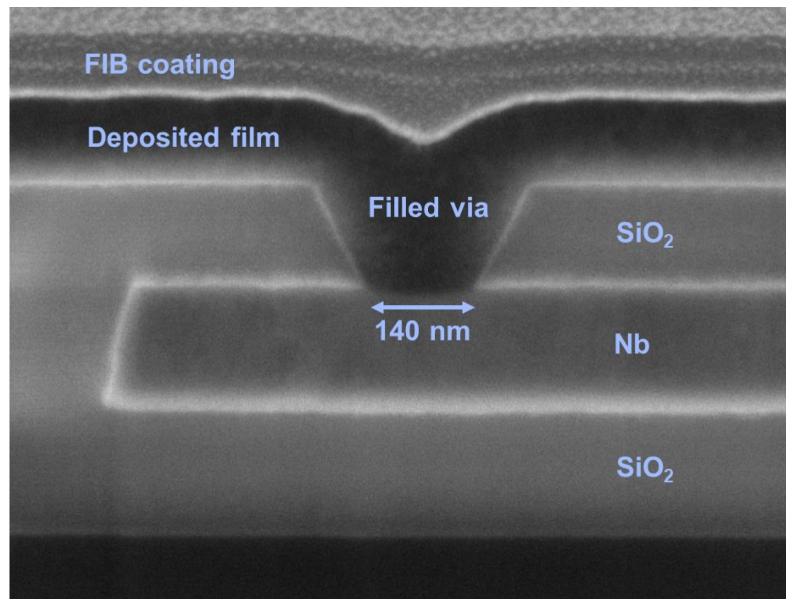
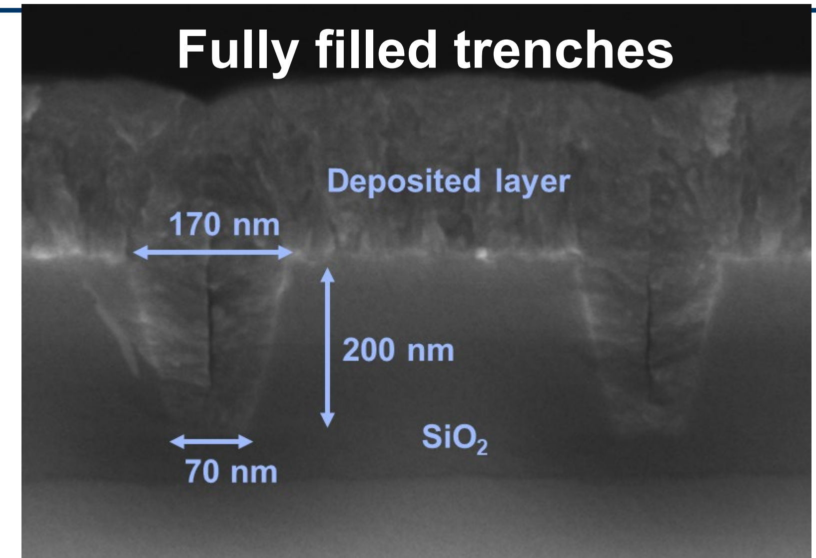
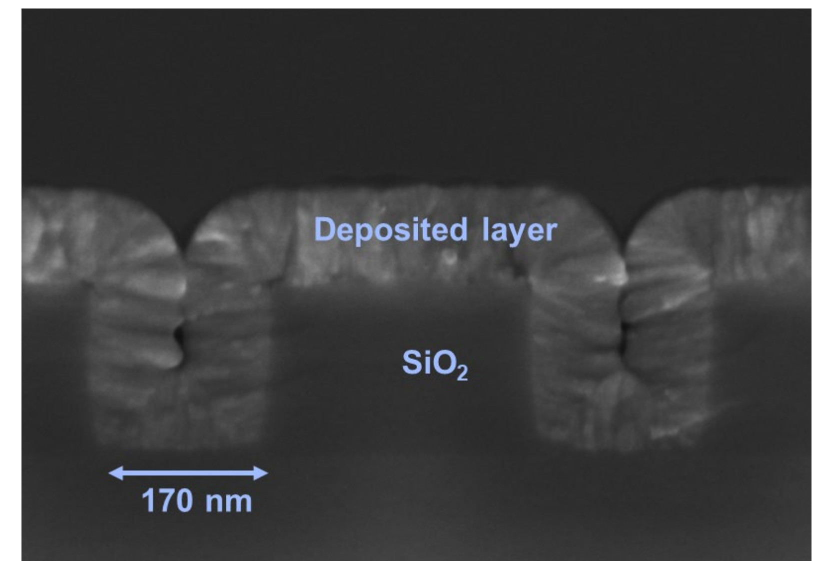
Conformal PECVD of NbN in Narrow Trenches and Vias

- Developed highly conformal via fill for via size sizes below 200 nm, using sloped sidewalls
- Additional recipe development may lead to fully planarized films over filled via
- A planarized deposition process may eliminate the need for chemical mechanical planarization (CMP)
- Demonstrated filling narrow trenches with minimal seaming and nearly planar overgrowth using PECVD







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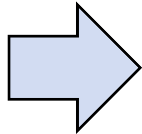
- Motivation: why we want NbN layers in the process stack
- Properties of NbN films
  - Critical currents of lines and vias
  - 1-NbN + 7-Nb-layer process SFQ5ee++
  - Inductance and mutual inductance of NbN inductors in the 9-metal-layer process (poster 1EPo2A-8 today)
- Why we do not want all NbN layers in the process stack
- Reconciliation of the requirements: Bilayer NbN/Nb inductors; see also Invited poster 2EPo2F-1 on Tuesday, 2:15 pm – 4:15 pm
- Conclusion



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1NbN+7Nb-layer Process SFQ5ee++

Pad
Pad Opening, PO
Pad
M7
M6
M5
M4
M3
M2
M1
M0
I6
C5J
C5R
I5
NbN/Nb
R5
J5
J5
R5
J5
I4
I3
I2
I1
I0
C0
Nb
L0
Wafer

M6: NbN or NbN/Nb bilayer, 200 nm

M0-M4, M7: Nb layers, 200 nm

M5: Nb,150 nm

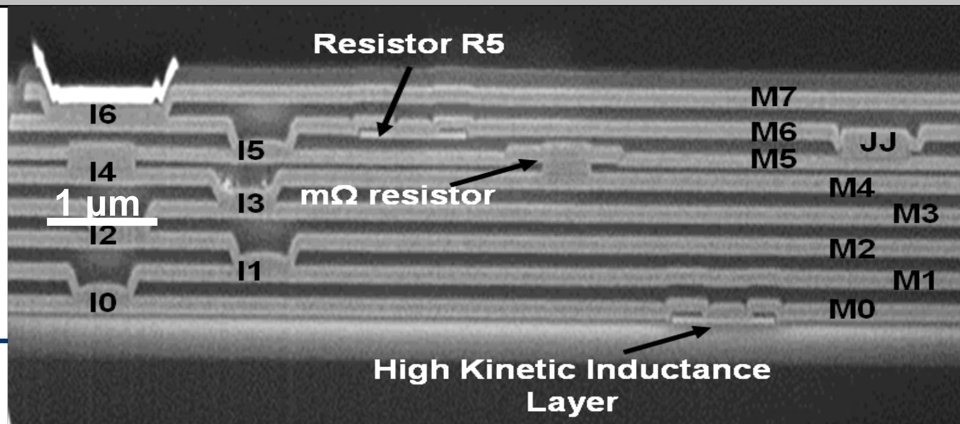
R5: Mo or MoN_x resistor, 40 nm

L0: Mo_2N kinetic inductor, 40 nm

Pad: Nb/Pt/Au

I0-I4, I6, I7: vias in SiO_2 interlayer dielectric, 200 nm

I5: 270 nm



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Self- and Mutual Inductance Structures Measured

- NbN layer with T_c ~ 16 K and 200-nm thickness was incorporated instead of Nb layer M6 in the SFQ5ee process with Nb/Al-AlO$_x$/Nb junctions
- Inductance of NbN inductors was measured using SQUID-based integrated circuits for inductance extraction
- Inductors studied:
  - a) microstrips M6aM4
  - b) inverted microstrips M6bM7
  - c) mutual inductance of microstrip inductors M6aM4 and M7aM4; p_x is distance between geometrical centers of the signal traces in the horizontal, *x*-direction
  - d) stripline inductors M6aM4bM7
  - e) mutual inductance of striplines M5aM4bM7 and M6aM4bM7; p_x was varied

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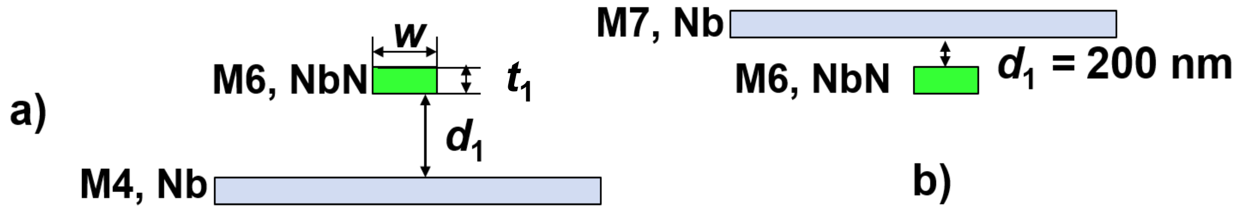
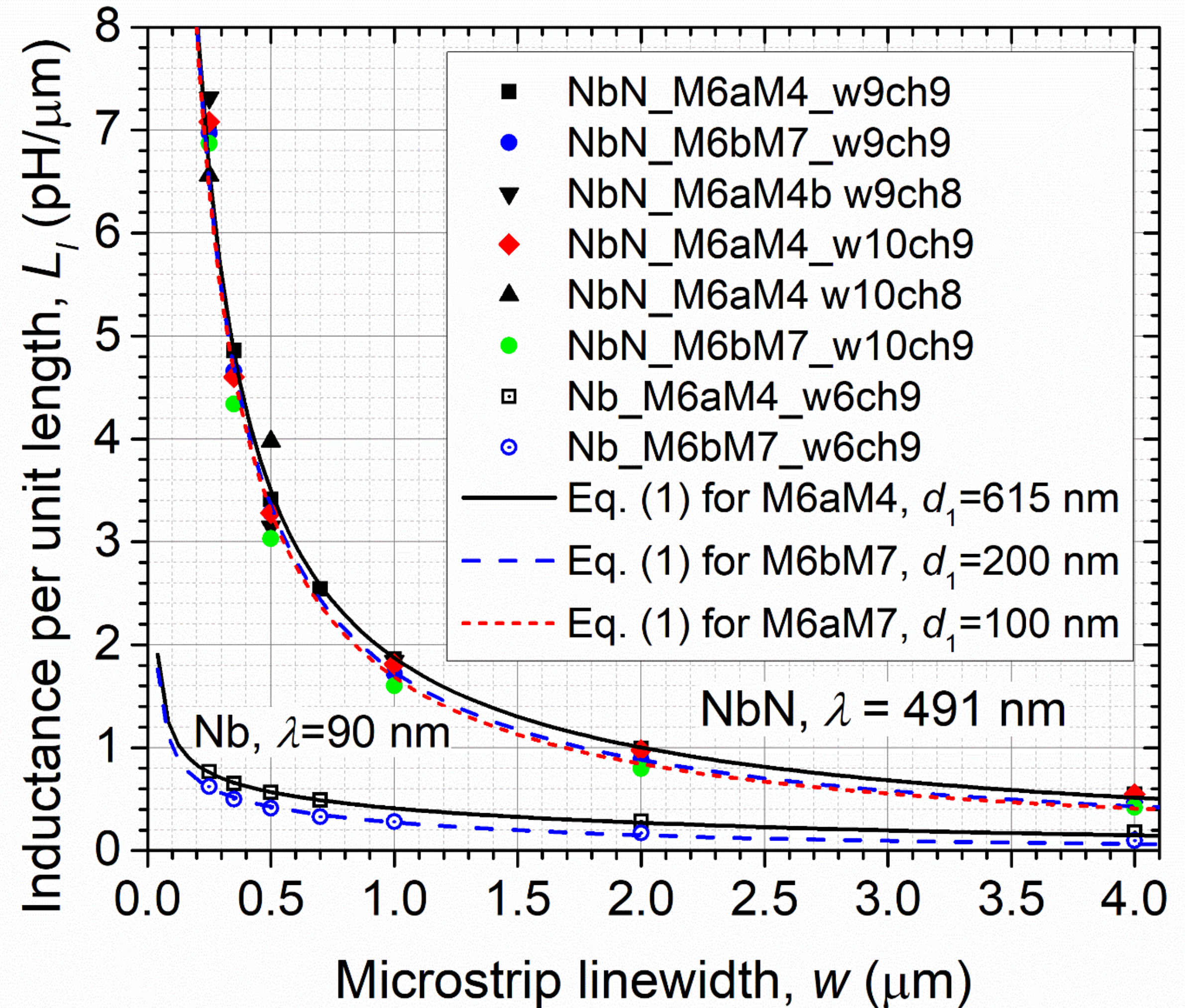
Inductance of NbN Microstrips with Nb Ground Plane



- **Inductance of superconducting microstrips per unit lengths is given by [1]**

$$L_l = \frac{\mu\mu_0}{4\pi} \ln\left[1 + \frac{4\left(d_1 + \frac{t_1}{2} + \lambda\right)^2}{0.2235^2 (w + t_1)^2}\right] + \frac{\mu_0 \lambda_1^2}{t_1 w}, \qquad (1)$$

- **Solid and dash curves are fits to (1), giving magnetic field penetration depth in NbN λ = 491 ± 5 nm at magnetic field penetration depth in Nb ground planes of $\lambda = 90$ nm; see the two bottom curves for Nb**
- **Short dash magenta curve is also a fit to (1) but at a different dielectric thickness $d_1 = 100$ nm between the layers M6 and M7 on w10**
- **NbN kinetic inductance L_K = 1.51 pH/sq**



[1] S.K. Tolpygo, E.B. Golden, T. J. Weir, and V. Bolkhovsky, *IEEE TAS*, vol. 32, no. 5, Aug. 2022, Art no. 1400331

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Inductance of NbN Striplines with Nb Ground Planes

- **Superconducting stripline inductance is given in [1]:**

$$L_l = \frac{\mu\mu_0}{4\pi}\ln\left(1+\frac{\sin^2\frac{\pi\left(d_1+\frac{t_1}{2}+\lambda\right)}{H+2\lambda}}{\sinh^2\frac{\pi r_{eq}}{2(H+2\lambda)}}\right)+\frac{\mu_0}{8\pi}+\frac{\mu_0\lambda_1^2}{t_1 w}, \qquad (2)$$

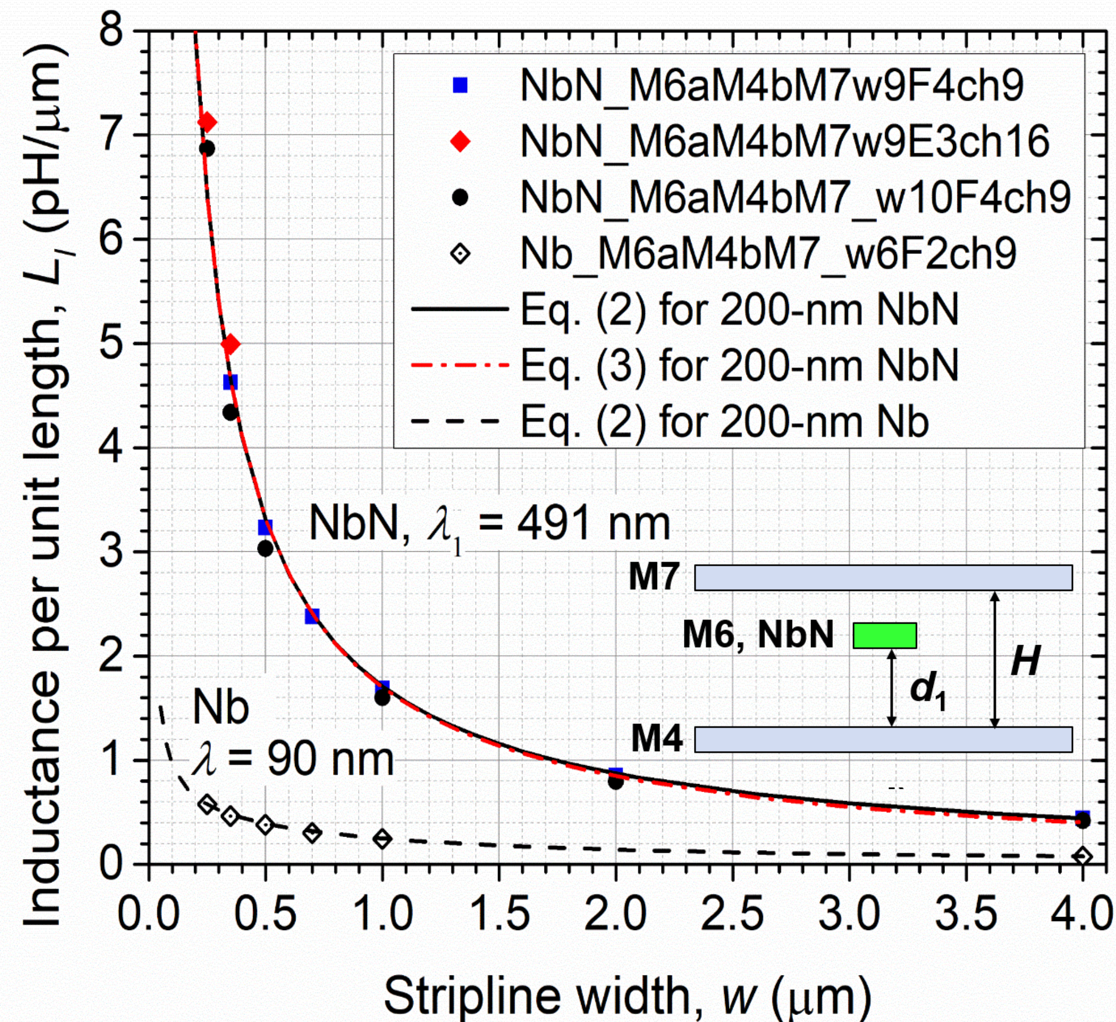
where r_{eq} is the equivalent radius of the rectangular cross section

- **Stripline inductance can also be obtained using Maxwell's geometric mean distance method, calculating self-inductance as mutual inductance of the rectangular wire with itself placed at the geometrical mean distance:**

$$L_l = \frac{\mu\mu_0}{4\pi}\ln\left(1+\frac{\sin^2\frac{\pi\left(d_1+\frac{t_1}{2}+\lambda\right)}{H+2\lambda}}{\sinh^2\frac{0.2235\pi(w+t)}{2(H+2\lambda)}}\right)+\frac{\mu_0\lambda_1^2}{t_1 w}, \qquad (3)$$

where 0.2235(w+t_1) is Maxwell's geometrical mean distance for a rectangular cross section

- **NbN kinetic inductance: L_K = 1.51 pH/sq**



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Mutual Inductance of NbN and Nb Microstrips

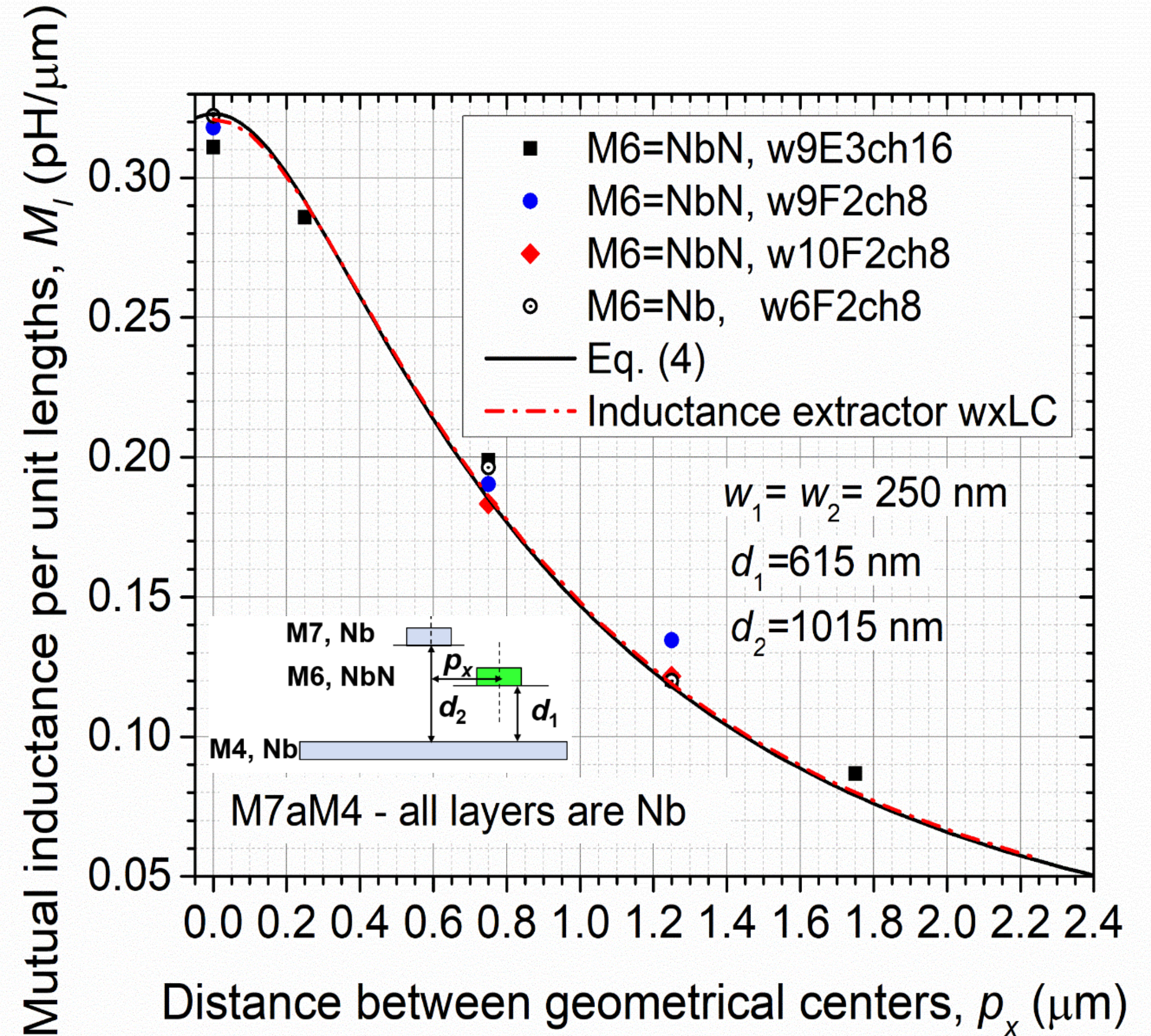
- **Mutual inductance of two superconducting microstrips with thicknesses t_1 and t_2, dielectric thicknesses d_1 and d_2, and linewidths $w_1, w_2 \lesssim |d_2 - d_1|$ is given in [1] by**

$$M_l = \frac{\mu\mu_0}{4\pi} \ln\left[1 + \frac{4\left(d_1+\lambda+\frac{t_1}{2}\right)\cdot\left(d_2+\lambda+\frac{t_2}{2}\right)}{p_x^2+(d_2-d_1+\frac{t_2-t_1}{2})^2}\right] \quad (4)$$

- **Mutual inductance per unit length between NbN and Nb microstrips is the same as between two Nb microstrips (open dots in the Figure)**
- **Solid black curve is (4) at magnetic field penetration depth in the Nb ground plane λ =90 nm and d_1 =615 nm, and d_2 =1015 nm. Red dash-dot curve shows numerical simulation using inductance extractor wxLC**
- **However, mutual coupling constant**

$$\kappa = \frac{M_{12}}{(L_1 L_2)^{1/2}}$$

diminishes with increasing kinetic inductance



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Mutual Inductance of NbN and Nb Striplines

- **Mutual inductance of two superconducting striplines with thicknesses t_1 and t_2, dielectric thicknesses d_1 and d_2, and linewidths $w_1, w_2 \lesssim |d_2 - d_1|$ is given in [1] by**

$$M_l = \frac{\mu\mu_0}{4\pi} \ln \frac{\cosh\frac{\pi p_x}{H+2\lambda} - \cos\frac{\pi(d_1+d_2+t_1+t_2+2\lambda)}{H+2\lambda}}{\cosh\frac{\pi p_x}{H+2\lambda} - \cos\frac{\pi(d_2-d_1+t_2-t_1)}{H+2\lambda}} \quad (5)$$

- **Mutual inductance of NbN and Nb striplines is the same as between Nb striplines**

- **However, the coupling constant $\kappa = \frac{M_{12}}{(L_1 L_2)^{1/2}}$ diminishes because of kinetic inductance**

Mutual inductance per unit lengths, M_l (pH/μm)

0.00, 0.02, 0.04, 0.06, 0.08, 0.10, 0.12

Distance between geometrical centers, p_x (μm)

0.00, 0.25, 0.50, 0.75, 1.00, 1.25, 1.50, 1.75, 2.00

■ M6=NbN, M5=Nb, w9E3ch16

— Eq. (5)

$w_1 = w_2 = 250$ nm

$t_1 = 135$ nm (M5)

$t_2 = 200$ nm (M6)

$d_1 = 200$ nm

$d_2 = 615$ nm

$H = 1015$ nm

M7, Nb

M6, NbN

M5, Nb

M4, Nb

p_x

H

d_1

d_2

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Why We Do Not Want Only NbN Layers in the Stack

- High penetration depth >0.3 μm makes NbN and NbTiN unsuitable for circuit ground (sky) planes:
  - Very poor interlayer shielding
  - Very high parasitic mutual inductance (intralayer coupling) between inductors and logic cells
  - To provide the same shielding as Nb, thickness of NbN ground plane layers should be ~ 1.1 μm
- High kinetic inductance decreases length (and area) of inductors – Good for circuit density
- However, short inductors have low mutual inductance – Good for reducing parasitic crosstalk. Bad for AC power and flux bias transformers
- Kinetic inductors are not suitable for ac power and data PTLs
  - Make PTL impedance too high, $Z = (L/C)^{1/2}$
  - At the same linewidth, Z of PTLs with NbN signal traces is 3x higher than Z of Nb PTLs
  - Or need 3x wider PTLs
- Inductance of vias filled by NbN is >> of Nb vias and no longer negligible
- Therefore, we need a right mix of NbN and Nb layers: Nb for ground planes, PTLs, and transformers; NbN for cell inductors

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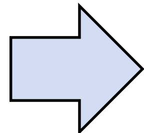
Outline

"It makes no good to point out the failures without showing at the same time the remedy to address them"

Johann Wolfgang von Goethe

- **Introduction**
- **Motivation for using NbN in the process stack**
- **Properties of NbN films**
  - **Critical currents of lines and vias**
  - **1-NbN + 7-Nb-layer process SFQ5ee++**
  - **Inductance and mutual inductance of NbN inductors in the 9-metal process layer stack**
- **Why we do not want all NbN layers in the process stack**



- **Reconciliation of the requirements: Bilayer NbN/Nb inductors**
- **Conclusion**

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Reconciliation: Bilayer NbN/Nb Inductors and Transformers

- We have developed and implemented bilayers of magnetic (geometrical) inductors on top of kinetic inductors: NbN/Nb bilayers with 100 nm /100 nm thicknesses (variable process / circuit-design-informed parameter)
- Since λ_{NbN}>>λ_{Nb}, bilayer inductance is the same as of 100-nm Nb layer – can be used for low-inductance interconnects, PTLs, vias, *etc*.
- Mutual inductance of 200-nm-thick bilayer strips is the same as of 200-nm Nb strips – can be used for transformers
- Selective patterning of the top Nb layer opens access to the bottom NbN kinetic inductance layer
- Using two photolithography steps and two etch steps (two-step pattering) creates variable thickness and variable (if needed) width inductors
- Gigantic inductance range: from 0.3 pH/µm (like Nb geometrical inductors) to ~ 30 pH/µm (like NbN kinetic inductors)

NbN/Nb bilayers as inductor layers

S.K Tolpygo *et al*., "System and method for providing multiconductive layer metallic interconnect for superconducting integrated circuits," US Patent # 8437818

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Conclusion

- **We have developed conformal deposition and CMP of superconducting NbN using PECVD from metalorganic precursors for damascence processing of vias and narrow trenches**
- **We incorporated NbN layer and NbN/Nb bilayer into the full layer stack with Nb layers as a dedicated inductor layer**
- **Self- and mutual inductance of NbN inductors with Nb ground planes was studied to provide input data for circuit design**
- **Magnetic field penetration depth in 200-nm thick NbN films deposited by reactive sputtering was determined to be 491 ± 5 nm at 4.2 K, giving kinetic inductance of 1.51 pH/sq**
- **Mutual inductance between NbN and Nb, between NbN and NbN microstrips and striplines was found to be the same as for Nb structures with the same geometrical dimensions and placement between the ground plane, as predicted**
- **Implementation of kinetic inductors in logic (and memory) cells allows for a 10x increase in the integration scale (device number density) of SCE**
- **We welcome suggestions from the community on other useful features to incorporate in the next node of our fabrication process**

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WE STAND WITH UKRAINE

Thank you very much for your attention

Questions?

"If you want a wise answer, ask a reasonable question"

– Johann Wolfgang von Goethe