22nd Biennial U.S. Workshop on Superconductor Electronics, Devices, Circuits, and Systems Hotel Santa Fe, Santa Fe, NM 87505, April 6, 2025 - April 10, 2025



## Current Status of Superconducting Electronics (SCE) in Japan

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## Outline

- Japan's national projects on quantum computing
- Superconducting electronics projects related to quantum computing
- Superconducting digital electronics projects

## Japan's National Projects on Quantum Computers

Moonshot R&D Program 6



- Japan Science and Technology Agency
- Title: Realization of a fault-tolerant universal quantum computer by 2050
- Sponsor: Cabinet Office, Japan Science and Technology Agency (JST)
- Duration: Phase 1: 2020-2025, Phase 2: 2026-2030
- Institutions: NEC, Hitachi, AIST, RIKEN, NICT, NTT, U Tokyo, Osaka U, YNU etc.
- NEDO Post-5G Project (NEDO New Energy and Industrial Technology Development Organization



- Title: Research and development of quantum computing and Ising computing systems
- Sponsor: New Energy and Industrial Technology Development Organization (NEDO)
- Duration: 2018-2027
- Institutions: AIST, NEC, Toshiba, NII, Waseda U, TIT, YNU etc.
- Q-LEAP (JST) Japan Science and Technology Agency

- Title: Quantum Leap Flagship Program (Q-LEAP)
- Sponsor: MEXT, JST
- Duration: 2018-2029
- Institutions: RIKEN, U Tokyo, NII, Osaka U, etc.

## Moonshot R&D Program 6

 Aim: Development of basic technologies for a fault-tolerant universal quantum computer.

Research Area	Details
Hardware	Superconducting qubits, spin qubits, photonics, neutral atoms
Error Correction	Surface codes, topological codes, cat codes
Algorithms	Applications in chemistry, optimization, machine learning
System Integration	Scalable quantum processor design, cryogenic electronics, quantum control infrastructure



## Development of Integration Technologies for Superconducting Quantum Circuits

- Reader: Tsuyoshi Yamamoto (NEC)
- Goal: Realize a large-scale superconducting quantum computer by developing key hardware technologies.
- Approach:
  - Solve wiring bottlenecks using cryo electronics (e.g., SFQ circuits, flip-chip interconnects)
  - Reduce hardware demands via high-coherence qubits and bosonic error-correcting codes



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## beyond NISQ



https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf

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### Cryo-electronics

#### Cryo-CMOS, SFQ, AQFP etc.

 Potentially reduces the number of physical interconnects (coaxial lines) between the quantum-classical interface and room-temperature electronics



https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf



#### High-speed digital LSIs using quantized magnetic flux

- Voltage pulse-driven logic
- ✤ 10+ GHz, low-power operation
- Transmission line interconnects

https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf

K. K. Likharev and V. K. Semenov, IEEE Trans. Appl. Supercond.  $\boldsymbol{1}$  (1991).

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#### IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 59, May 2025. Presentation given at 22nd Biennial U.S. Workshop on Superconductor Electronics, Devices, Circuits, and Systems Santa Fe, New Mexico, April 6-10, 2025.

T. Yamamoto

#### Selection of Critical Current Density $(J_c)$



https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf

### 1:2 Demux (Demultiplexer) Demo

 Demux forwards the input signal (SFQ pulse trains) to one of the outputs based on the control signals.



## Demonstration of current-controlled 1:2 demux



https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf

## Generation of Kerr cat qubit

Wigner tomography



https://www.jst.go.jp/moonshot/sympo/20240327/pdf/05\_yamamoto\_tsuyoshi.pdf

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## **NEDO – Post-5G Project**

- Title: Research and development of quantum computing and Ising computing systems
- Sponsor: New Energy and Industrial Technology Development Organization (NEDO)
- Duration: 2018-2027
- Institutions: AIST, NEC, Toshiba, Fujitsu, U Tokyo, Waseda U, YNU etc.

#### Task 1: R&D of Generic Software for Ising Machines

- R&D of common software for quantum annealing
- Optimization of architecture
  - Exploration od application
  - Comparison with classical computer.

Task 2: R&D of Quantum-Classical Interface

- R&D of control and readout interfaces using
  - Cryo-CMOS IC
  - Superconducting IC

Task 3: R&D of Quantum processor

- R&D of a JPO-based quantum annealer
- R&D of 3D integration technology

## **All-to-All Connected JPO Ising Machine**

- Build a quantum annealer using Josephson parametric oscillators (JPOs).
- Employ the LHZ scheme for all-to-all gubit connections.



#### LHZ architecture for all-to-all gubit connections

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 59, May 2025. Presentation given at 22nd Biennial U.S. Workshop on Superconductor Electronics, Devices, Circuits, and Systems Santa Fe, New Mexico, April 6-10, 2025.

## **Correlated Oscillations in Coupled JPOs**



#### Oscillation amplitudes of two JPOs



Optical image and circuit schematic of a device chip contain two JPOs





T. Yamaji et al., Phys Rev Appl 20 014057 (2023).

Output signal from the *left* JPO plotted in the *IQ* plane

## **Project in YNU**

## Control and detection of JPO states by SFQ and AQFP circuits at low temperatures





## **Operation Principle of AQFP-mux QC**



Simulation at 4.5 and 5 GHz



Cable # does not increase with qubit # due to microwave multiplexing
Parallel qubit control available.

N. Takeuchi, et al. npj Quantum Inf 10, 53 (2024).

## **Experiment @4.2K: Microwave Switching**





Each output switched on/off by digital signals

Output power: -82 dBm On/off ratio: ~40 dB power dissipation: 81.8 pW per qubit

N. Takeuchi, et al. npj Quantum Inf 10, 53 (2024).

## Superconducting digital electronics projects in Japan

- Research on ultra-low power sub-terahertz superconducting quantum digital systems based on pulsedriven circuits
  - Sponsor: Japan Society for the Promotion of Science (JSPS)
  - Research category: Grant-in-Aid for Specially Promoted Research
  - Leader: Akira Fujimaki (Nagoya University)
  - Duration: 2018-2024
  - Institutions: Nagoya U, Kyoto U, AIST, Tohoku U, YNU
- Creation and development of superconducting computing technology for post-Moore era
  - Sponsor: Japan Society for the Promotion of Science (JSPS)
  - Research category: Grant-in-Aid for Scientific Research (S)
  - Leader: Koji Inoue (Kyusyu University)
  - Duration: 2022-2027
  - Institutions: Kyusyu U, Tokyo U, Osaka U
- Creation of Ultra-Low Power High-Density Adiabatic Quantum Flux Logic
  - Sponsor: Japan Society for the Promotion of Science (JSPS)
  - Research category:
  - Research category: Grant-in-Aid for Scientific Research (A)
  - Leader: Nobuyuki Yoshikawa (YNU)
  - Duration: 2024-2027
  - Institutions: YNU, Kobe U



# Research on ultra-low power sub-terahertz superconducting quantum<sup>19</sup> digital systems based on pulse-driven circuits

#### Project goal:

- Development of a 100 GHz-class SFQ microprocessor
- Demonstration application of half-flux quantum circuits and their RAM application

Execution of stored programs by an SFQ RAM embedded bit-serial microprocessor at 50 GHz clock frequency



M. Tanaka, et al. Appl. Phys. Lett. 122, 192601 (2023).

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# Research on ultra-low power sub-terahertz superconducting quantum<sup>20</sup> digital systems based on pulse-driven circuits

Half-flux quantum (HFQ) circuits using  $\pi$  junctions

1-kb impulse-driven HFQ RAM



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F. Li, et al. Appl. Phys. Lett. 122, 162601 (2023).

## Creation and development of superconducting computing technology for post-Moore era

#### Project goal:

Investigation of novel superconducting device technologies, including novel optical, memory, and SFQ devices.

Shift-register-based memory

Output

Development of superconducting computer system architectures and OS technologies.

#### A 57.2GHz 8-bit superconductor microprocessor with dual-clocking scheme

#### Superconductor computing for neural networks

Timing gap between two PE's input



splitter (I) 2D Psum or Ofman fmap Weight dataf 8 Baseline architecture

K. Ishida et al., et al. IEEE Micro. 41, 19-26 (2021).

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Ifmap Psum

Nagaoka et al., 2022 IEEE Asian Solid-State Circuits Conference (A-SSCC)

## Creation of Ultra-Low Power High-Density Adiabatic Quantum Flux Logic

#### Project goal:

Investigation of high integration density adiabatic superconducting logic



N. Yoshikawa, et al. ASC2024, Salt Lake City.

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## Summary

- The current status of Japan's superconducting (SC) electronics projects was reviewed.
- Most large-scale funding is rerated to quantum computing.
  - Superconducting circuits, such as an RSFQ and AQFP, are used for qubit control and readout.
- Some small-scale projects on SC digital electronics are ongoging, supported by JSPS.