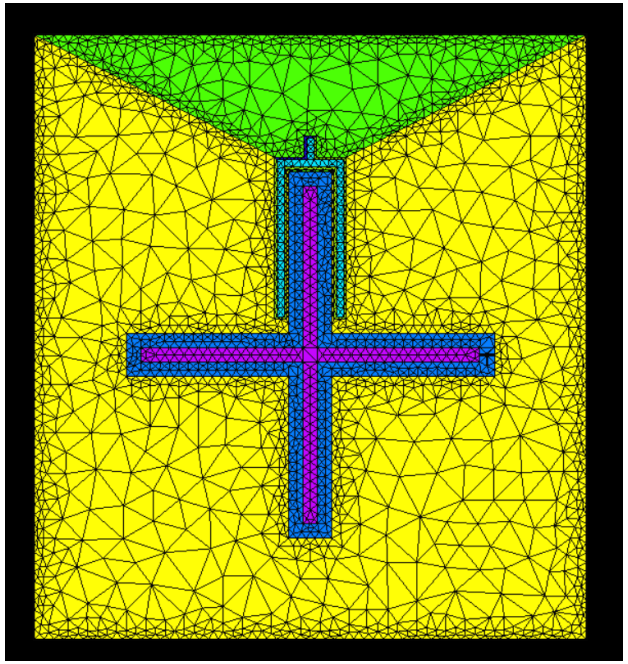
Empowering Quantum Design: Advanced EDA Tools for Superconducting and Quantum Circuits

Johannes A. Delport[1]

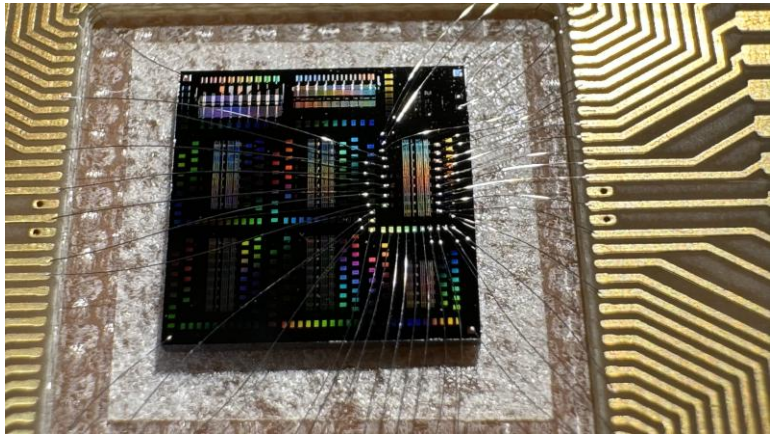


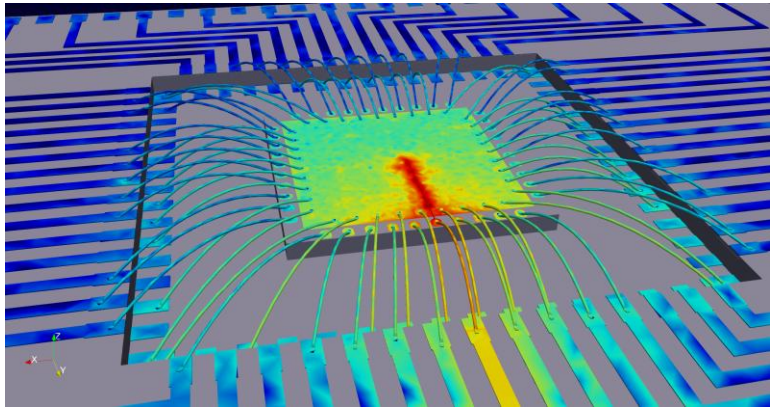
[1]SUN Magnetics (RF) (Pty) Ltd, 15 De Beer Street, Stellenbosch, 7600, South Africa

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Brief overview of SUN Magnetics

- Originated in superconducting & quantum-circuit research at Stellenbosch University.
- Developed into open and commercial-grade toolchains used in the community.
- Collaborations with academic and government programs (e.g., SuperTools) informed capabilities.





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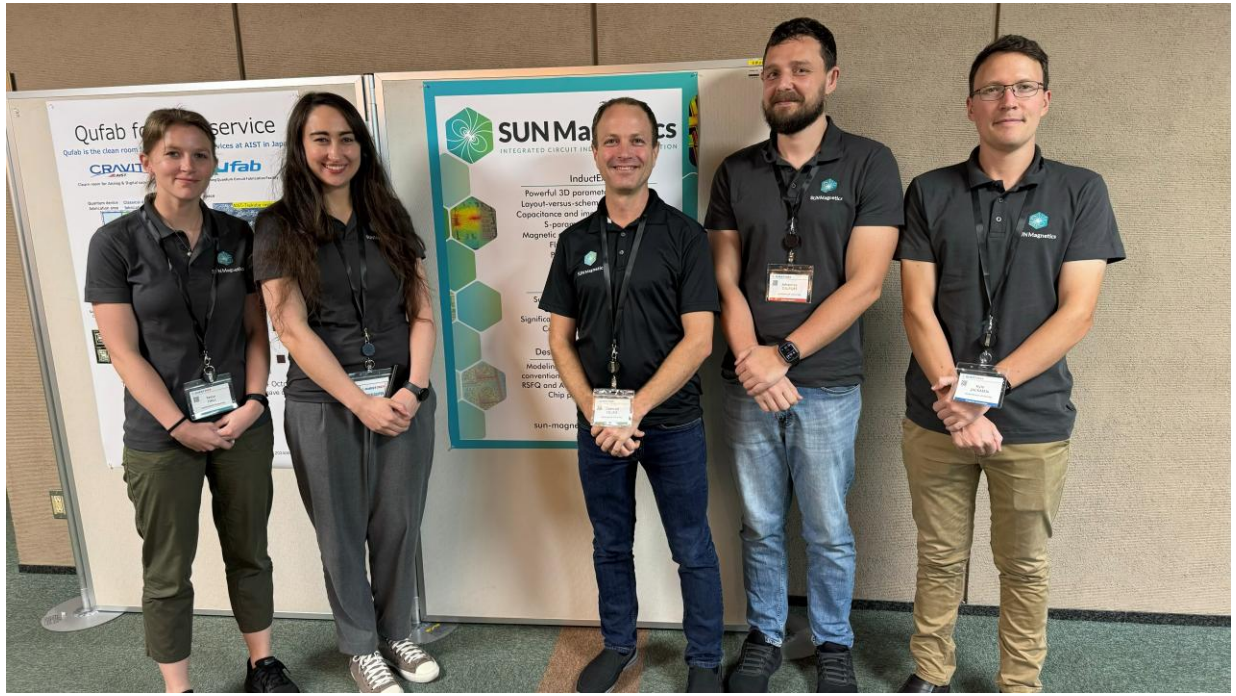
Brief overview of SUN Magnetics

- People behind the methods:
  - Core contributors:
    - C. Fourie
    - K. Jackman
    - J. Delport
    - L. Johnston
  - Collaborating students & topics:
    - T. Hall — SQUIDs/SQIFs/BiSQUIDs
    - P. Rossouw — SQUID noise modelling
    - R. Bird — Automated Hamiltonian extraction



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Superconducting/Quantum EDA: where tools meet physics

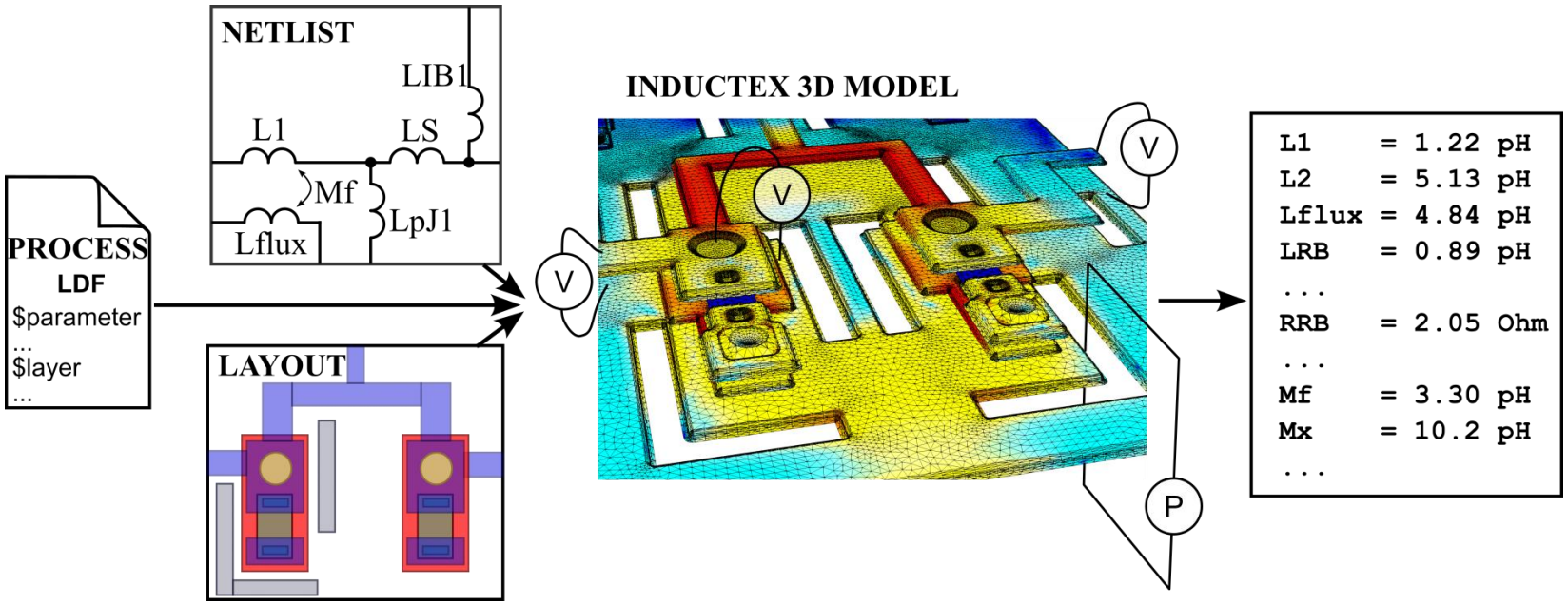
- Early S-EDA: fragmented research modules; limited integration.
- Persistent challenges:
  - Precise impedance control
  - Sensitivity to magnetic flux / trapped vortices
  - 3D layout verification at scale
  - Analog simulation for JJ-based circuits at cryo
- Field trend: broader investment → more mature, validated toolchains.

How we study these challenges

- Approach: physics-based extraction + compact models + circuit-level simulation
- Examples: inductance/capacitance extraction, flux-aware analysis, LVS checks
- We'll show results using an InductEx-based workflow

What is InductEx?

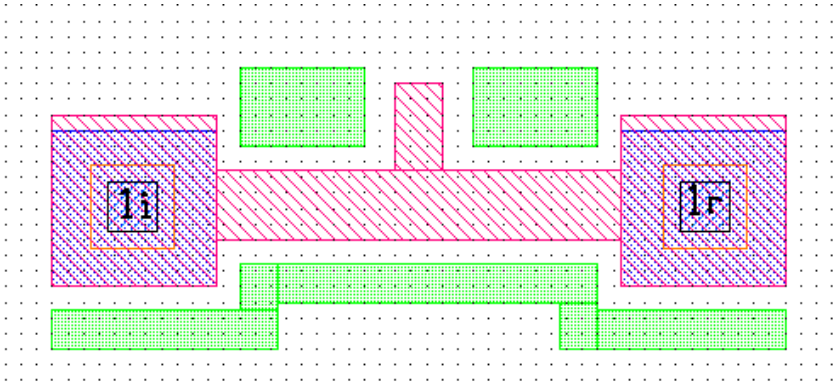
- InductEx [1] and engines FFH [2] / TetraHenry [3] extract inductance netlists.
  - Workflow: layout + netlist + process file → 3D model → field solver → impedance/inductance netlist
  - Purpose: self & mutual inductance for mixed-material, multilayer circuits

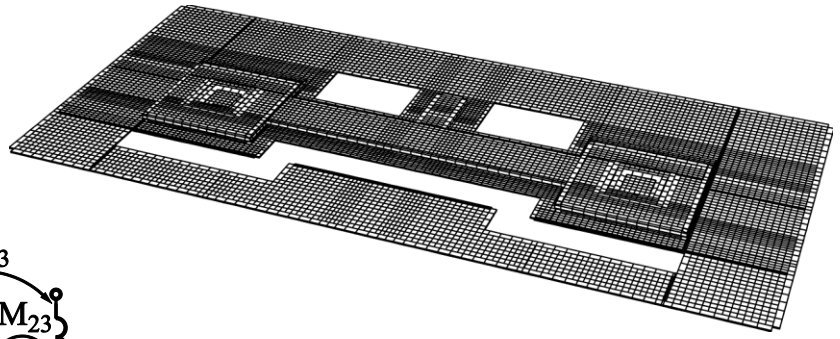


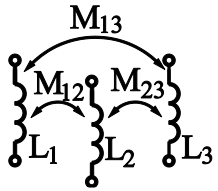
[1] C. J. Fourie, O. Wetzstein, T. Ortlepp, and J. Kunert, "Three-dimensional multi-terminal superconductive integrated circuit inductance extraction," *Supercond. Sci. Technol.*, vol. 24, 125015, 2011.
[2] K. Jackman and C. J. Fourie, "Fast multicore FastHenry and a tetrahedral modeling method for inductance extraction of complex 3D geometries," in *15th International Superconducting Electronics Conference*, Nagoya, 2015.
[3] K. Jackman and C. J. Fourie, "Tetrahedral modeling method for inductance extraction of complex 3-D superconducting structures," *IEEE Trans. Appl. Supercond.*, vol. 26, p. 0602305, 2016.

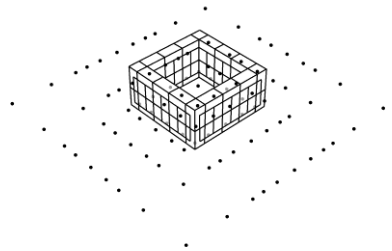
InductEx

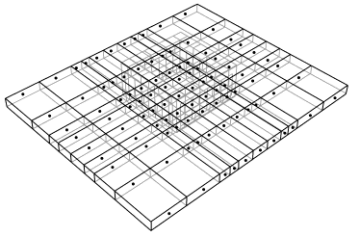
- **“InductEx” originated as generic term for a collection of modules that includes numerical engines and equation solvers (FastHenry, Solver, etc.)**
- v1: 2004 – InductEx [4] started as a wrapper for FastHenry.
  - Read structures from GDS layouts; no netlists; handled holes.
  - No lookup tables – full 3D structures handled up to ~10,000 segments.

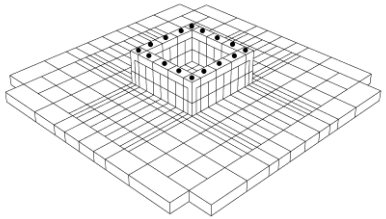








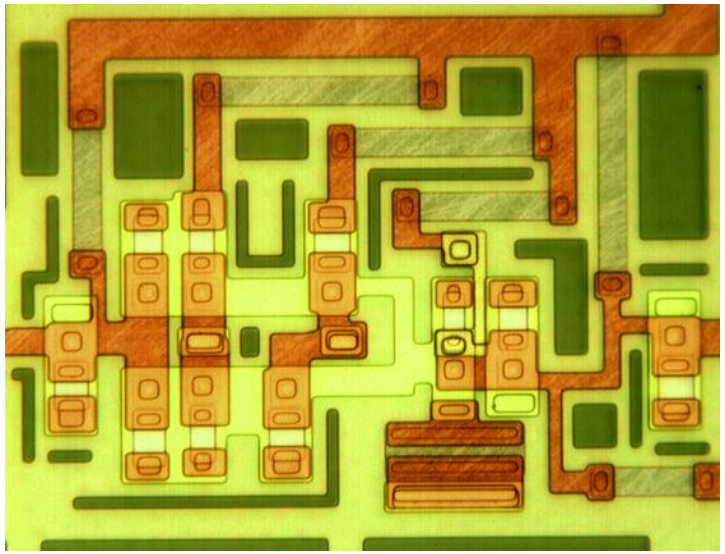


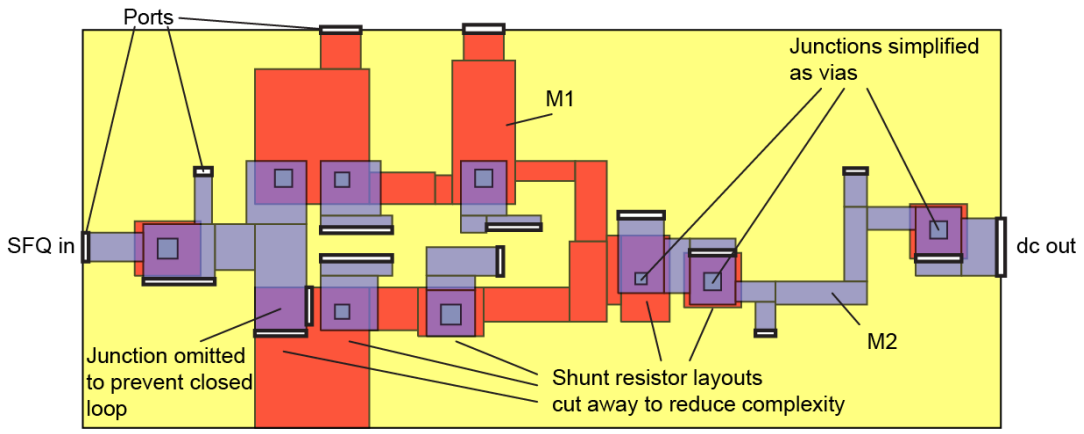


[4] C. J. Fourie, W. J. Perold, “Simulated inductance variations in RSFQ circuit structures," *IEEE Trans. Appl. Supercond.*, vol. 15, p. 300-304, 2005.

InductEx

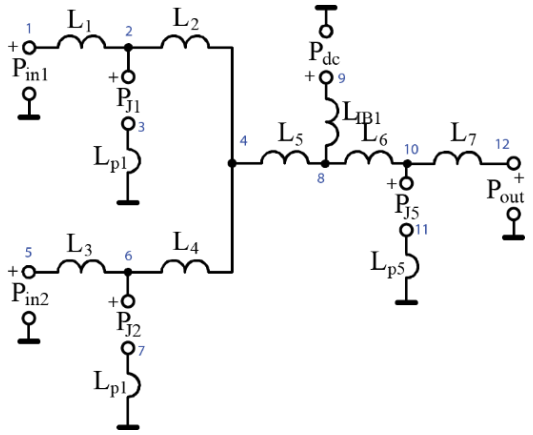
- v2: 2007
  - Multi-terminal network (netlists) – no mutual inductance.
  - Slow (15 hours, this example with 31 inductors, 20,000 segments).
  - (v3 experimental for NioCAD; more efficient; never released).

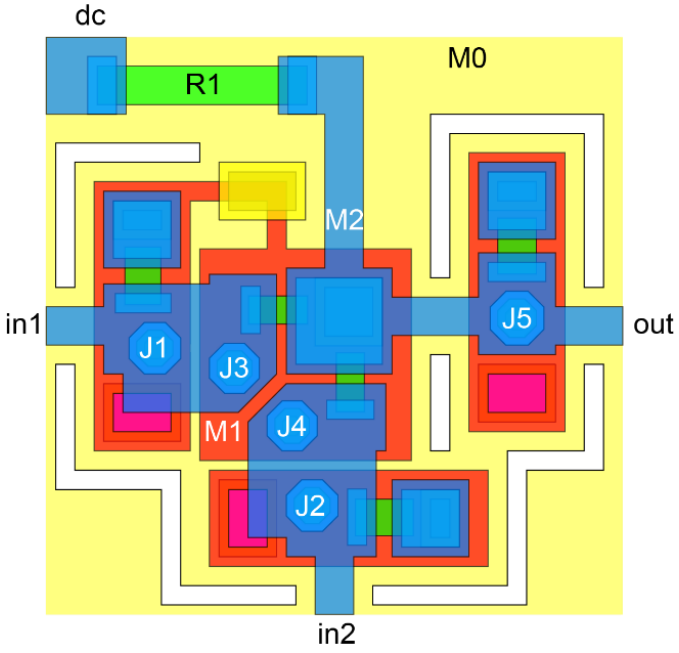


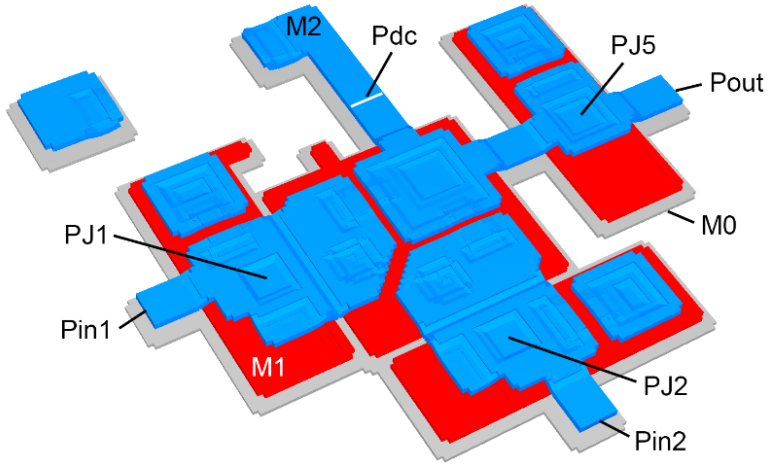


InductEx

- V4.1: 2011
  - GDS hierarchy, polygon/path support, fabrication-ready layouts.



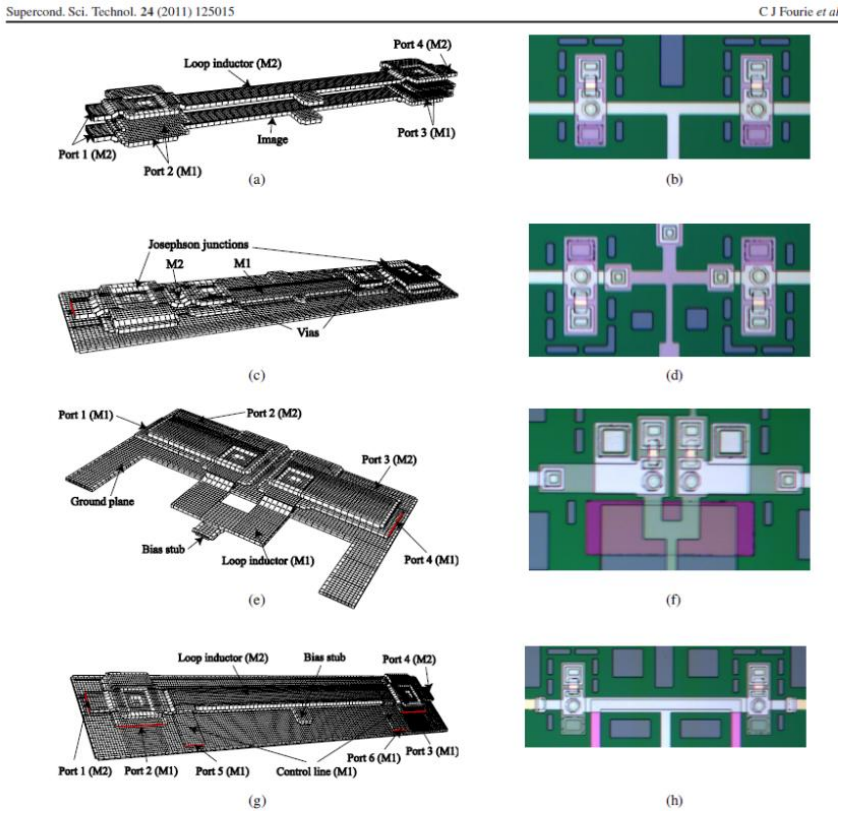





```
Inductor    Design      Extracted   AbsDiff     PercDiff
L1          2.01000     2.06540     +0.05536    +2.75%
L2          0.83000     0.84319     +0.01319    +1.59%
L3          2.03000     2.06370     +0.03371    +1.66%
L4          0.83000     0.83197     +0.00197    +0.24%
L5          0.27000     0.25668     -0.01332    -4.93%
L6          2.97000     2.98900     +0.01902    +0.64%
L7          1.97000     2.04070     +0.07065    +3.59%
Lp1         0.20000     0.17885     -0.02115    -10.58%
Lp2         0.20000     0.18080     -0.01920    -9.60%
Lp5         0.20000     0.19488     -0.00512    -2.56%
Lib1        0.00000     2.17660     +2.17660    --%
Deallocating memory.
Cycles found in 0.022 seconds.
SVD solution in 0.012 seconds.
Job finished in 136.750 seconds.
```

InductEx – Tool verification and acceptance

- Proved results – against measurements from Leibniz-IPHT in 2011.
  - Showed tool accuracy decisively, but not sufficient to sway users from older tools.



IOP Publishing
Superconductor Science and Technology
Supercond. Sci. Technol. 24 (2011) 125015 (12pp)
doi:10.1088/0953-2048/24/12/125015

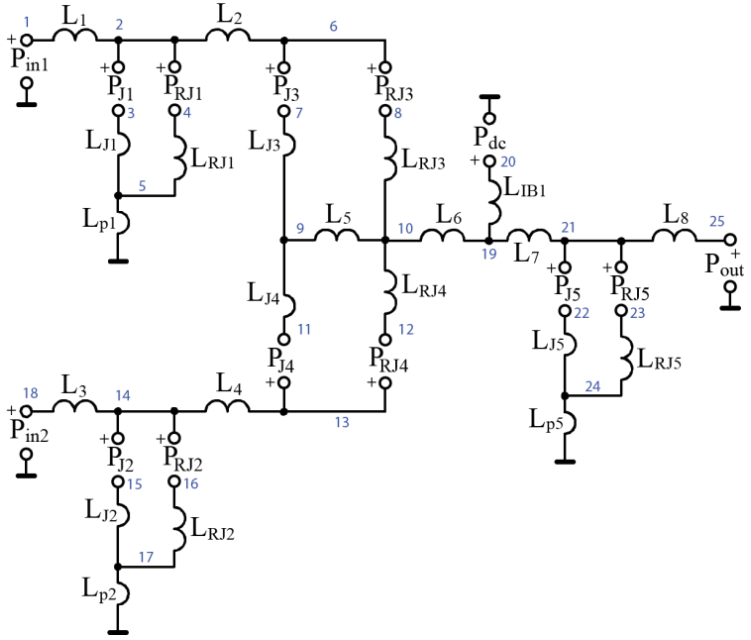
Three-dimensional multi-terminal superconductive integrated circuit inductance extraction

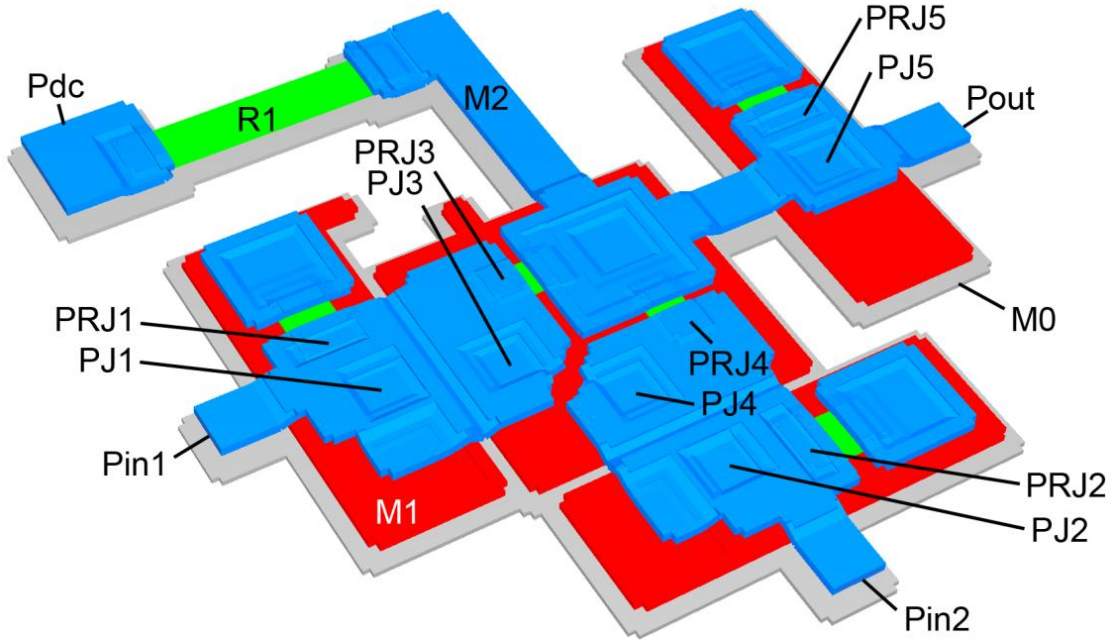
Coenrad J Fourie[1], Olaf Wetzstein[2], Thomas Ortlepp[3] and Jürgen Kunert[2]

Chip	Inductor	Measured (pH)	Uncalibrated (pH)	Calibrated (pH)	Error (%)
1	M2	9.83	9.09	9.89	+0.6
1	M1	5.61	5.64	5.62	+0.1
1	M1–M2	6.92	6.65	6.91	−0.1
2	M2	9.95	9.09	9.89	−0.6
2	L_{11} in M2	11.2	10.4	11.2	−0.4
2	$M_{M2–M1}$	3.84	3.92	4.00	+3.1
2	L_{11} in M1	5.68	5.80	5.78	1.7
2	$M_{M1–M2}$	4.36	4.46	4.44	+1.8
3	M2	20.5	18.8	20.5	−0.2
4	$M_{M1–M2}$	4.32	4.46	4.44	+2.7
4	M2	9.73	9.09	9.89	+1.6

InductEx

- V4.2 - 2013
  - Resistive layers and complex linear solvers; resistance.
  - Could now find inductance of shunts; full gate circuit extraction [5].

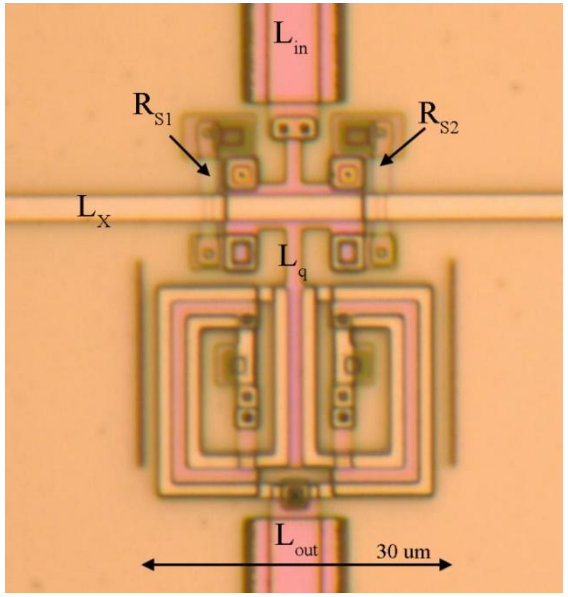


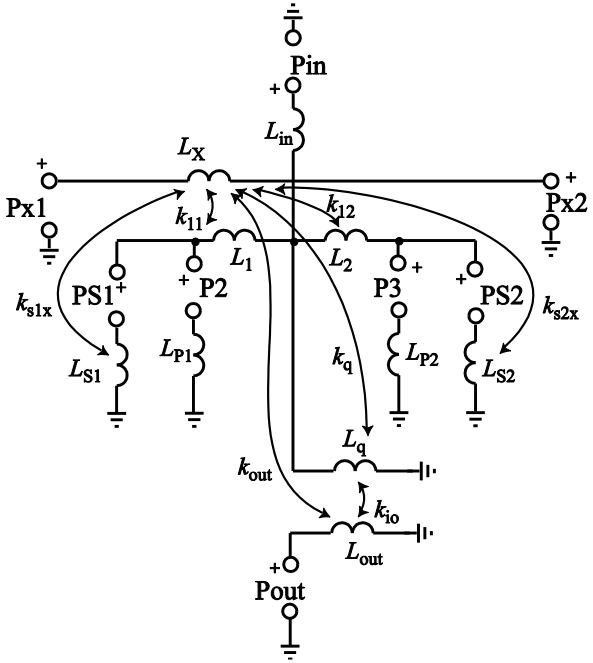


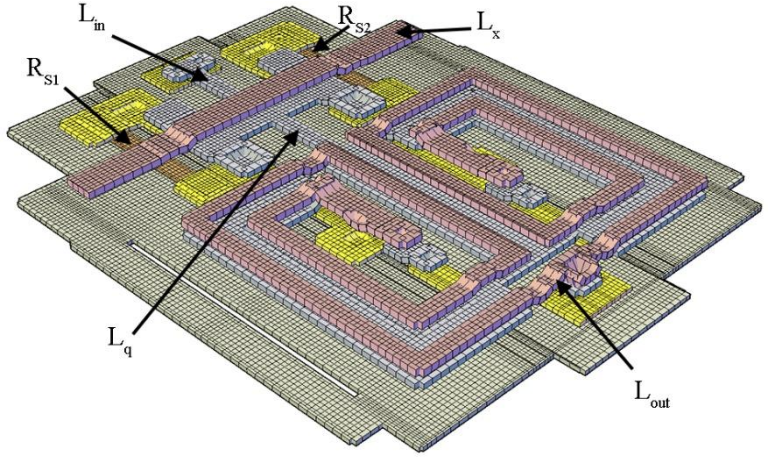
[5] C. J. Fourie, "Full-gate verification of superconducting integrated circuit layouts with InductEx," *IEEE Trans. Appl. Supercond.*, vol. 25, 1300209, 2015.

InductEx – Tool acceptance

- Used in AQFP & RSFQ research in 2013:
  - Yoshikawa group at YNU (Naoki Takeuchi) – AQFP.
  - Vasili Semenov at SUNY – later for IARPA C3.







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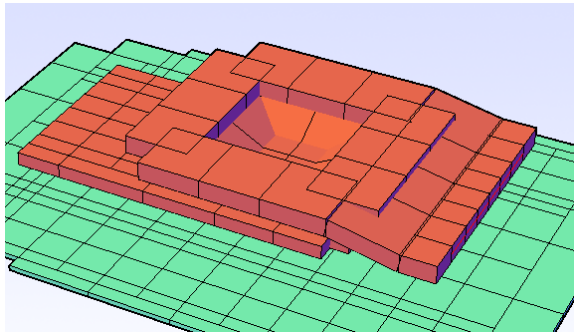
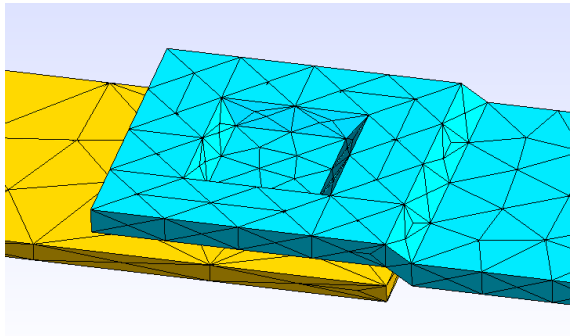
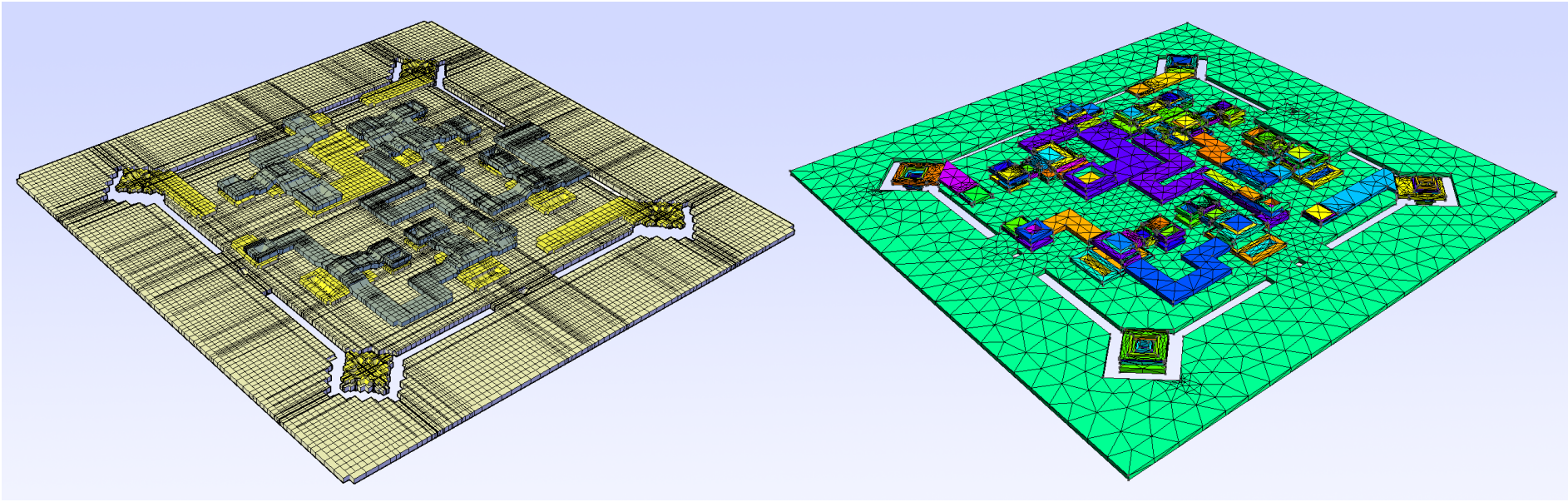
InductEx engines

- 2015: 2nd engine (TetraHenry).
  - Tetras, triangles, and cuboids.
  - Kyle Jackman's work.







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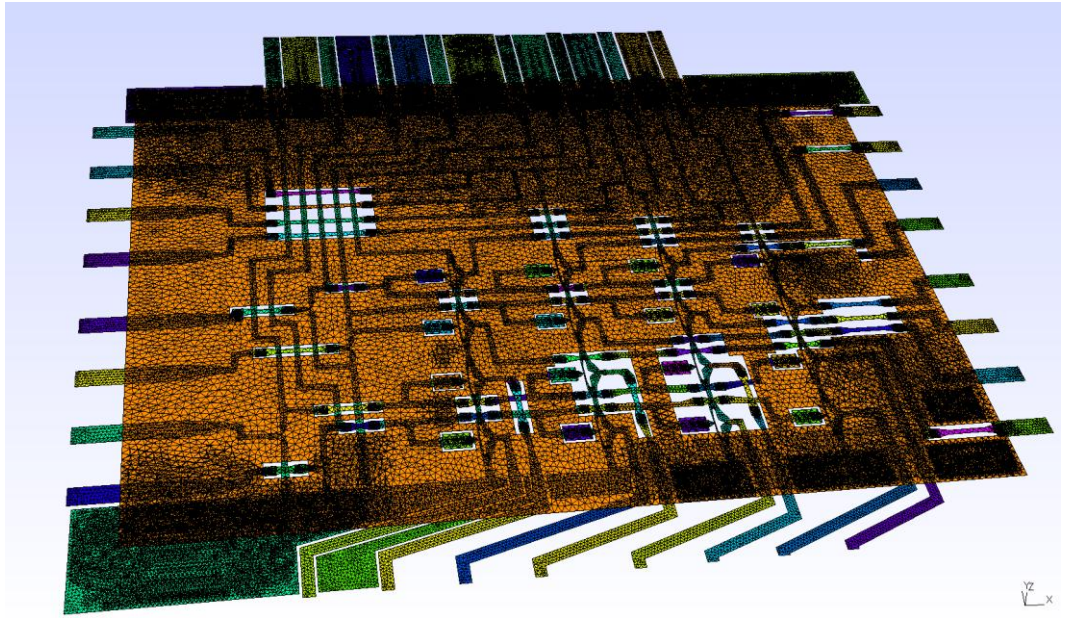
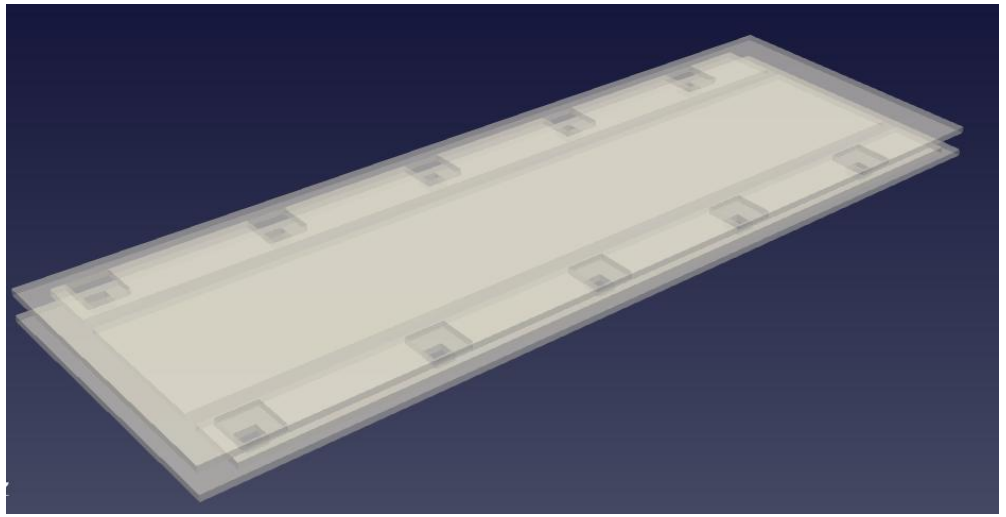
InductEx capabilities improved

- 2018: Capacitance extraction added
  - Allows characteristic impedance extraction.
  - EQS solver capability added to TetraHenry; surface models and meshing with InductEx.
  - Multiple dielectric interfaces.





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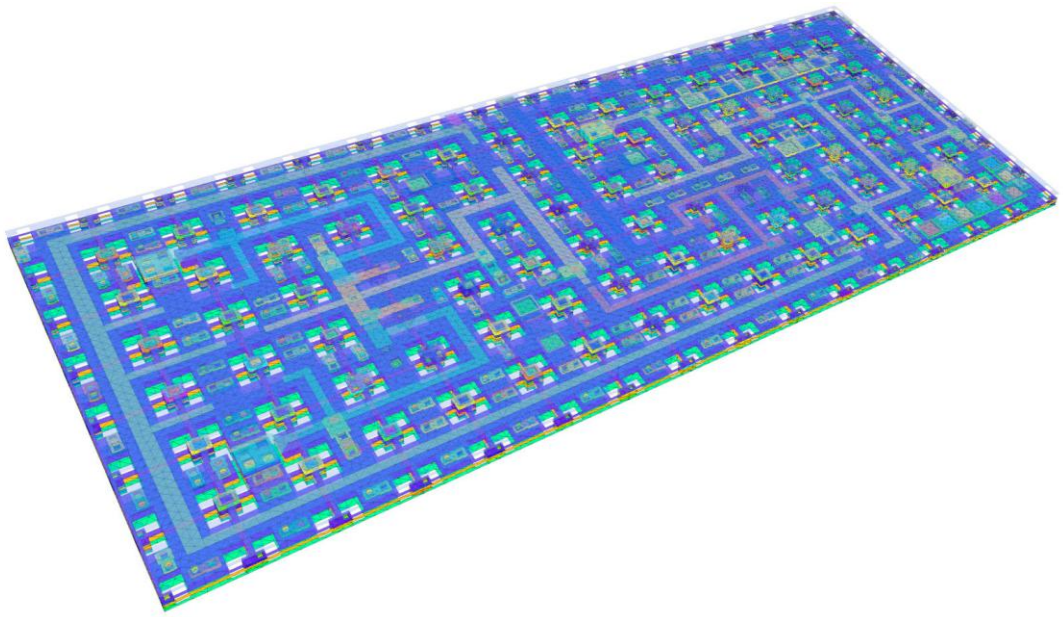
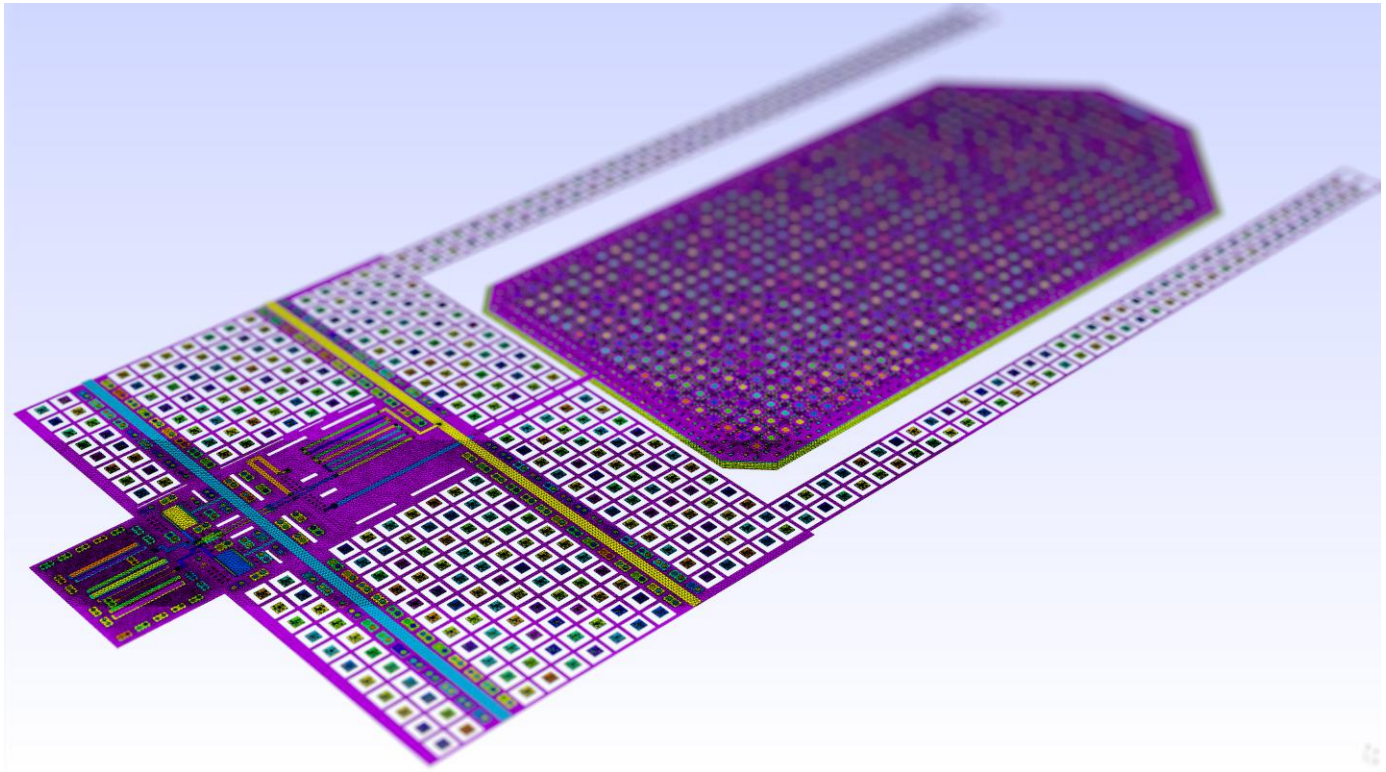
InductEx capabilities improved

- Solver speed/memory & meshing improvements → now 10 M+ segments.





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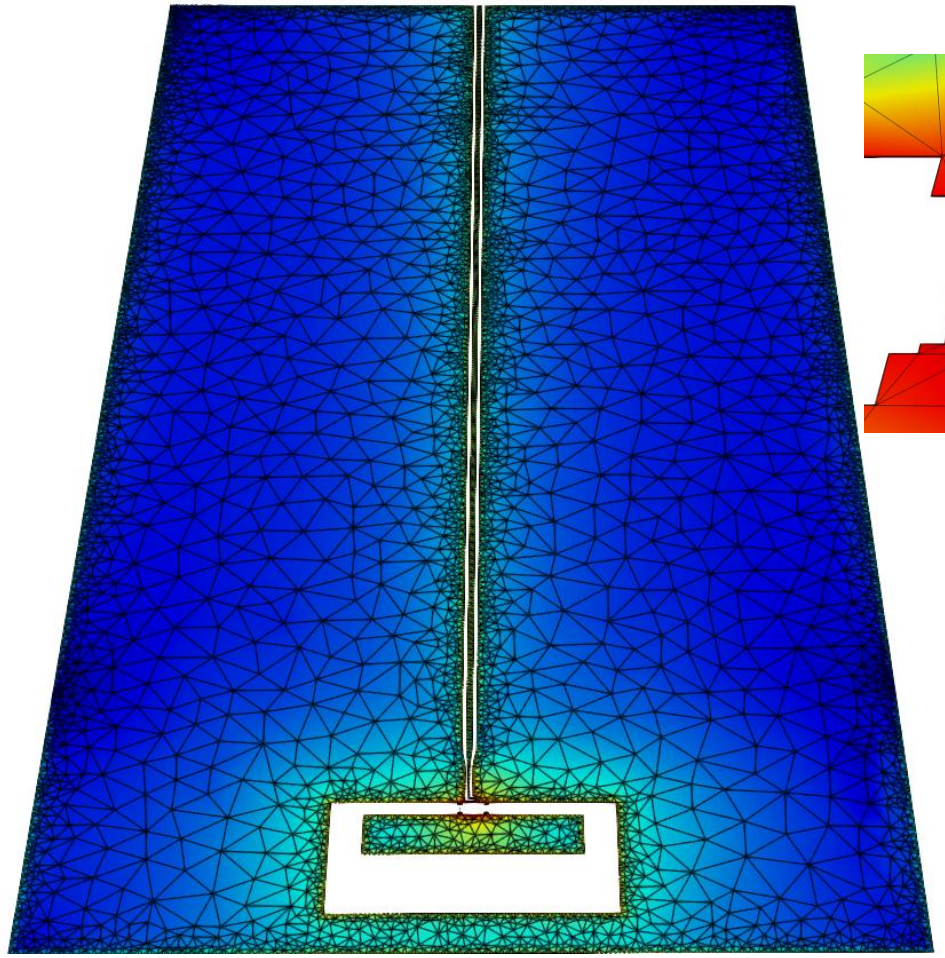
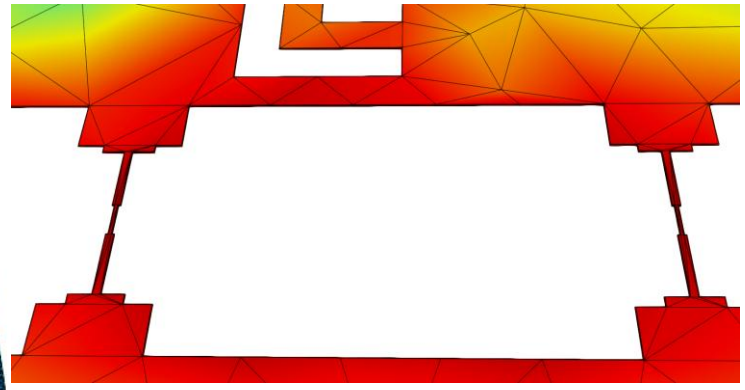
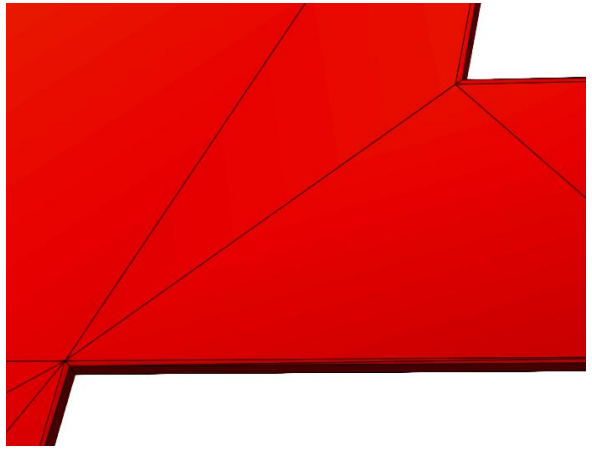
InductEx 8 – New

- Internal mesh engine.
- Shadow casting for high fidelity.
- Edge slice segments for edge currents
- Meshing optimized for weak coupling and current flow up to penetration depth from film edges.







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Mitigating flux sensitivity: modelling → experiment

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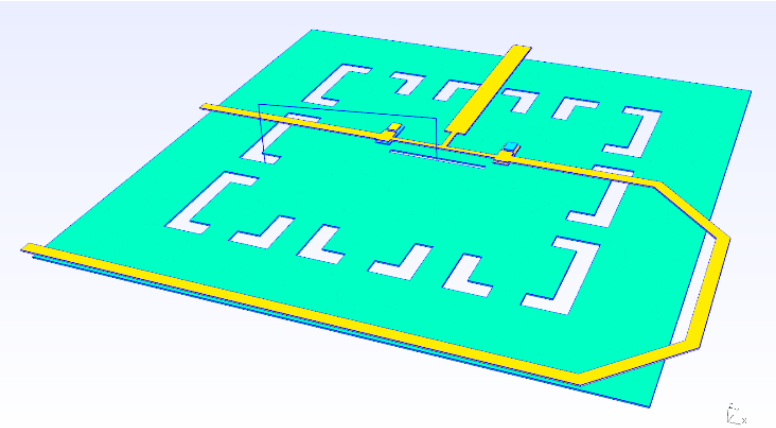
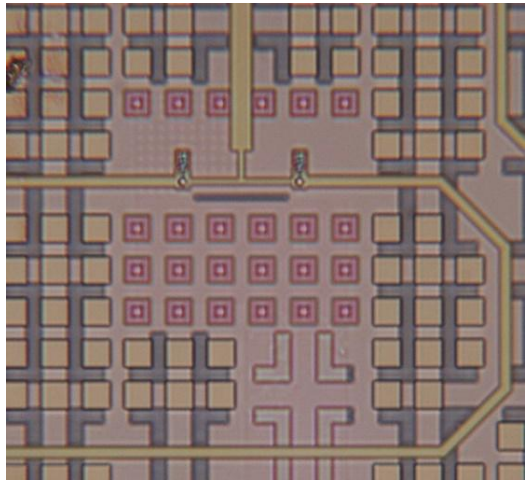
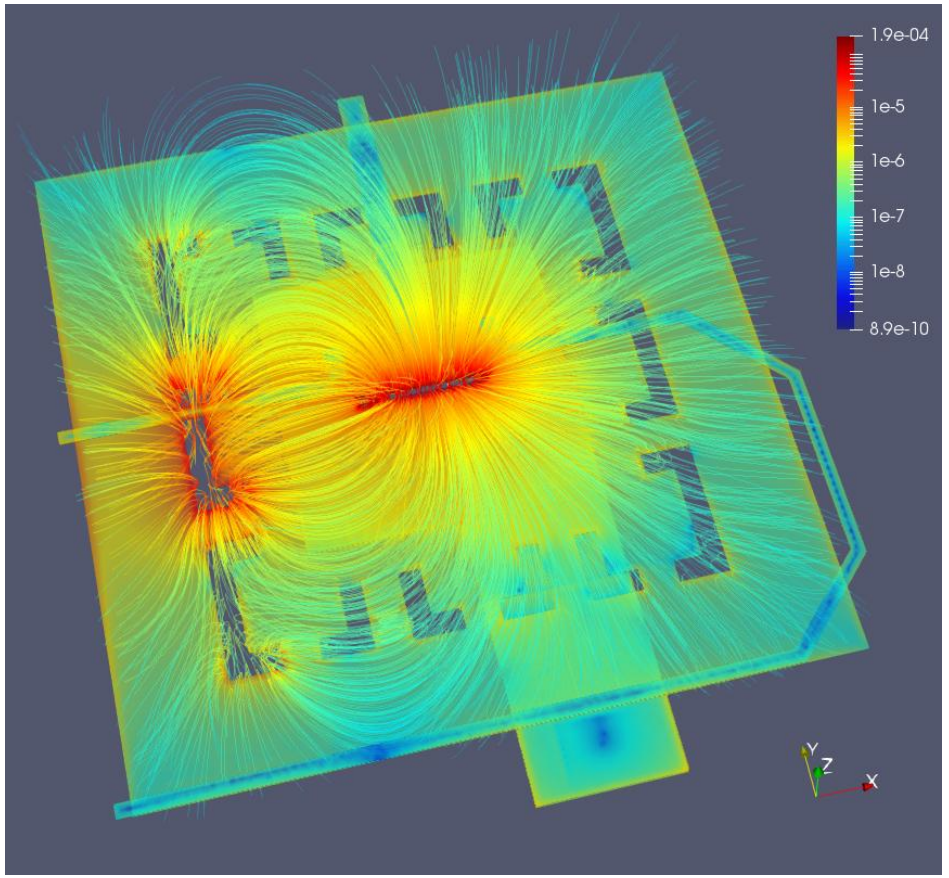
Flux trapping analysis

- One of most consequential outcomes of SuperTools.
- Experiments confirm simulations (2019).







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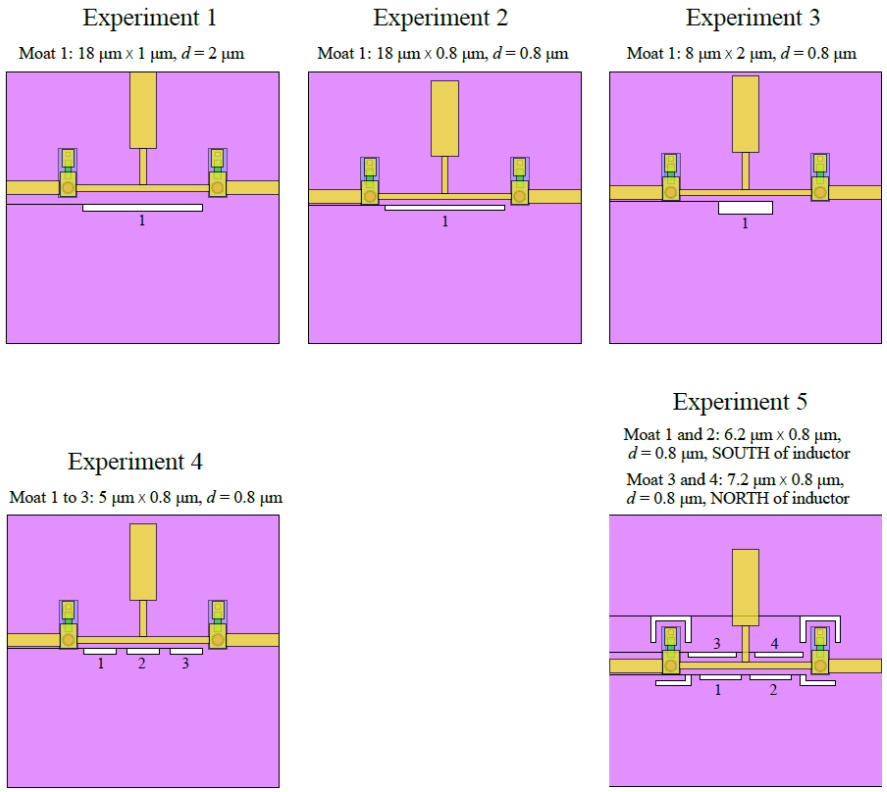
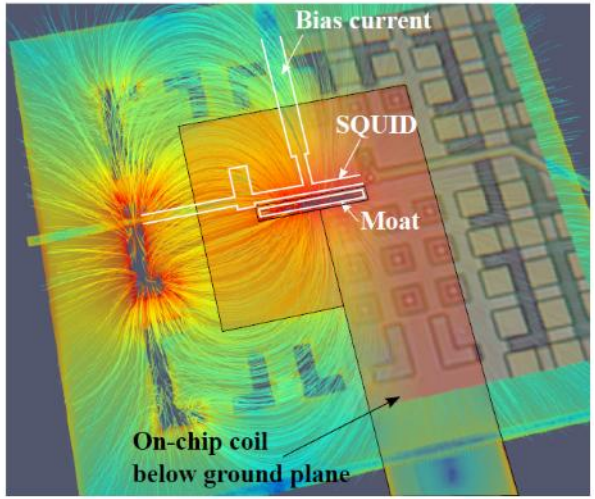
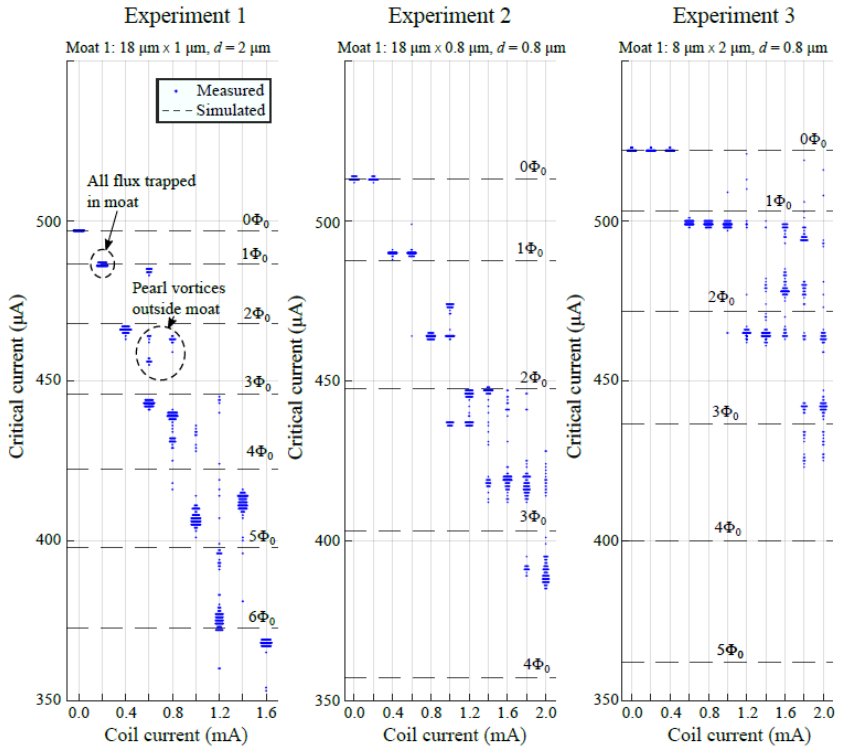
Flux trapping analysis

- Experimentally confirmed. Predicted (simulation) and measured discrete jumps in I_C for a SQUID agree [6].



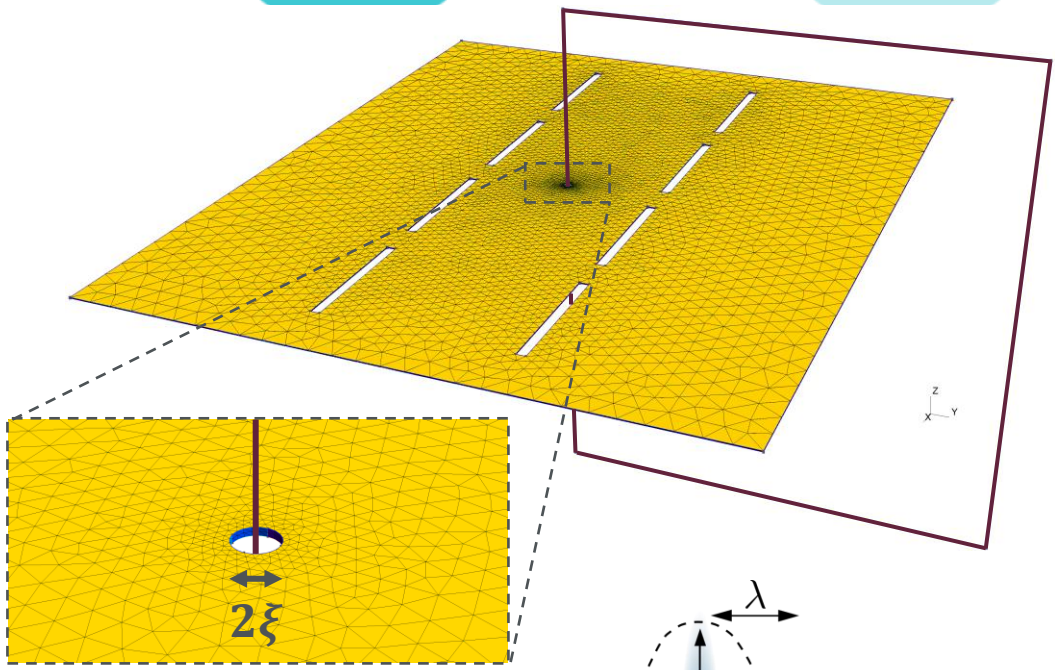


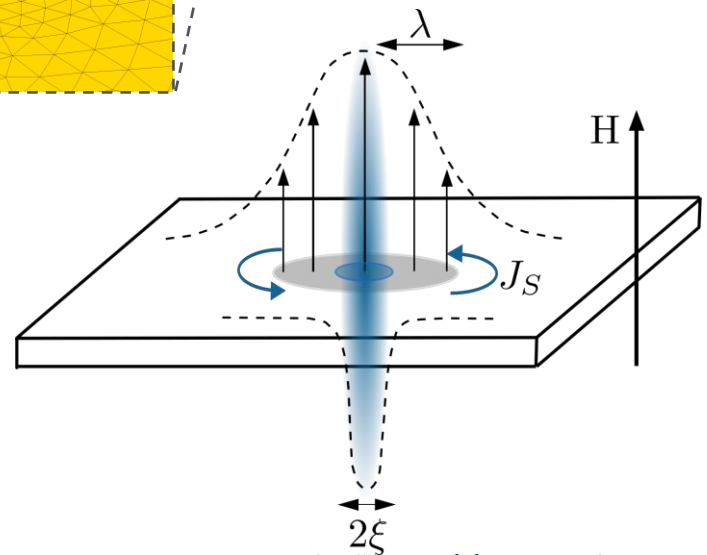


[6] K. Jackman, C. J. Fourie "Flux trapping experiments to verify simulation models," *Supercond. Sci. Technol.*, vol. 33, 105001, 2020

Vortex Simulation Using Gibbs Free Energy

- With InductEx, **Gibbs free energy** for every vortex, moat and current/field component can be calculated; allowing prediction of vortex displacement.
- Vortex is modelled as a small hole in the ground plane, with radius equal to coherence length ξ [1-5].
- Ideal for simulating vortex dynamics in **large-scale circuits**.

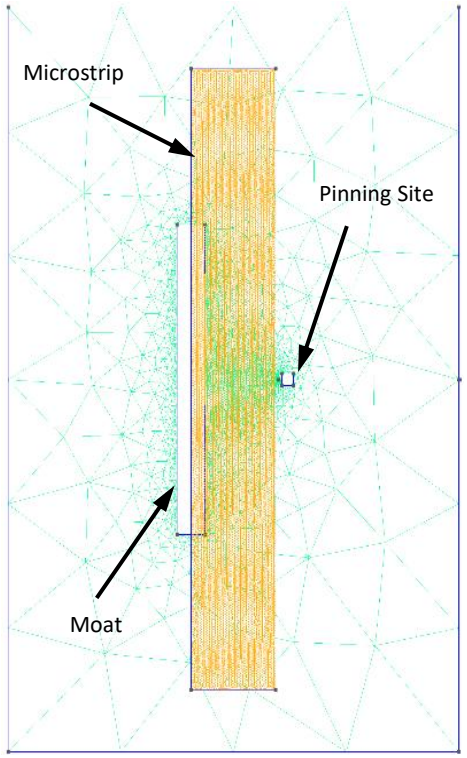


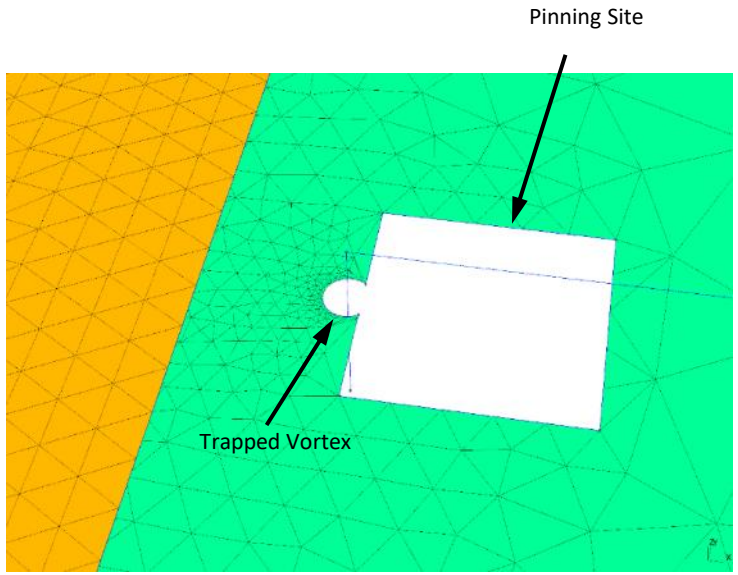


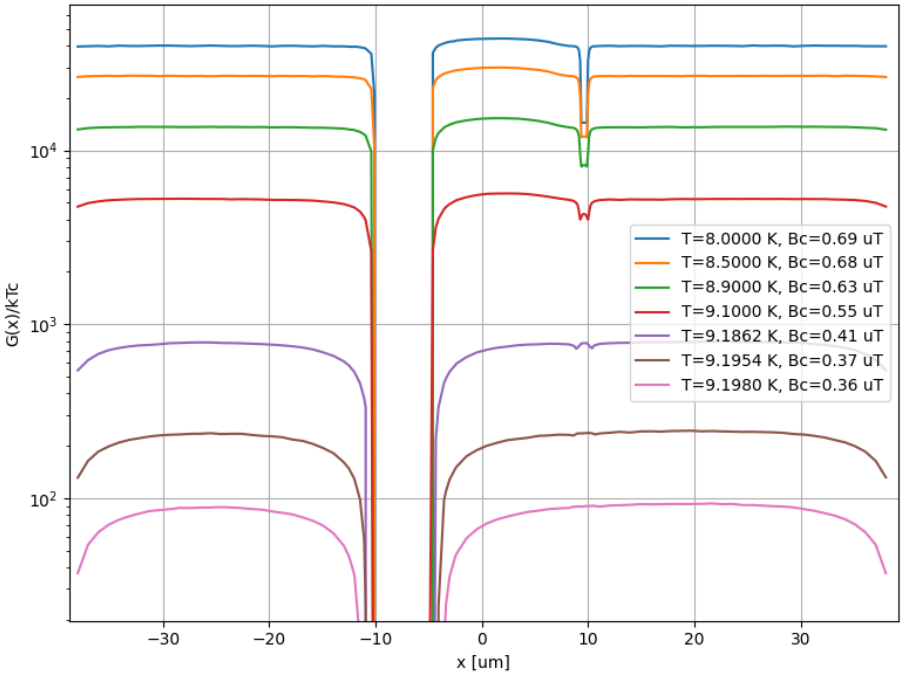
[1] K. Jackman and C. J. Fourie, "Flux Trapping Analysis in Superconducting Circuits," IEEE Transactions on Applied Superconductivity, vol. 27, pp. 1-5, 2017.
[2] V. K. Semenov and M. M. Khapaev, "How Moats Protect Superconductor Films From Flux Trapping," IEEE Transactions on Applied Superconductivity, vol. 26, pp. 1-10, 2016.
[3] K. K. Likharev, "The formation of a mixed state in planar semiconductor films," Radiophysics and Quantum Electronics, vol. 14, p. 722–727, 1971.
[4] G. Stan, S. B. Field and J. M. Martinis, "Critical Field for Complete Vortex Expulsion from Narrow Superconducting Strips," Phys. Rev. Lett., vol. 92, no. 9, p. 097003, March 2004.
[5] K. H. Kuit, et al., "Vortex trapping and expulsion in thin-film YBa 2 Cu 3 O 7− δ strips," Phys. Rev. B, vol. 77, no. 13, p. 134504, April 2008.

Effect of moats and pinning sites

- **Gibbs free energy** method also used to evaluate effect of **moats and pinning sites**.







Gibbs free energy of trapped vortex in the 80μm × 120μm Nb ground plane vs. position along x-axis at various temperatures

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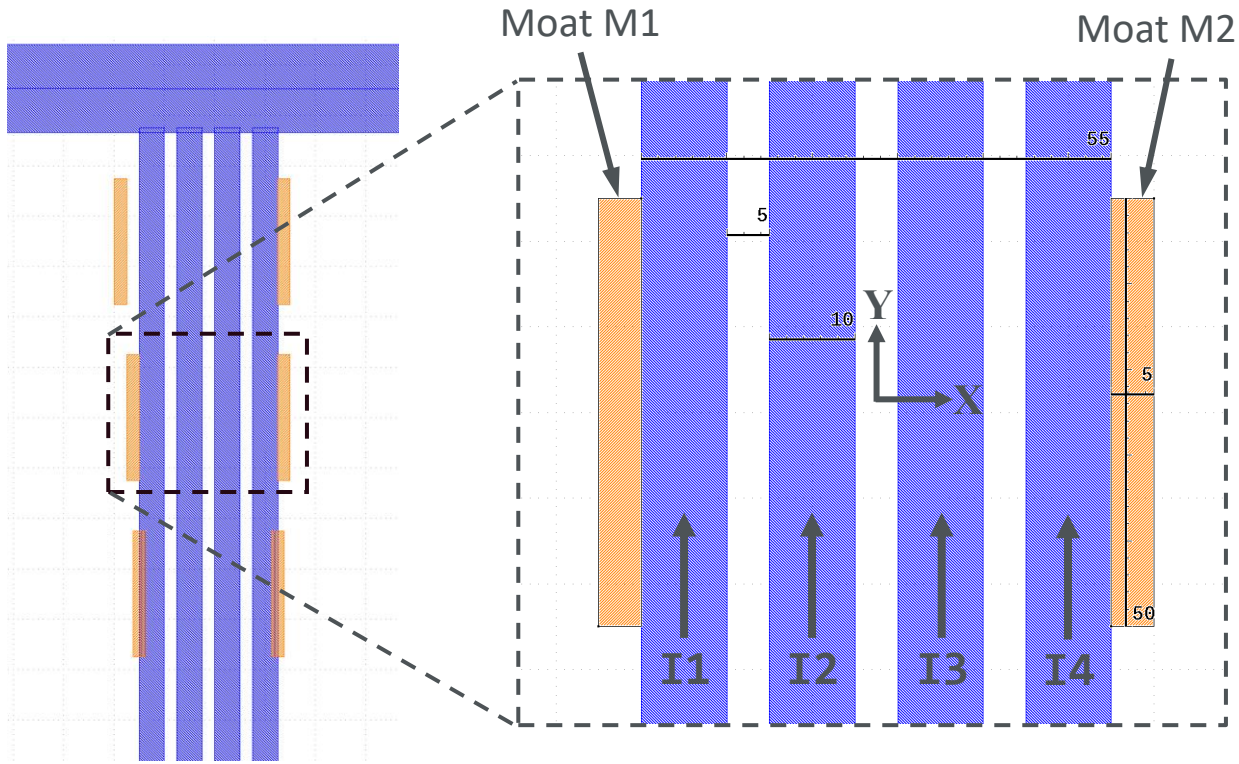
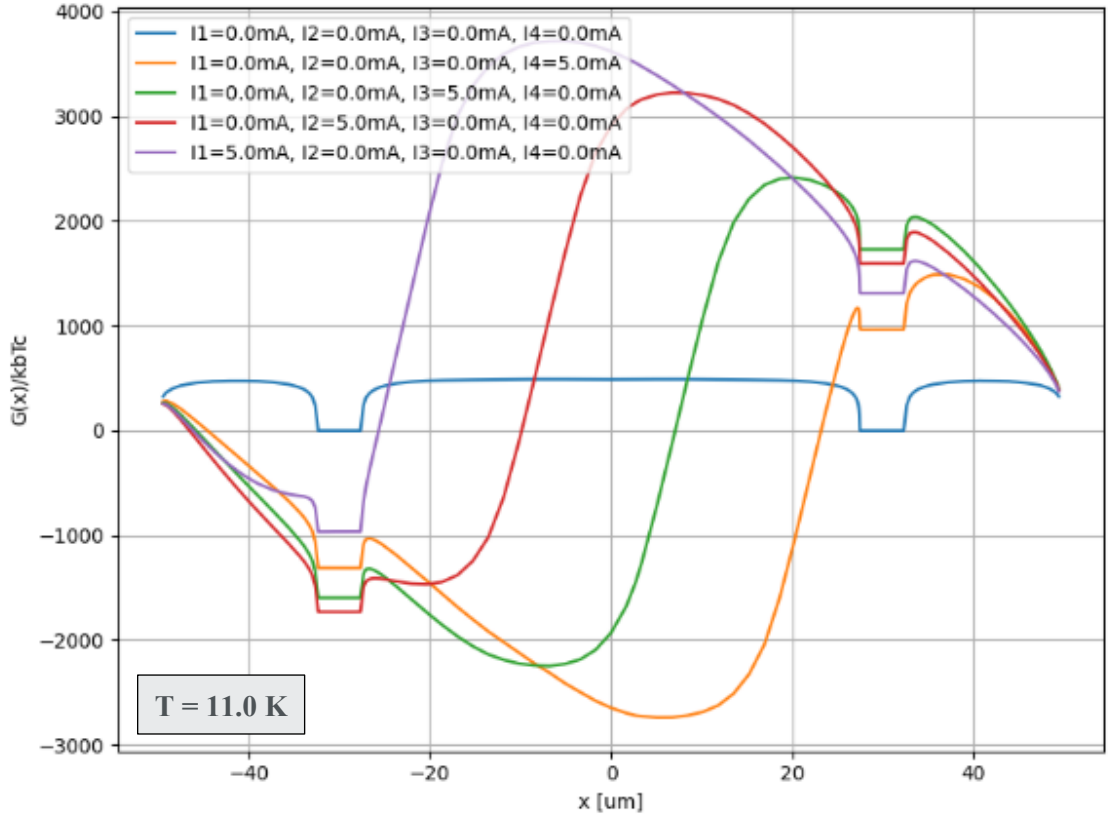
Effect of currents on vortex dynamics

- **Gibbs free energy** method also used to **evaluate effect of currents** on vortex dynamics.





The Gibbs free energy of a vortex trapped in the ground film for currents applied through drive lines.

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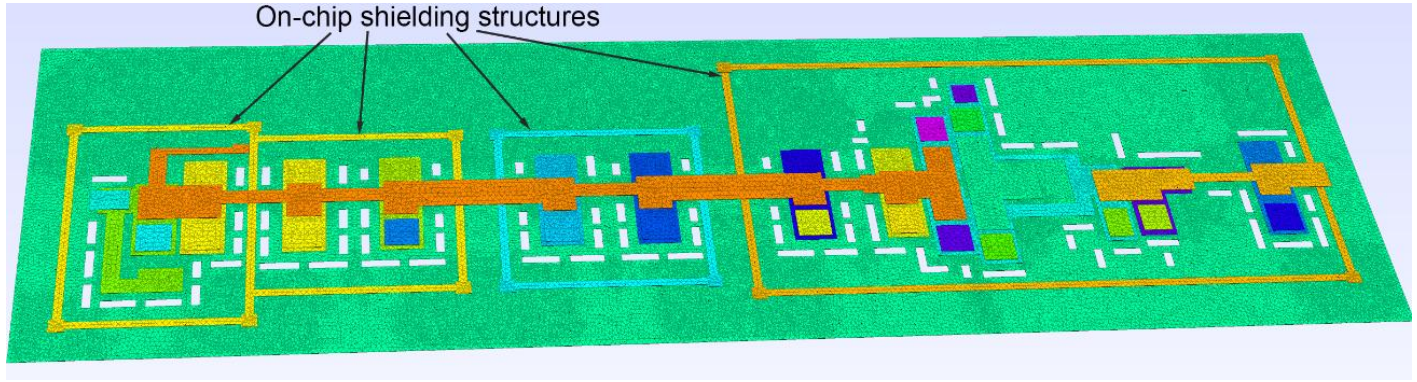
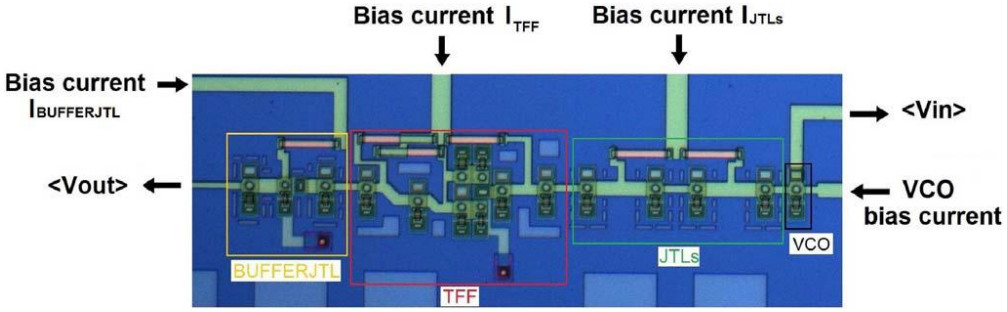
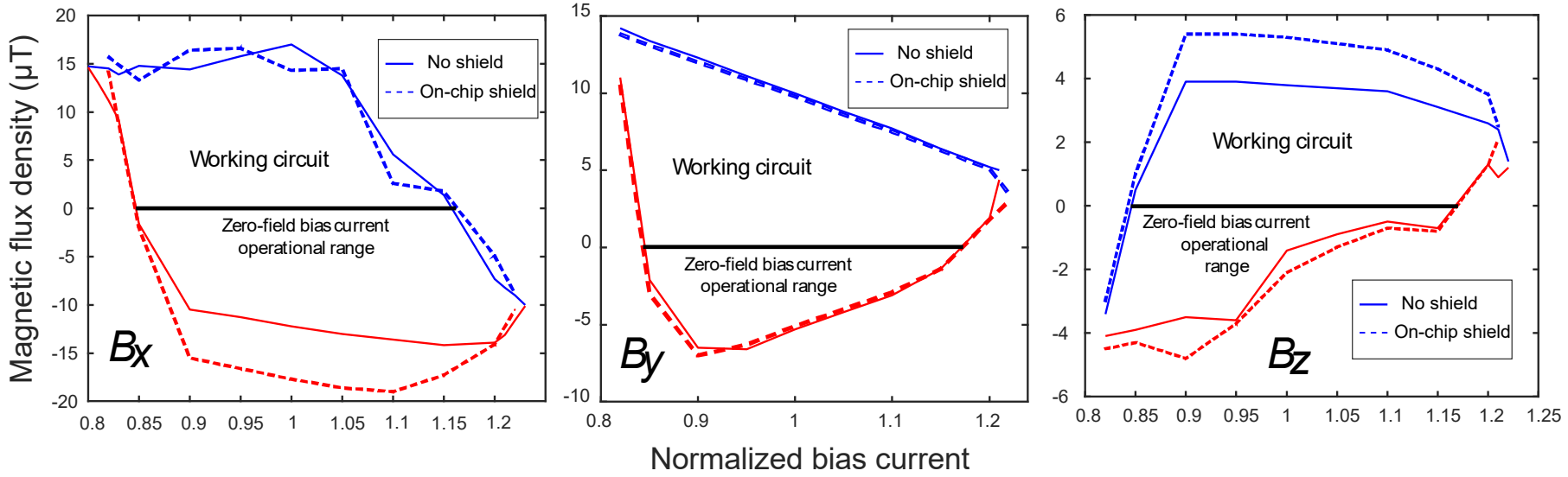
Compact models in EM environment



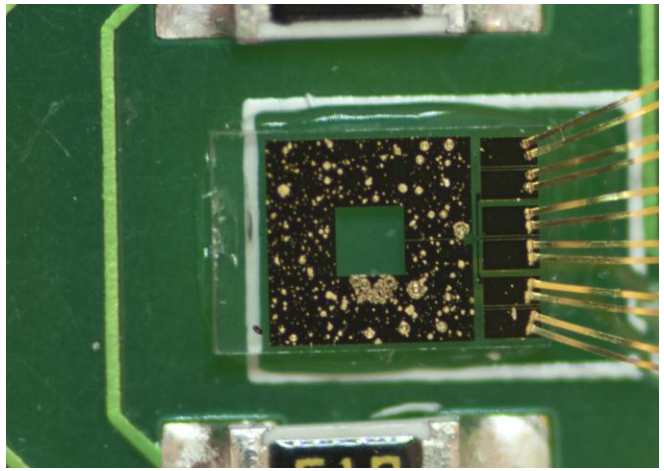


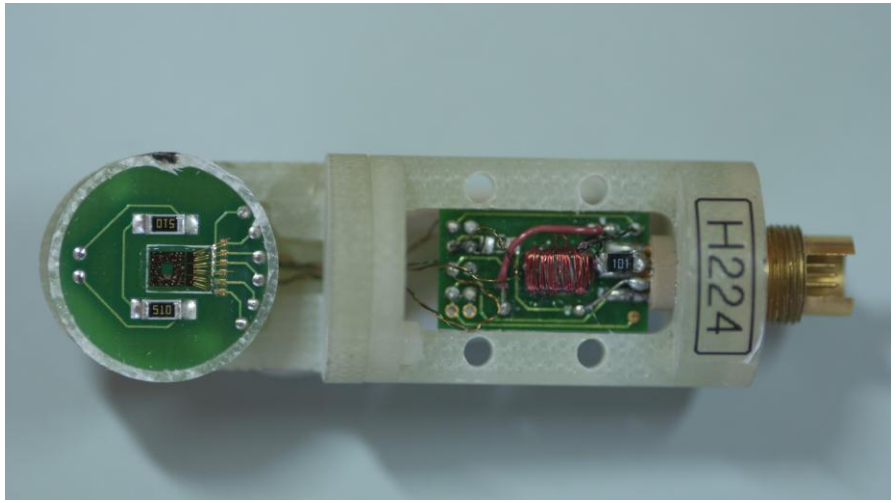


[7] C. J. Fourie, K. Jackman, "Software tools for flux trapping and magnetic field analysis in superconducting circuits," *IEEE Trans. Appl. Supercond.*, vol. 29, 1301004, 2019

Compact models: SQUIDs

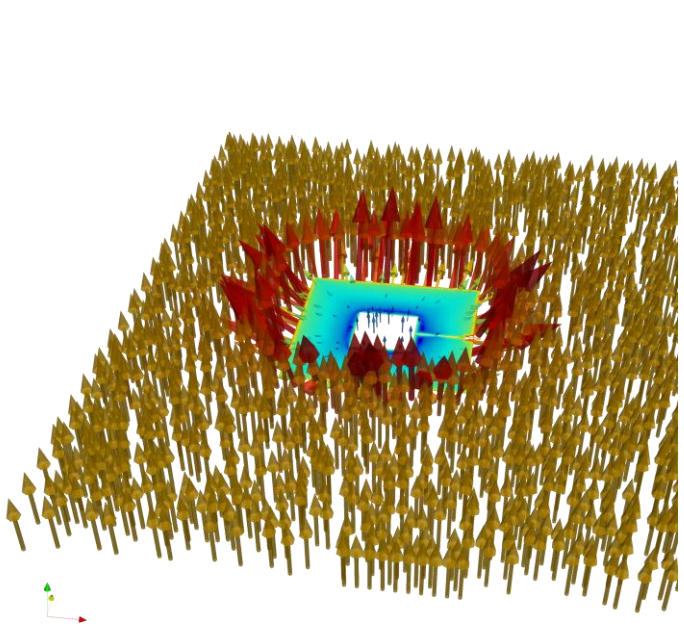
- Modelling and analysis of SQUIDs in magnetic fields, with structures such as feedback coils.
  - Find flux density sensitivity; effective area; feedback current sensitivity.

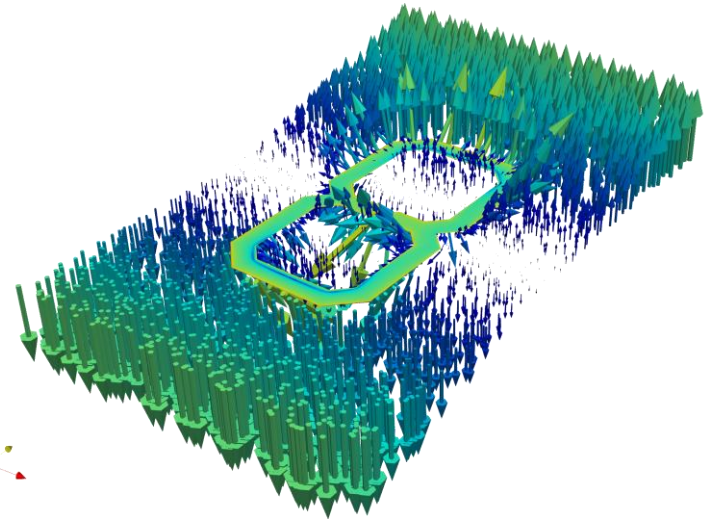


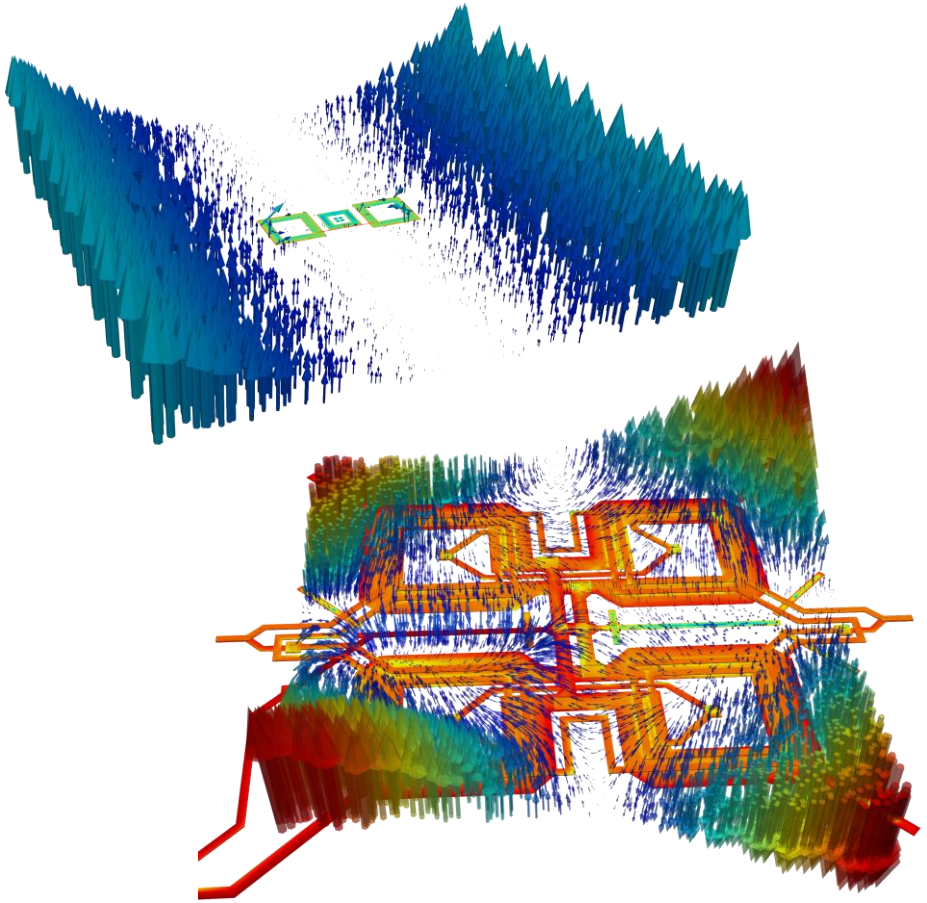


Compact models: SQUIDs and gradiometers in field

- Uniform fields, or functions to model gradient response.







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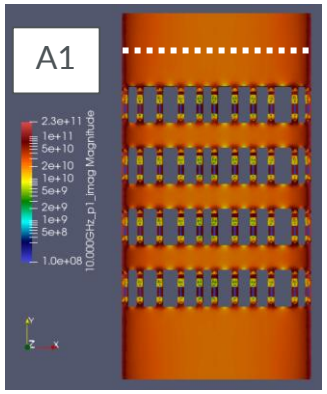
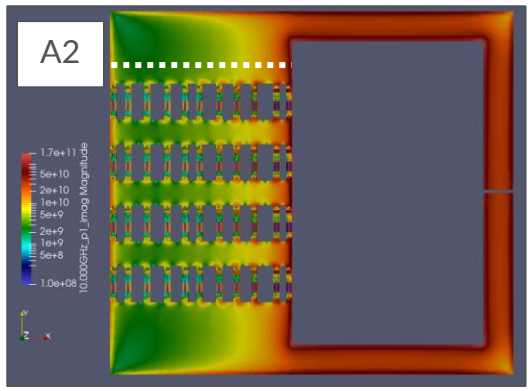
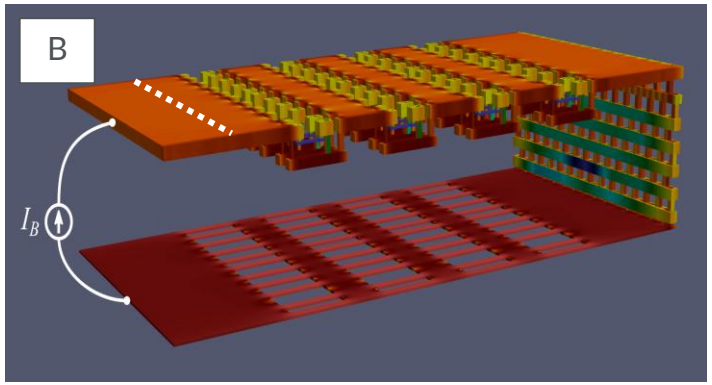
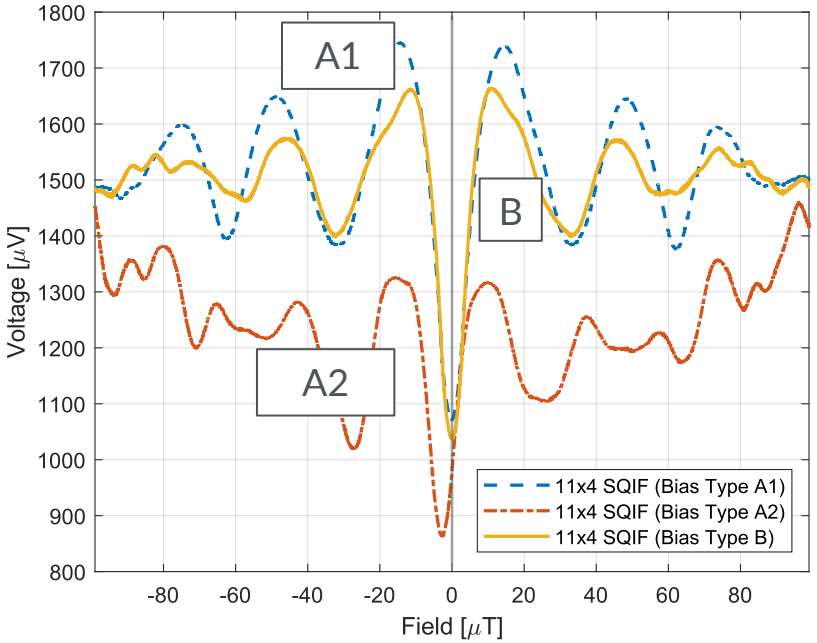
Compact models: SQIF analysis

- Under the IARPA SuperTools Project, we developed design automation tools for extracting high-fidelity models for superconductor integrated circuits.
- **These tools can be used for compact models of 2D SQIF arrays.**
  - These compact models include all mutual inductances.
  - Support external magnetic field excitations.
  - Compatible with existing circuit simulators: JoSIM, WRspice, etc.
  - Streamlines SQIF design and evaluation process.









VB-response of 4x11 SQIF array with different biasing techniques.

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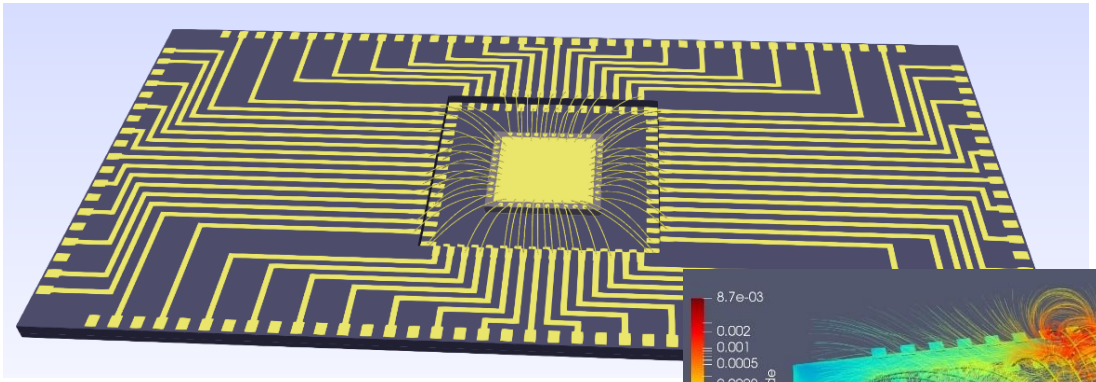
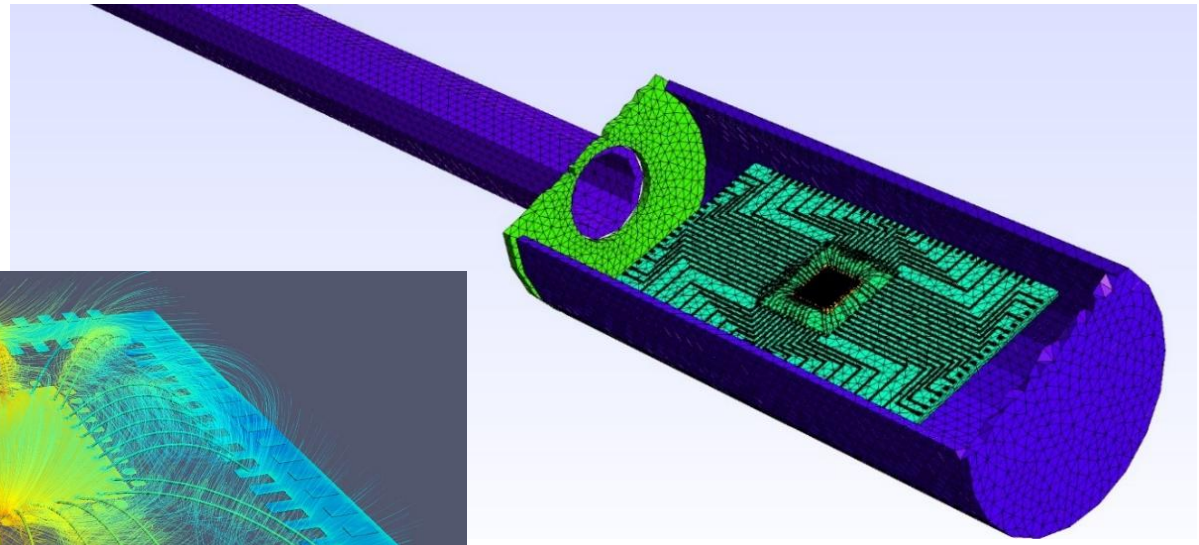
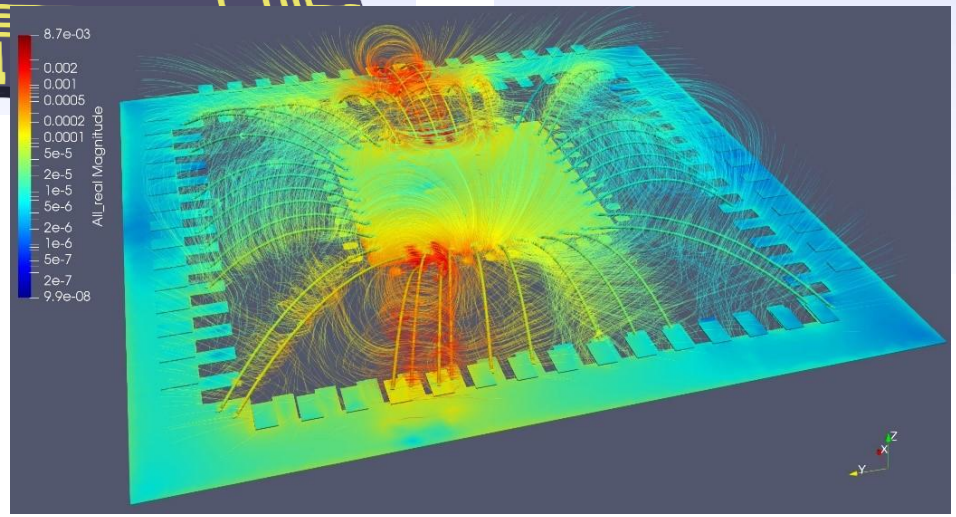
Packaging and shielding analysis

- Full chip-in-package with shields, wire/bump bonds
- Use IXI/mesh exports to include enclosure effects







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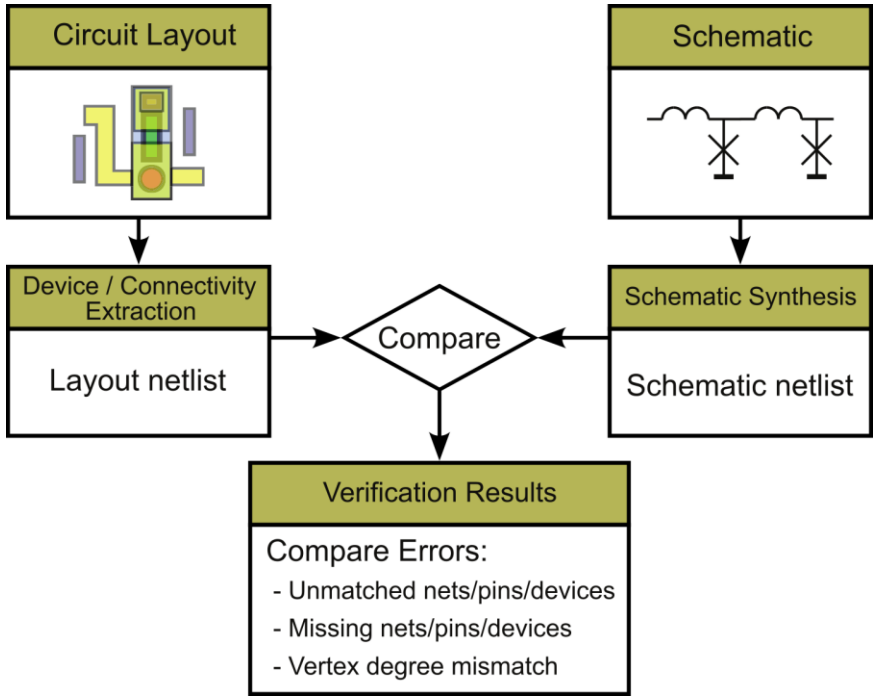
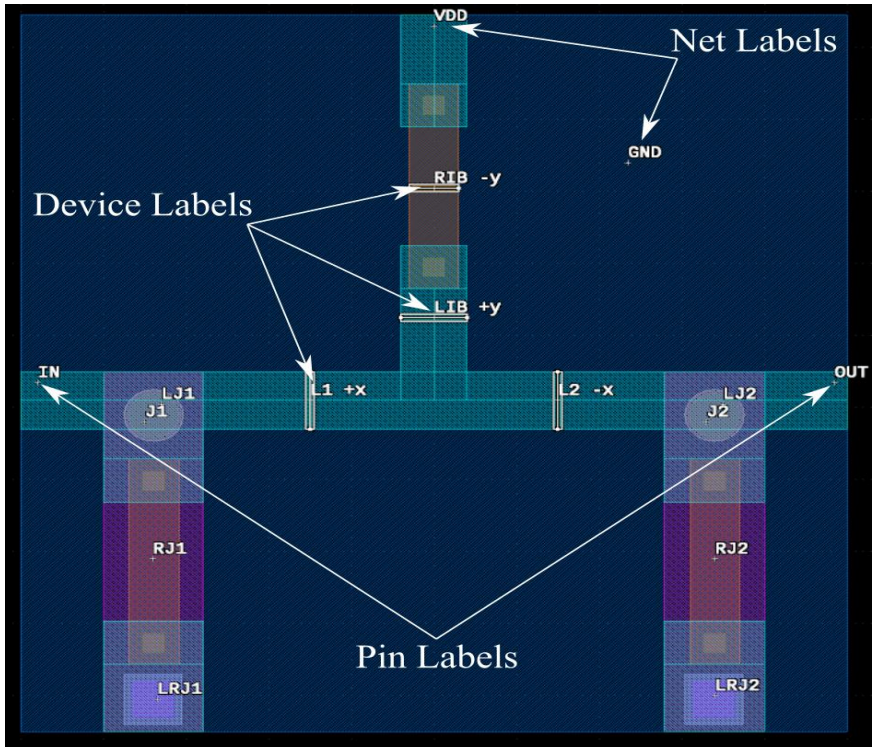
From extraction to verification

Topology checks + magnetic-coupling sanity checks

InductEx-LVS: Layout-versus-Schematic Verification

- **LVS for superconducting layouts:**
  - Compares layout topology ↔ schematic netlist
  - Device recognition: JJs, resistors, inductors, vias, interconnect
  - Goal: catch connectivity mistakes early (especially multi-layer stacks)





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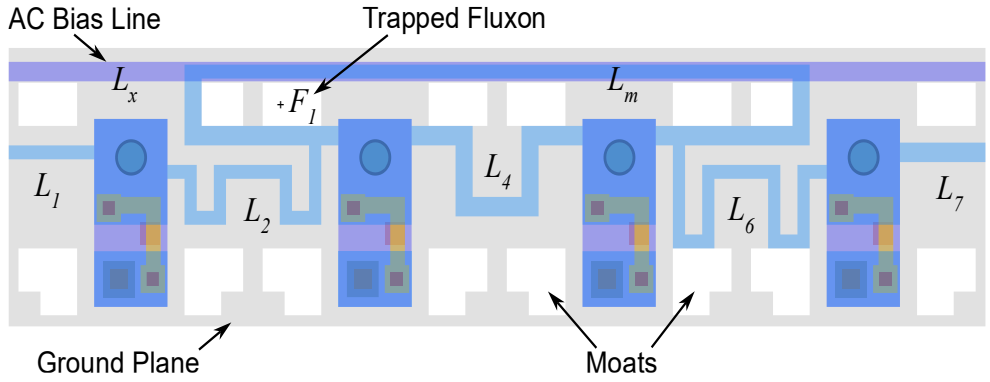
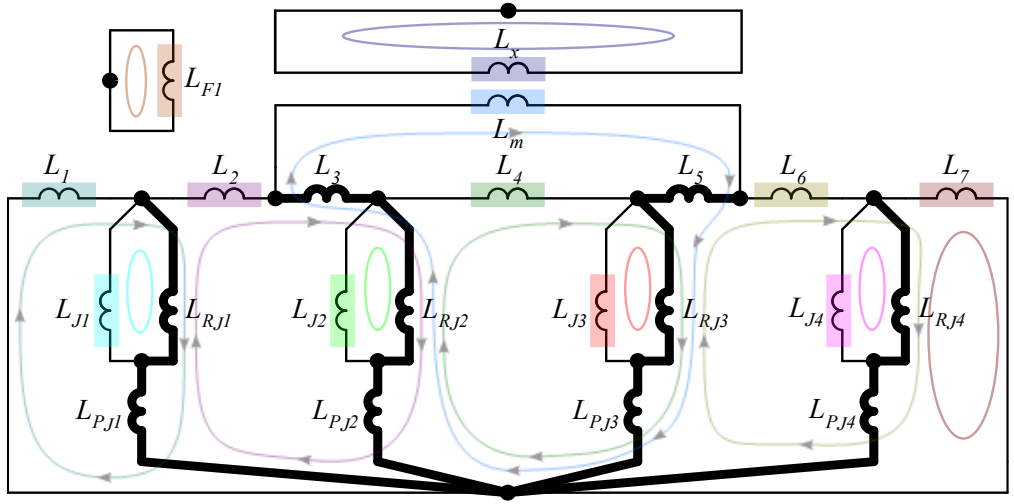
CheckNet: Automatic Identification of Magnetic Couplings

- Build the full inductance matrix
- Flag missing/invalid couplings; highlight strong/weak links
- Use graph views to spot unintended paths



Layout of AC-biased RSFQ shift register



Graph representation of circuit diagram

	L_1	L_2	L_4	L_6	L_7	L_{F1}	L_{J1}	L_{J2}	L_{J3}	L_{J4}	L_M	L_x
L_1	L_1	•	$M_{1,4}$	$M_{1,6}$	$M_{1,7}$	$M_{1,F1}$	$M_{1,J1}$	$M_{1,J2}$	$M_{1,J3}$	$M_{1,J4}$	$M_{1,M}$	$M_{1,x}$
L_2		L_2	•	$M_{2,6}$	$M_{2,7}$	$M_{2,F1}$	•	$M_{2,J2}$	$M_{2,J3}$	$M_{2,J4}$	•	$M_{2,x}$
L_4			L_4	$M_{4,6}$	$M_{4,7}$	$M_{4,F1}$	$M_{4,J1}$	•	$M_{4,J3}$	$M_{4,J4}$	•	$M_{4,x}$
L_6				L_6	•	$M_{6,F1}$	$M_{6,J1}$	$M_{6,J2}$	$M_{6,J3}$	$M_{6,J4}$	•	$M_{6,x}$
L_7					L_7	$M_{7,F1}$	$M_{7,J1}$	$M_{7,J2}$	$M_{7,J3}$	•	$M_{7,M}$	$M_{7,x}$
L_{F1}						L_{F1}	$M_{F1,J1}$	$M_{F1,J2}$	$M_{F1,J3}$	$M_{F1,J4}$	$M_{F1,M}$	$M_{F1,x}$
L_{J1}							L_{J1}	$M_{J1,J2}$	$M_{J1,J3}$	$M_{J1,J4}$	$M_{J1,M}$	$M_{J1,x}$
L_{J2}								L_{J2}	$M_{J2,J3}$	$M_{J2,J4}$	$M_{J2,M}$	$M_{J2,x}$
L_{J3}									L_{J3}	$M_{J3,J4}$	•	$M_{J3,x}$
L_{J4}										L_{J4}	$M_{J4,M}$	$M_{J4,x}$
L_M											L_M	$M_{M,x}$
L_x												L_x

Full inductance matrix with valid couplings (dots indicate invalid couplings)

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Frequency-dependent behaviour

MQS + EQS → Z_0, delay; EMQS/full-wave for filters & resonators

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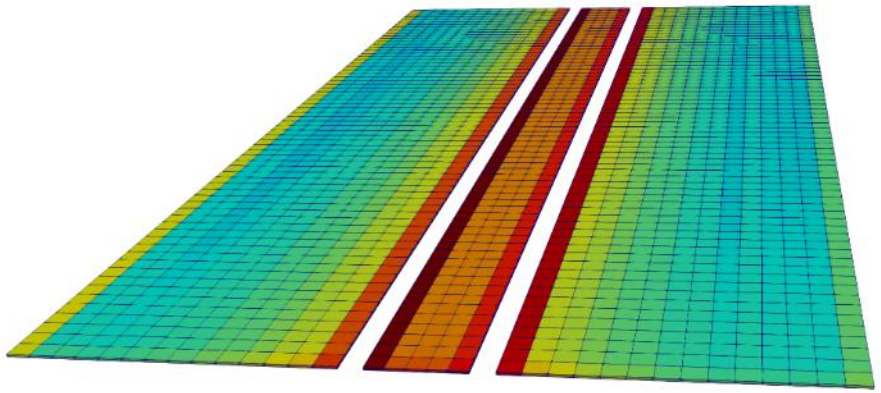
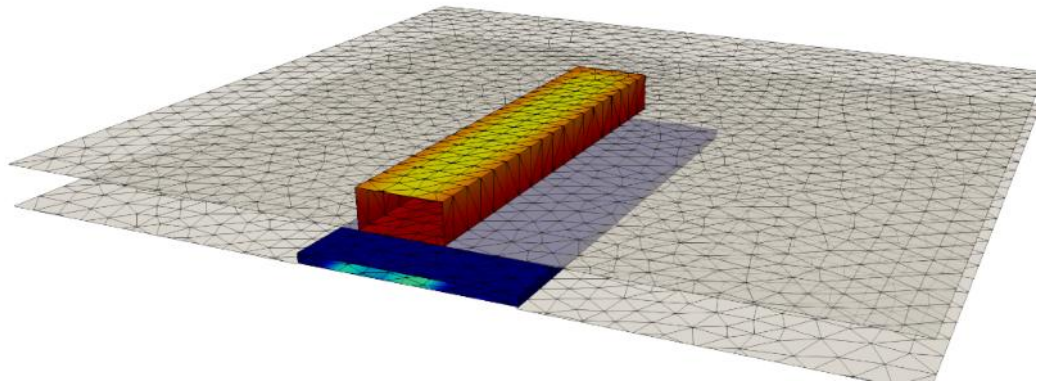
Frequency-dependent characteristics

- Use MQS (inductance) and EQS (capacitance) solutions, find Z_O.
  - Useful for microstrip, stripline, CPW, etc.
  - Multiple dielectric boundaries supported in EQS, EMQS mode.



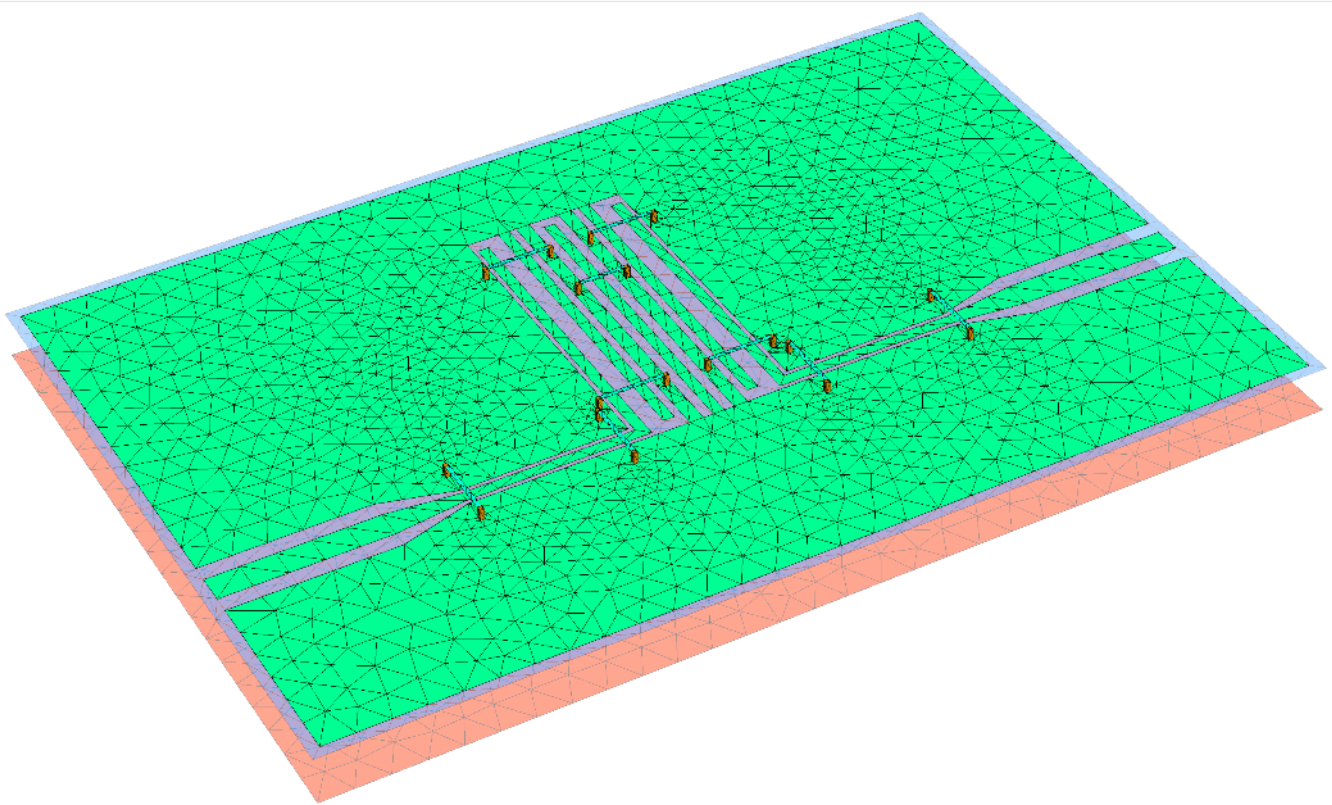


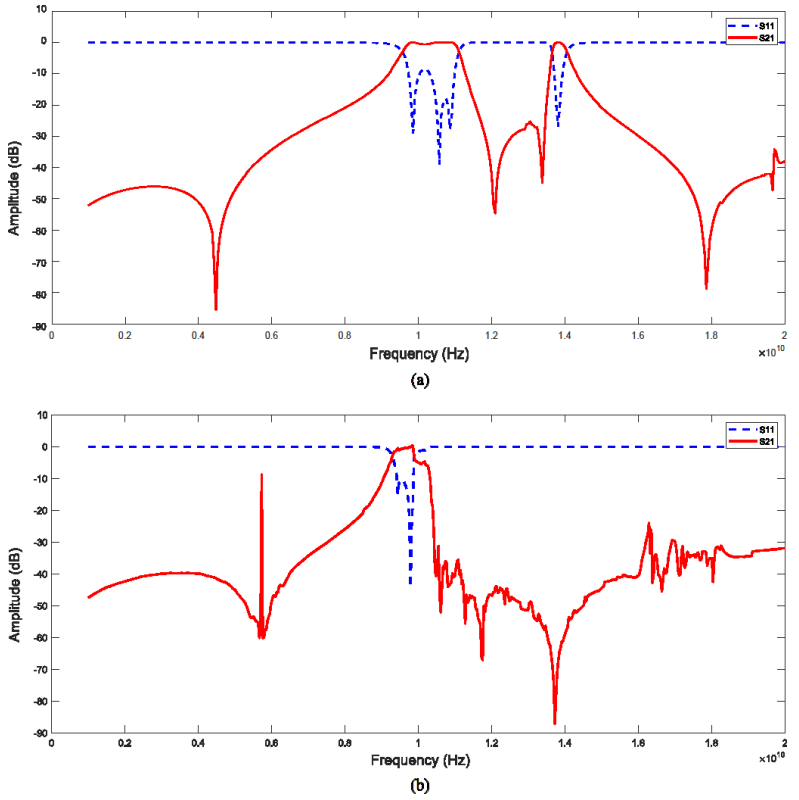
```
Transmission line structure between ports Z1 and Z2

Z = 27.947 ohms
L = 3.1636E-12 H
C = 4.0506E-15 F
T = 0.0075467 ps/um
v = 132.51 um/ps
Distance = 15 um
```

Frequency-dependent characteristics

- EMQS/Full-wave: filters





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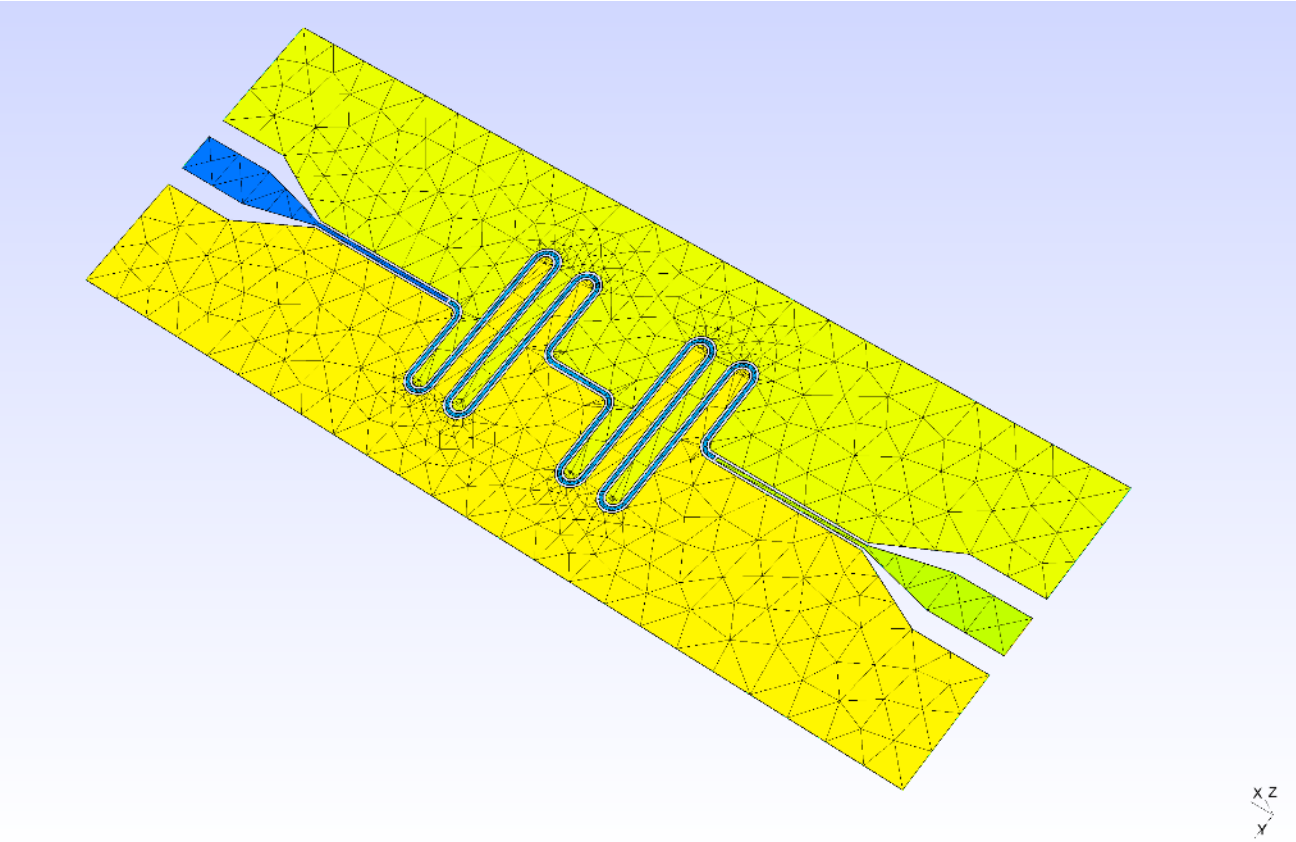
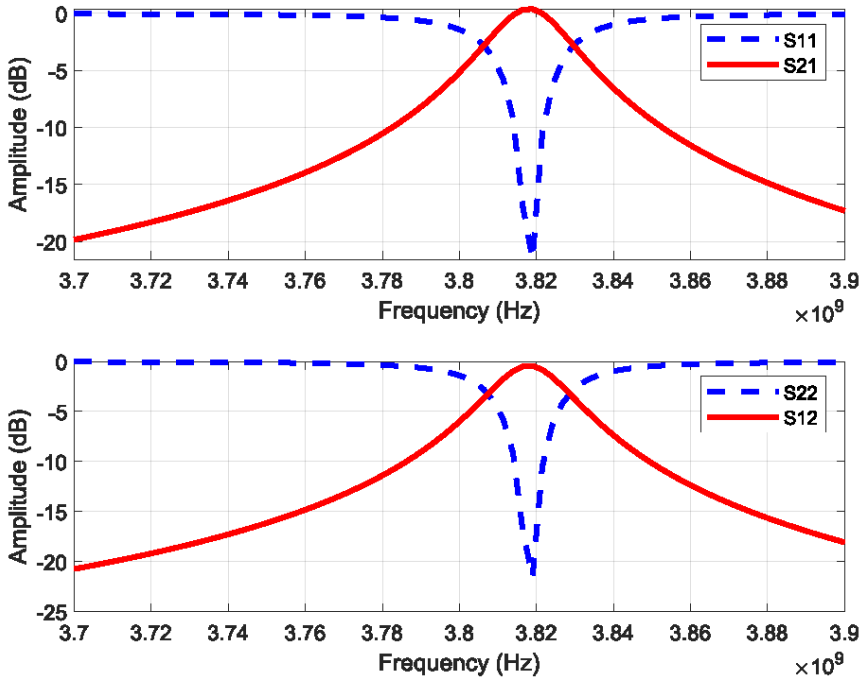
Frequency-dependent characteristics

- EMQS/Full-wave: resonators



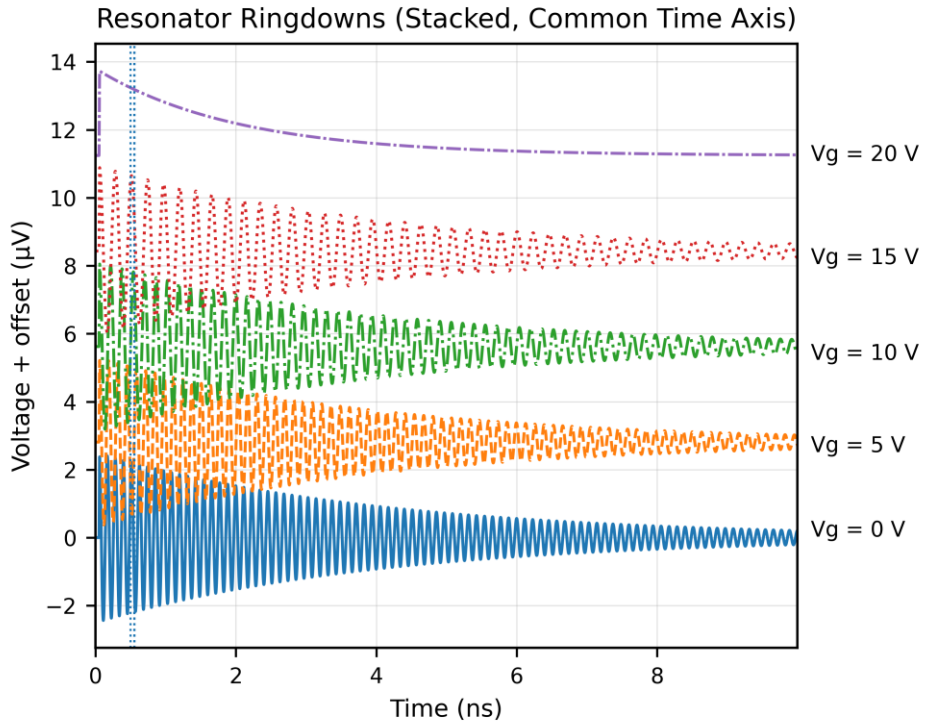


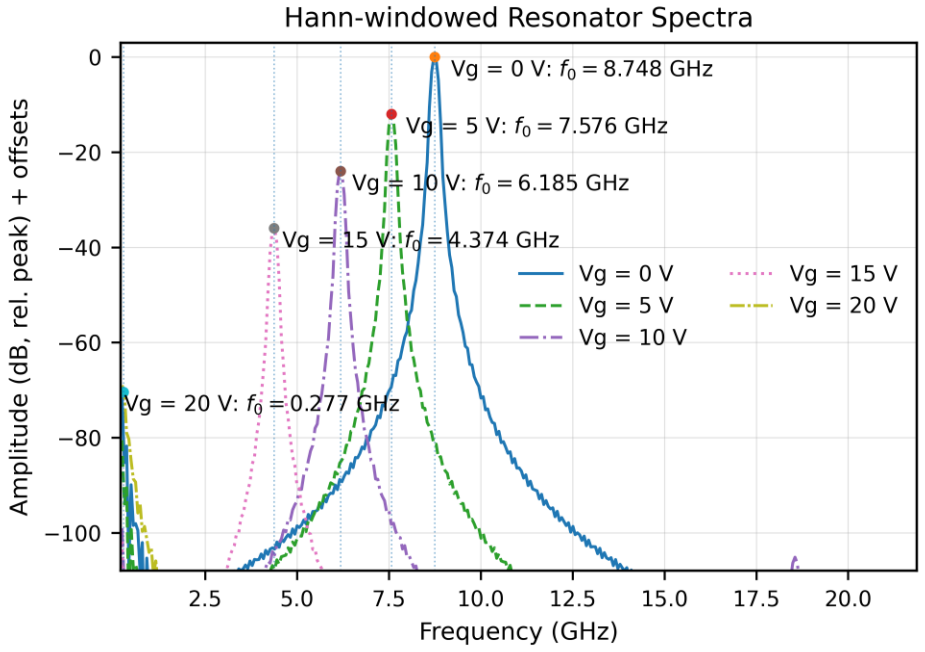
Analog simulation under quantum conditions

From JJ device models → circuit-level behaviour

JoSIM Improvements

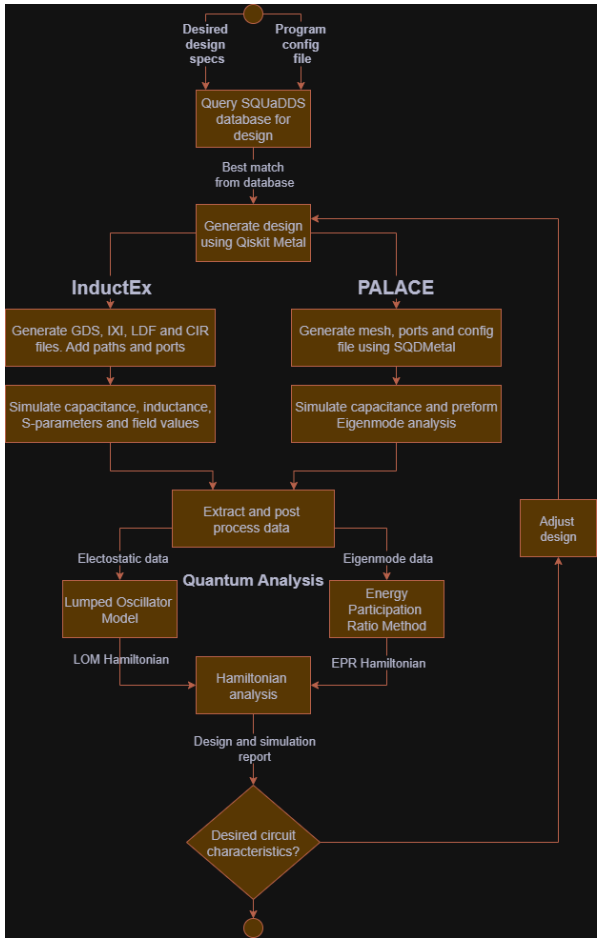
- Electrostatic Gate-Tunable Josephson Junctions in JoSIM (Gatemons) [8]

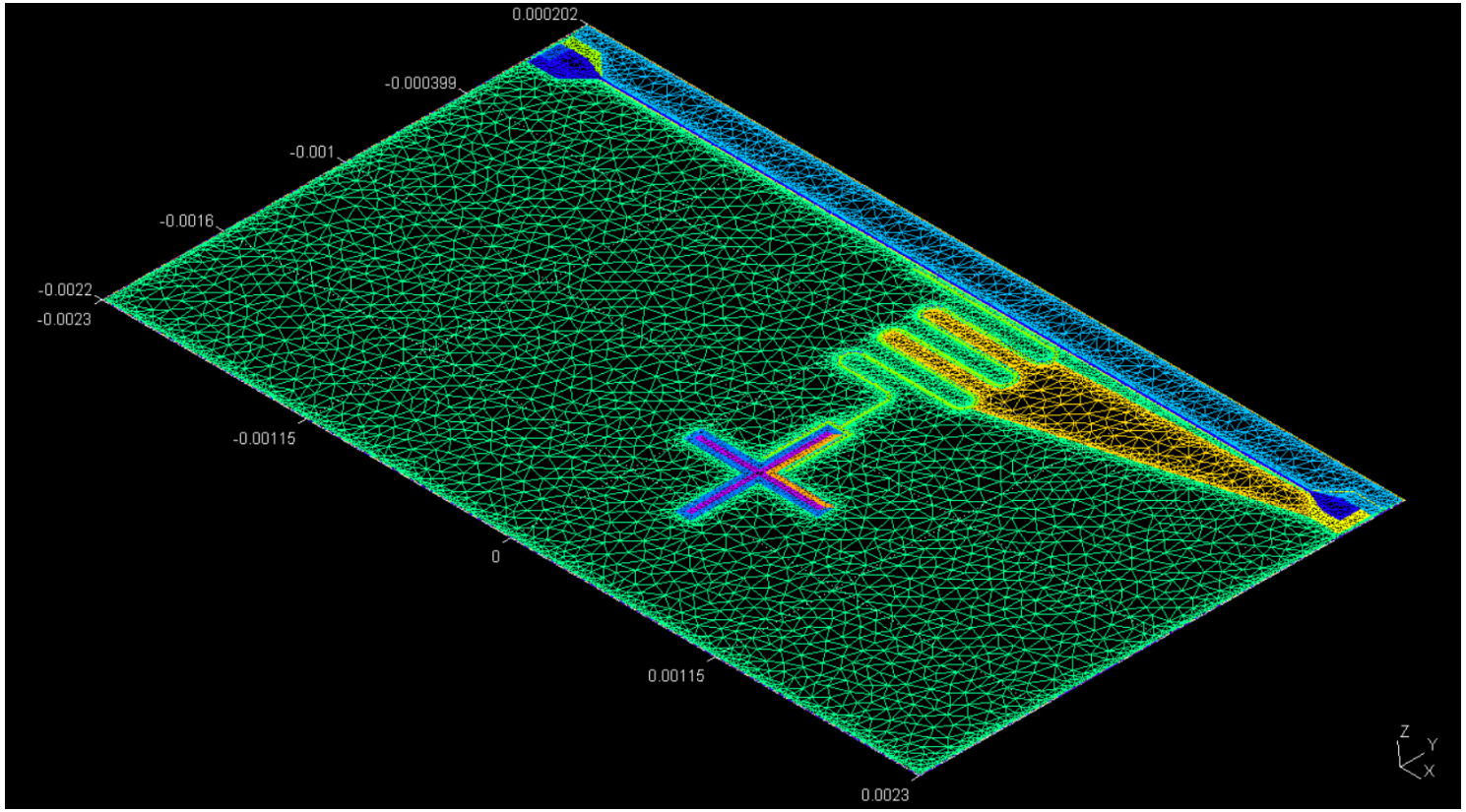




[8] J. A. Delport and O. Chen, "Electrostatic Gate-Tunable Josephson Junctions in JoSIM: Modeling, Simulation, and I–V Characterization," *IEEE Trans. Appl. Supercond.*, doi: 10.1109/TASC.2025.3617516.

Automated Hamiltonian extraction (work-in-progress)





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Early results (LOM)

- First comparisons: InductEx/TetraHenry vs Palace/HFSS reference
- Differences trace to kinetic-inductance + dielectric modelling
- Next: refine stack params; add EPR

Parameter	Design	Δ%	HFSS Reference	Δ%	$HFSS_{LOM}$	Δ%	$InductEx_{LOM}$	Δ%	$PALACE_{LOM}$	Δ%
Qubit Frequency (F_q) (GHz)	1.8000	-	1.8176	+0.98%	1.8163	+0.91% -0.07%	1.8560	+3.11% +2.11%	1.8282	+1.57% +0.59%
Cavity Frequency (F_c) (GHz)	4.2000	-	5.1226	+21.97%	5.0670	+20.64% -1.09%	4.1820	-0.43% -18.36%	5.0969	+21.35% -0.50%
Anharmonicity (α) (MHz)	-120.00	-	-122.81	+2.34%	-122.57	+2.14% -0.19%	-129.09	+7.57% +5.11%	-124.52	+3.77% +1.39%

Conclusion

- **Takeaways:**
  - Physics-aware extraction + verification + circuit modelling are the enablers
  - Field practice: validate against measurement/simulation references
  - Open questions: materials (εr, loss), packaging fields, scalable workflows
  - Invitation: compare methods, share datasets, co-validate

- **Thank you!**

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