IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), January 2017 (Preview 1).
Preprint of ASC 2016 manuscript 4EOr3A-04 submitted to *IEEE Trans. Appl. Supercond.* for possible publication.
DOI: 10.1109/TASC.2016.2646926

Energy-Efficient and Compact ERSFQ Decoder for Cryogenic RAM

I. V. Vernik, *Senior Member, IEEE,* A. F. Kirichenko, O. A. Mukhanov, *Fellow, IEEE,* and T. A. Ohki

***Abstract*—We report on the development of energy-efficient decoders for cryogenic random access memory and register file. To reduce the pitch, area, and energy, our decoder employs a scalable binary tree architecture. We implemented these decoders using ERSFQ logic controlled by magnetically coupled address lines. These lines are driven by energy-efficient drivers based on the current-stirring technique. A 4-to-16 version of the decoder was laid out and fabricated in HYPRES 6-layer 10 kA/cm^2 and MIT LL 8-layer 10 kA/cm^2 processes with 15 μm and 28 μm decoder row pitch, respectively. The decoders were designed to have ~ 30 ps latency and dissipate ~ 40 aJ per clock. We experimentally confirmed the functionality of the circuits with ±8% dc bias margins and verified its operation up to 13 GHz clock.**

***Index Terms*—energy-efficient logic, random access memory, cryogenic magnetic memory, RSFQ, SFQ.**

I. Introduction

SUPERCONDUCTING energy-efficient single flux quantum circuits [1]-[3] have been identified as a promising technology for the next generation high-end computing systems [3], [4]. The design of energy-efficient computers requires the development of high-density, low-p cryogenic random access memories (RAMs) [5]-[9] register files [10] with short access and cycle times.

Typically RAM and register file are organized as a mer cell matrix addressable using n-to-2^n address decoders, w n is a number of address bits. For the efficient design, decoder has to be low power and match dimensions (pitc that of memory cell rows or columns as close as poss There are several known decoder design types impleme using superconducting circuits: loop decoders, tree deco NOR and NAND decoders [11]-[22]. The first decoder b on energy-efficient ERSFQ logic [1] was described in This 4-to-16 bit decoder was implemented using Hypre layer process with 4.5 kA/cm^2 critical current der occupied 0.7 x 1.8 mm^2 and dissipated ~70 aJ per one ad decode operation. The pitch of output decoder rows wa μm. While this decoder design was successful, its complexity and power scales as $n2^n$. The pitch has to be further reduced to match our design objectives for high-density memory matrices.

In this paper, we present a new ERSFQ decoder based on a binary tree architecture featuring 2^n scaling and with significantly more compact layout enabled by advanced fabrication processes developed at Hypres and at MIT-LL.

II. Design

A. Decoder with Binary Tree Architecture

Fig. 1 shows a block diagram of the n-to-2^n bit address decoder with a binary tree architecture. It consists of n address line drivers. In contrast to our previous decoder design with $n2^n$ decoder cells [23], the binary tree architecture requires only 2^n-1 decoder cells. With energy efficiency being one of the primary goals of this design, the binary tree approach has a significant power scaling advantage (~ factor of n) comparing to the previous matrix design.

When an address sequence (A_0, A_1, ...) arrives at the decoder

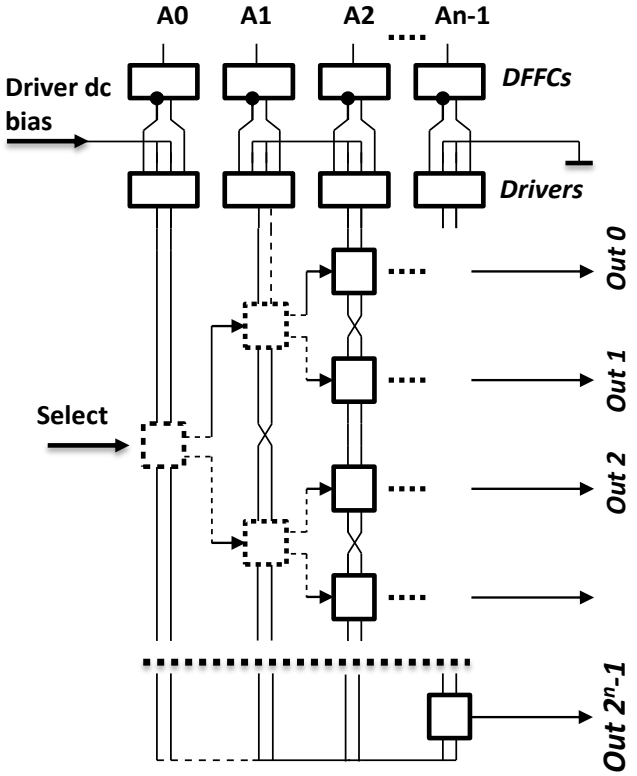

Fig. 1. Block diagram of the binary tree decoder.

Automatically generated dates of receipt and acceptance will be p here; authors do not produce these dates. The research is based upon supported by the Office of the Director of National Intelligence (O Intelligence Advanced Research Projects Activity (IARPA), via cor W911NF-14-C0089 and W911NF-14-C0090. The views and conclu contained herein are those of the authors and should not be interpret necessarily representing the official policies or endorsements, either expr or implied, of the ODNI, IARPA, or the U.S. Government. The Government is authorized to reproduce and distribute reprints Governmental purposes notwithstanding any copyright annotation thereo

A. F. Kirichenko, I. V. Vernik, and O. A. Mukhanov are with HYP Elmsford, NY 10523 USA (e-mail: alex@hypres.com; vernik@hypres mukhanov@hypres.com).

T. A. Ohki is with Raytheon BBN Technologies, Cambridge, MA USA (e-mail: tohki@bbn.com).

currents for each input address bit. An address line driver [23] comprises an ERSFQ D flip-flop with complementary outputs (DFFC) that generates SFQ control signals for the dc-powered current steering loop driver [22]. For each column of the decoder, two complementary superconductive lines (A_n *and* $\bar{A}_n$) traverse the entire vertical dimension of the decoder (Fig. 1). Each cell of the decoder cell tree is magnetically coupled to one of the complementary lines. By commutating *An* and $\bar{A}n$ lines in the proper order, a unique combination of control currents can be achieved to address all 2^n outputs. This addressing allows for the select signal to propagate to the appropriate output, thus performing address decoding. Similarly to the earlier demonstrated decoder [23], once the address is set, the decoder settings do not change until another address is applied, allowing this circuit to be used also as a switch.

B. *Decoder Cell*

Fig. 2 shows a decoder cell based on SFQ switches controlled by dc currents via magnetic coupling. Each decoder cell (Fig. 2) consists of two dc-current driven SFQ switches. Each switch is magnetically coupled to one of two complementary lines. When the current is present in the line, the switch is in ON position - the incoming SFQ pulse can propagate through the switch. On the contrary, the absence magnetically induced current puts the switch in the OFF position, and the SFQ pulse escapes via the buffer junction. Thus, the decoder cell commutates its input to one of two outputs. When the corresponding address bit is "1" (line *A* is carrying current), the cell sends the input SFQ pulse to its output Out1. And when the address bit is "0" (line $\bar{A}$ is carrying current), the cell sends the input SFQ pulse to its output Out0.

Each decoder output from *Out0* to *Out2^n-1* has a unique combination of true and complement address lines, thus connecting it to the input of the tree.

We estimate the energy consumption for a single address change operation as

$$E_s = \delta n \cdot L \cdot I_{b2}^2 + n \cdot I_{b3} \cdot \Phi_0,$$

and for a single decoding operation:

$$E_d = (2^n\text{-}1) \cdot I_{b1} \cdot \Phi_0,$$

where

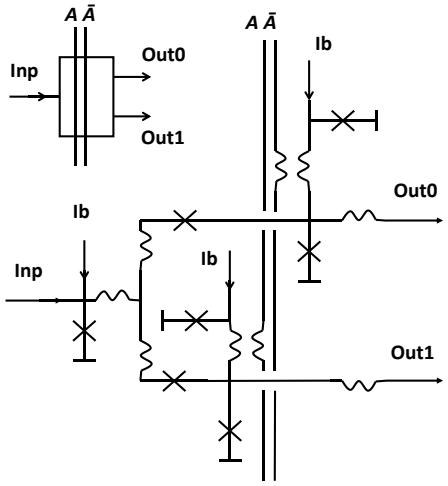

Fig. 2. Decoder cell symbol and schematics.

n – number of bits in decoder address (4)
δn – number of address bits that toggle (0-4)
I_{b1} – dc bias current of a decoder cell (~0.8 mA)
I_{b2} – dc bias current of a bit-line loop (~0.2 mA)
I_{b3} – dc bias current for a DFFC and a driver (~ 1.0 mA)
L – inductance of the bit control line (~ $2^n \cdot 6.0$ pH)

This gives a total energy estimate $E_s + E_d$ for $n = 4$ (4-to-16 decoder) for a single operation as ~40 aJ.

The addressing time of the decoder (i.e., time of address setting) is the time to charge/discharge current from control lines, that is estimated as ~100 ps [23]. The select time is the time delay for SFQ pulse propagating from input to output. For $n = 4$ and at 10 kA/cm^2 process, it can be estimated based on our simulations as 30 ps at nominal bias. Therefore, the total cycle time for decoder is ~ 130 ps.

III. Layout

The important layout design requirement for the address decoder is to match the decoder row dimension (vertical pitch) to the vertical dimension of memory array row defined by memory cell size. For magnetic RAMs (MRAMs), we are working on the development of two different compact memory cells based on magnetic storage elements: cryogenic orthogonal spin transfer (COST) [6] or cryogenic spin-hall effect (CSHE) [24]. To form an addressable memory cell, the magnetic element is integrated with a three-terminal device, a cell selector. We are using three-terminal superconducting devices - nTron [25] and superconducting-ferromagnetic transistor (SFT) [26]-[27] devices. The target dimension of memory cells is a few microns. The initial versions of memory cells are of the order of 10-20 μm.

For register file, the size requirements are less stringent as the register file memory cell size is typically larger. It is based

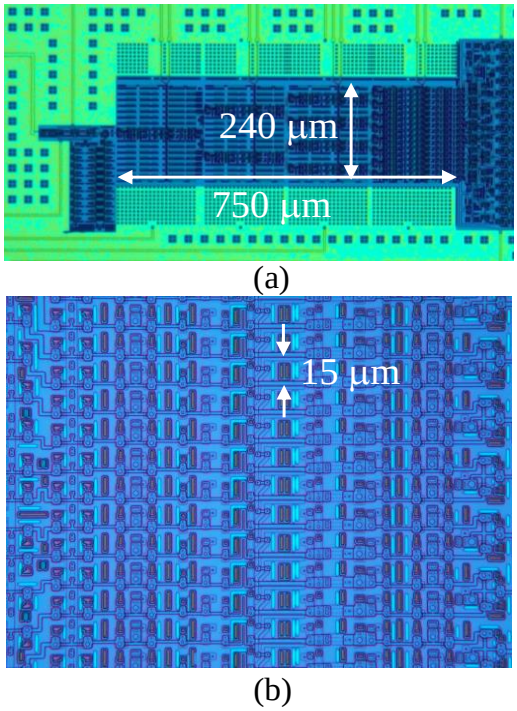

Fig. 3. (a) Micrograph of 4-to-16 bit decoder fabricated in HYPRES' 6-layer 10 kA/cm^2 process. (b) Zoom-in of sixteen decoder rows showing the pitch.

DOI: 10.1109/TASC.2016.2646926

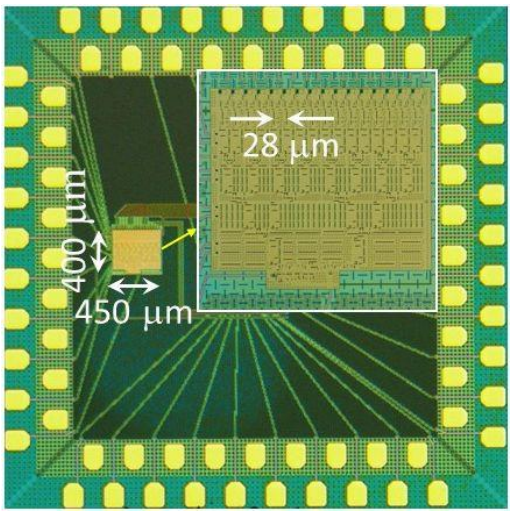

Fig. 4. Micrograph of a 4-to-16 bit decoder 5 x 5 mm^2 test chip fabricated in MIT LL 8-layer 10 kA/cm^2 process with inset showing decoder area in details.

first design is targeting MRAM. It is laid out for the implementation using HYPRES 10 kA/cm^2 process [28], which is an integral part of Integrated Memory Process (IMP) [29]. The second design is done for a register file applications and laid out for MIT-LL 10 kA/cm^2 fabrication process [30]. Both fabrication processes feature the high kinetic inductance (HKI) layer allowing the placement of the large ERSFQ bias inductors under the cells to reduce the decoder cell area.

Fig. 3(a) shows a micrograph of the decoder composed of 540 Josephson junctions (including ERSFQ bias JJs) fabricated using HYPRES' 6-layer process. The decoder occupies an area of 860 µm x 240 µm. The binary tree architecture, smaller feature size and introduction of NbN_x HKI layer resulted in a ~6x area reduction when compared to the decoder realized earlier [23]. Fig. 3(b) shows a closeup of the output section of the decoder with sixteen output rows. As one can see, the pitch of decoder outputs is 15 µm - a significant reduction from 50 µm in [23] realized with HYPRES' legacy 4-layer, 1.0-µm process with 4.5 kA/cm^2 critical current density.

Fig. 4 shows a micrograph of the decoder test chip fabricated using MIT-LL 8-layer Nb process. The decoder occupies an area of 450 µm x 400 µm. This version of the decoder utilizes 480 Josephson junctions. The pitch of the decoder outputs was 28 µm (see insert to Fig. 4 for more details). A complete version of the decoder with the earlier demonstrated current drivers [23] is being designed.

IV. Experimental Results

A. Low-Speed Functionality Test

We have performed functionality testing of the decoder matrix fabricated using MIT-LL process. The fabricated chips were mounted in flip-chip cryoprobe. The chip was measured at 4.2 K temperature with multilayer mu-metal providing necessary magnetic shielding. Evaluation of 4-bit decoder functionality and dc bias current margins measurements were performed with multifunctional test system OCTOPUX [31].

We successfully tested the 4-to-16 bit decoder matrix. Fig. 5 shows the correct functionality of the fabricated decoder for all possible 16 addresses. The pattern includes: (a) a test pattern comprising a train of SFQ pulses (select) being sent to the input; (b) the address control dc current patterns (*A0*, $\bar{A0}$,

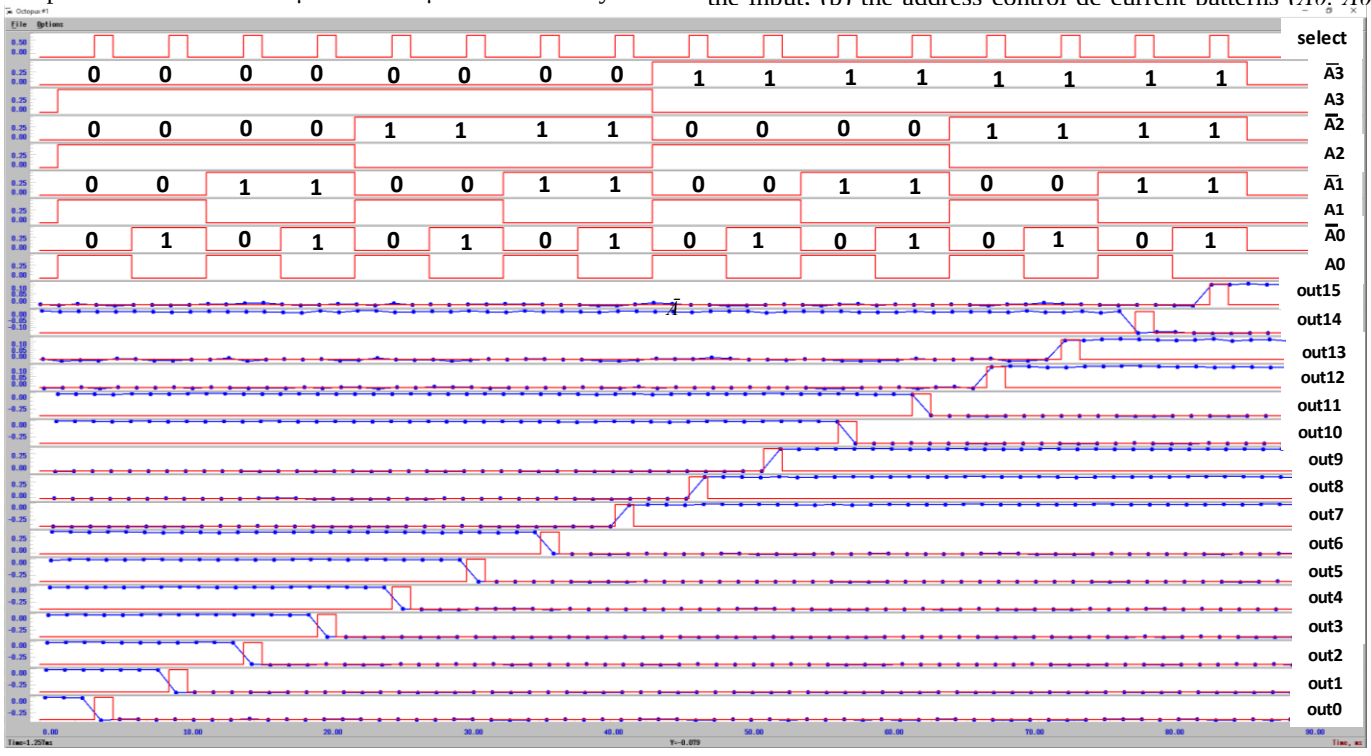

Fig. 5. Functionality test of the 4-bit decoder. Correct operation was verified for all various 16 addresses with dc bias current operational margins measured. The red traces indicate select signal (select) and expected outputs (Out0 – Out15). The blue traces with dots are the measured decoder outputs via standard toggle flip-flop SFQ/dc converters.

A1, Ā1 A2, Ā2, A3 and Ā3) applied to provide all possible addresses from 0 to 15; (c) sixteen outputs from the decoder matrix being measured via standard toggle flip-flop SFQ/dc converters. The measured output pattern confirms the correct operation for all possible 16 addresses (from 0000 to 1111) observed on all outputs from *Out0* to *Out15*. The correct operation was confirmed for this exhaustive address pattern with bias margins ±8%.

For the ERSFQ circuitry the dc bias is provided by Josephson transmission line through large superconducting inductors. We estimate that FJTL should exceed ~25% of total dc bias current [32]. The decoder with the larger FJTL has already been designed for HYPRES 10 kA/cm^2 6-layer process with HKI NbN layer. Although, the introduction of the feeding JTL reduced the overall energy-efficiency of the stand-alone decoder by raising the required bias current with ~30% of total bias being drawn by FJTL; it is also resulted in improvement of the operational bias margins. When decoder is integrated into a larger circuit, e. g., into MRAM or register file, the role of FJTL will be taken by other circuits such as a clock distribution network.

B. High-speed test

In order to perform high-speed test, we employed a similar to one demonstrated in [33], [34] technique. We apply a high-speed select signal from the high-frequency generator, while with two 8-channel oscilloscopes synchronized to the address pattern generators. When the output is "0" with no pulses coming to the converter, the output will be a static voltage level either 0 or V_{max}. Alternatively, if a high-speed stream of SFQ pulses is coming to the converter, it oscillates with the clock frequency resulting in average voltage level between two voltage states at ~ $V_{max}/2$. Using the low frequency oscilloscope, the "0" will be represented with a double line, and "1" – as a single "fat" line.

Fig. 6(a) shows the oscilloscope screenshot of the signals applied to the *A0, Ā0,… A3* and *Ā3* address lines from eight synchronized generators at 20, 10, 5 and 2.5 kHz, respectively. The address pattern was similar to the one in Fig. 5.

Fig. 6 shows the correct operation of the 4-to-16 ERSFQ decoder at 13 GHz clock frequency with the applied address pattern shown in Fig. 6(a) (similar to one shown in Fig. 5). Fig. 6(b) depicts the first eight outputs (*Out0* - *Out7*) monitored with an 8-channel oscilloscope. The similar pattern was observed on the other eight outputs (*Out8* - *Out15*) with the correct phase shift relatively to the address pattern, i.e. the phase shift between *Out7* and *Out8* was identical to the one between any other two consecutive outputs. We should mention, that the circuit under test was not adapted for high-speed testing, i.e. the input DC/SFQ converter was a low-speed version and did not match the 50-Ohm impedance. With upgrading DC/SFQ converter to its high-frequency version, the maximum frequency at which the decoder is operating will

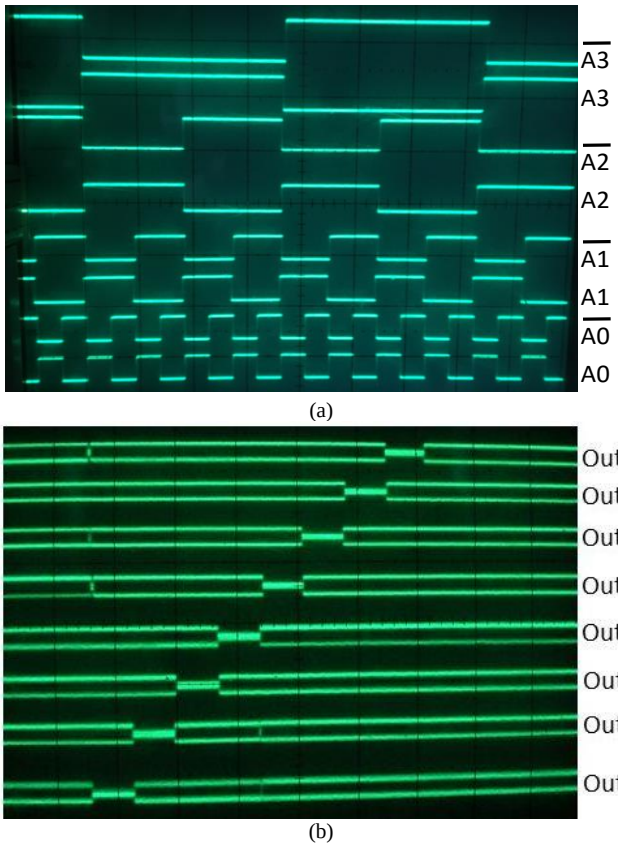

Fig. 6. High-speed test of the decoder. a) Signals applied to the *A0, Ā0… A3* and *Ā3* address lines from 8 synchronized generators. b) A 13-GHz test of the 4-to-16 ERSFQ decoder with first 8 output being shown

…its using a scalable
…pective MRAM and
…nted two different
…he first design was
…Memory Process and
… of output decoder
…ws in MRAM. The
…IT-LL process and
…egister file in a

…s was to minimize
…ed using a space-
…eme dissipating no
…atively small power
… ding is done by the
… power dissipation
…energy consumption
…is 40 aJ per address

…YPRES fabrication
…nt, and D. Amparo and MIT-LL fabrication team. We are also grateful to G. Gibson, S. Rylov, and L. Albu for useful discussions.

Preprint of ASC 2016 manuscript 4EOr3A-04 submitted to *IEEE Trans. Appl. Supercond.* for possible publication.
DOI: 10.1109/TASC.2016.2646926

REFERENCES

[1] D. Kirichenko, S. Sarwana, A. Kirichenko, "Zero static power dissipation biasing of RSFQ circuits," *IEEE Trans. Appl. Supercon*., vol. 21, pp.776-779, Jun. 2011

[2] O. A. Mukhanov, "Energy-efficient Single Flux Quantum technology," *IEEE Trans. Appl. Supercond.*, vol. 21, pp.760-769, Jun. 2011.

[3] Q. Herr, A. Herr, O. Oberg, A. Ioannidis, "Ultra-low-power superconductor logic," *J. Appl. Phys.*, vol. 109, 2011. Art. No. 103903.

[4] M. A. Manheimer, "Cryogenic Computing Complexity Program: Phase 1 Introduction," *IEEE Trans. Appl. Supercond*., vol. 25, no. 3, Jun. 2015, Art. No. 13017004.

[5] D. S. Holmes, A. L. Ripple, M. A. Manheimer, "Energy-efficient superconducting computing – power budgets and requirements," *IEEE Trans. Appl. Supercond*., vol. 23, Jun. 2013, Art. No. 1701610.

[6] L. Ye, D. B. Gopman, L. Rehm, D. Backes, G. Wolf, T. Ohki *et al.*, "Spin-transfer switching of orthogonal spin-valve devices at cryogenic temperatures," *J. Appl. Phys.*, vol. 115, 2014. Art. No. 17C725.

[7] I. V. Vernik, V. V. Bol'ginov, S. Bakurskiy, A. A. Golubov *et al.*, "Magnetic Josephson junctions with superconducting interlayer for cryogenic memory," *IEEE Trans. Appl. Supercond.*, vol. 23, Jun. 2013, Art. No. 1701208.

[8] B. Niedzielski, S. Diesch, E. Gingrich, Y. Wang, R. Loloee *et al.*, "Use of Pd–Fe and Ni–Fe–Nb as Soft Magnetic Layers in Ferromagnetic Josephson Junctions for Nonvolatile Cryogenic Memory," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 4, Aug. 2014, Art. No. 1800307.

[9] B. Baek, W. Rippard, S. Benz, S. Russek, and P. Dresselhaus, "Hybrid superconducting-magnetic memory device using competing order parameters," *Nature Comms*., vol. 5, May 2014, Art. No. 3888.

[10] A. F. Kirichenko, A. Sahu, T. V. Filippov, O. A. Mukhanov, A. Dotsenko, M. Dorojevets, A. K. Kasperek, "Demonstration of an 8×8-bit RSFQ multi-port register file," *2013 IEEE 14th Int. Supercond. Electron. Conf. (ISEC)*, p. A2, 7-11 July 2013.

[11] W. Henkels and H. Zappe, "An experimental 64 bit decoded Josephson NDRO random access memory array," *IEEE J. Solid-State Cir*. vol. 13, no. 5, pp. 591-600, Oct. 1978.

[12] S. Nagasawa, Y. Hashimoto, H. Numata, S. Tahara, "A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield," *Applied IEEE Trans. Appl. Supercond.* vol. 5, no. 2, pp. 2447-2452, Jun. 1995.

[13] P. F. Yuh, "A 2-kbit superconducting memory chip, *IEEE Trans. Appl. Supercond.* vol. 3, no. 2, pp. 3013-3021, Jun. 1993.

[14] T. Van Duzer, L. Zheng, S. Whiteley, H. Kim, J. Kim, *et al.*, "64-kb hybrid Josephson-CMOS 4 Kelvin RAM with 400 ps access time and 12 mW read power," *IEEE Trans. Appl. Supercond.* vol. 23, no. 3, Jun. 2013, Art. No. 1700504.

[15] S. M. Faris, "Loop decoder for Josephson memory arrays," *IEEE J. Solid-State Cir*. vol. 14, no. 4, pp. 699-707, Aug. 1979.

[16] A. F. Kirichenko, V. K. Semenov, Y. K. Kwong, V. Nandakumar, "4-bit Rapid Single-Flux-Quantum decoder, *IEEE Trans. Appl. Supercond*. vol. 5, no. 2, pp. 2857-2860, Jun. 1995.

[17] M. Tanaka, R. Sato, Y. Hatanaka, and A. Fujimaki, "High-density shift-register-based rapid single-flux-quantum memory system for bit-serial microprocessors," *IEEE Trans. Appl. Supercond*. vol. 26, no. 5, Aug. 2016, Art. No. 1301005.

[18] S. Nagasawa, H. Hasegawa, T. Hashimoto, H. Suzuki, K. Miyahara, Y. Enomoto, "Design of a 16 kbit superconducting latching/SFQ hybrid RAM," *Supercond. Sci. Technol.*, vol. 12, no. 11, pp. 933–936, Nov. 1999.

[19] A. F. Kirichenko, O. A. Mukhanov, and D. K. Brock, "A Single Flux Quantum cryogenic random access memory," *Ext. Abstracts of 7th Int. Supercond. Electron. Conf. (ISEC'99)*, Berkeley, USA, pp. 124-127, 1999.

[20] A. F. Kirichenko, S. Sarwana, D. K. Brock, M. Radparvar, "Pipelined dc-powered SFQ RAM," *IEEE Trans. Appl. Supercond*. vol. 11, no. 1, pp. 537-540, Mar. 2001.

[21] P. Bunyk, A. Y. Kidiyarova-Shevchenko, and P. Litskevich, "RSFQ microprocessor: new design approach," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2697–2704, Jun. 1997.

[22] S. Nagasawa, K. Hinode, T. Satoh, Y. Kitagawa, M. Hidaka, "Design of all-dc-powered high speed single flux quantum random access memory based on a pipelined structure for memory cell array," *Supercond. Sci. Technol.*, vol. 19, no. 11, pp. 325–330, Mar. 2006.

[23] A. F. Kirichenko, I. V. Vernik, O. A. Mukhanov, and T. A. Ohki, "ERSFQ 4-to-16 decoder for energy-efficient RAM," *IEEE Trans. Appl. Supercond.*, vol. 25, Jun. 2015, Art. No. 1301304.

[24] S. V. Aradhya, G. E. Rowlands, J. Oh, D. C. Ralph, and R. A. Burman, "Nanoscale-timescale low energy switching of in-plane magnetic tunnel junctions through dynamic oersted-field-assisted spin-hall effect," *Nano Lett.*, Jun. 2016.

[25] A. N. McCaughan and K. K. Berggren, "A superconducting-nanowire three-terminal electrothermal device," *Nano Lett.*, vol. 14, no. 10, pp. 5748–5753, Sep. 2014.

[26] I. P. Nevirkovets, O. Chernyashevskyy, G. V. Prokopenko, O. A. Mukhanov, and J. B. Ketterson, "Superconducting-ferromagnetic transistor," *IEEE Trans. Appl. Supercond*., vol. 24, Aug. 2014, Art. No. 1800506.

[27] I. P. Nevirkovets, O. Chernyashevskyy, G. V. Prokopenko, O. A. Mukhanov, and J. B. Ketterson, "Control of supercurrent in hybrid superconducting-ferromagnetic transistors," *IEEE Trans. Appl. Supercond*., vol. 25, Jun. 2015, Art. No. 1800705.

[28] D. T. Yohannes, R. T. Hunt, J. A. Vivalda, D. Amparo *et al.*, "Planarized, extendible, multilayer fabrication process for superconducting electronics," *IEEE Trans. Appl. Supercond.*, vol. 25, Jun. 2015, Art. No. 1100405.

[29] D. T. Yohannes, R. T. Hunt, J. A. Vivalda, D. Amparo *et al.*, "Development of Integrated Memory Process: Combining Josephson junctions, nanowire and magnetic devices into a single integrated circuit," this conference.

[30] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, L. M. Johnson *et al.*, "Fabrication process and properties of fully-planarized deep-submicron Nb/Al–Josephson junctions for VLSI circuits," *IEEE Trans. Appl. Supercond*., vol. 25, Jun. 2015, Art. No. 1101312.

[31] D. Y. Zinoviev and Y. A. Polyakov, "Octopux: an advanced automated setup for testing superconductor circuits," *IEEE Trans. Appl. Supercond*., vol. 7, no. 2, pp. 3240-3243, Jun. 1997.

[32] C. Shawawreh, D. Amparo, J. Ren, M. Miller, *et al.*, "Optimization of dc Bias Margins in ERSFQ Circuits," *IEEE Trans. Appl. Supercond.*, submitted for publication.

[33] T. V. Filippov, A. Sahu, A. F. Kirichenko, I. V. Vernik, M. Dorojevets, C. L. Ayala, and O. A. Mukhanov, "20 GHz operation of an asynchronous wave-pipelined RSFQ arithmetic-logic unit," *Physics Procedia*, vol. 36, pp. 59–65, 2012.

[34] A. F. Kirichenko, I. V. Vernik, J. A. Vivalda, R. T. Hunt and D. T. Yohannes, "ERSFQ 8-Bit parallel adders as a process benchmark," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun 2015, Art. No. 1300505.