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Demonstration of Signal Transmission between Adiabatic Quantum-Flux-Parametrons and Rapid Single-Flux-Quantum Circuits Using Superconductive Microstrip Lines

F. China, N. Tsuji, T. Narama, N. Takeuchi, T. Ortlepp, Y. Yamanashi, *Member, IEEE*, and N. Yoshikawa, *Member, IEEE*

***Abstract*—We have been investigating interface circuits between rapid single-flux-quantum (RSFQ) circuits and adiabatic quantum-flux-parametron (AQFP) circuits for use in high-speed, low-power hybrid computing system. These interface circuits also enable us to use long-distance interconnections between AQFP gates. In this study, we fabricated and demonstrated AQFP circuits, including long interconnections of passive transmission lines (PTLs), in which the interface circuits were used to convert the signal currents of the AQFP gates into single-flux-quantum (SFQ) pulses traveling along PTLs. The length of each PTL was approximately 4.3 mm. During low-speed measurements, correct operations with wide bias margins were confirmed.**

***Index Terms*—RSFQ, AQFP, passive transmission line, interface, superconducting integrated circuit**

I. Introduction

Studies on energy-efficient integrated circuits are being extensively pursued for next-generation computing systems such as an exascale supercomputers. Superconductive circuits are attracting attention as a beyond complementary metal-oxide-semiconductor (CMOS) technology. Rapid single-flux-quantum (RSFQ) logic [1] can operate at an extremely high operation of up to several hundred GHz with a power consumption that is approximately three orders of magnitude lower than that of CMOS technology. Recently, in order to realize even higher energy efficiency, new low-power RSFQ-based circuits have been investigated [2-6]. In addition, the adiabatic quantum-flux-parametron (AQFP) [7] has been proposed as an adiabatic superconductor logic and is being studied. In AQFP logic, quantum-flux-parametron (QFP) gates [8-10] are optimized to obtain a fully adiabatic operation mode. The power consumption of AQFP logic is estimated to be three orders of magnitude lower than that of RSFQ logic [11]. In general, AQFP gates can operate with small input currents, which enables fairly long direct interconnections between them. However, the maximum length of the interconnections is limited to approximately 1 mm due to circuit parameter deviations [12], [13].

In a previous study [14], we investigated interface circuits between RSFQ circuits and AQFP gates with the aim of constructing an RSFQ/AQFP hybrid computer system. Moreover, these interface circuits enable us to use long-distance interconnections based on passive transmission lines (PTLs) [15], [16] between AQFP gates. Fig. 1 shows the basic concept of long-distance interconnections between AQFP gates using such interface circuits. The AQFP/RSFQ interface converts signal currents in the AQFP gates into single-flux-quantum (SFQ) pulses traveling along a PTL. The RSFQ/AQFP interface receives the SFQ pulses and converts them into signal currents in the AQFP gates. In this study, we designed and demonstrated AQFP circuits including PTL long interconnections made using the interface circuits. We simulated the interface circuits using the Josephson circuit simulator, JSIM [17]. The circuits were fabricated using the AIST Nb 2.5 kA/cm^2 standard process (STP2) [18].

II. Interface Circuits

A. RSFQ/AQFP interface

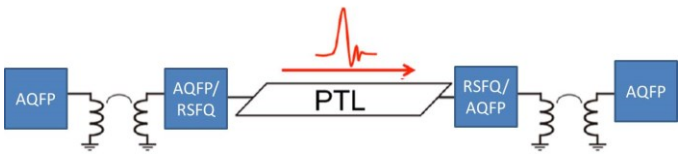

Fig. 1. Diagram of long-distance interconnection between AQFP gates using AQFP/RSFQ and RSFQ/AQFP interface circuits.

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F. China, N. Tsuji, T. Narama, Y. Yamanashi and N. Yoshikawa are with the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama 240-8501, Japan (e-mail: china-fumihiro-pf@ynu.jp).

N. Takeuchi is with the Institute of Advanced Sciences, Yokohama National University, Yokohama 240-8501, Japan (e-mail: takeuchi-naoki-kx@ynu.jp).

T. Ortlepp is with the CiS Research Institute for Microsensor Systems, D-99099 Erfurt, Germany (e-mail: tortlepp@cismst.de).

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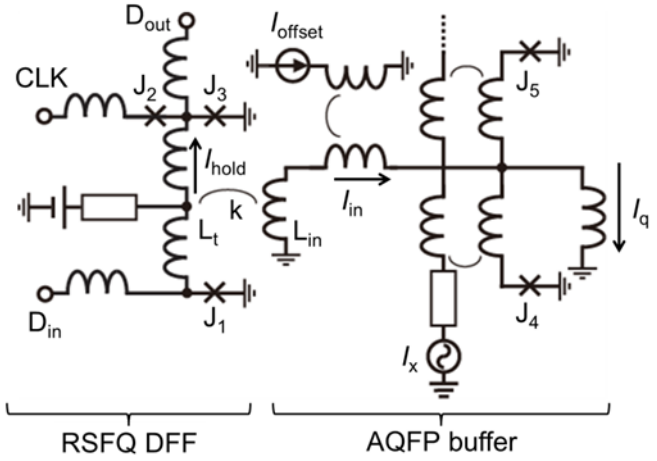

Fig. 2. Circuit schematic of the RSFQ/AQFP interface. J_1 = 234 μA, J_2 = 163 μA, J_3 = 169 μA, $J_4 = J_5$ = 50 μA, L_t = 6.59 pH, L_{in} = 8.5 pH, k = 0.212

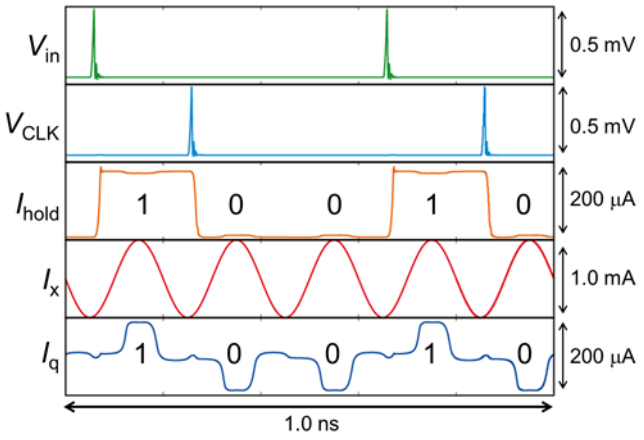

Fig. 3. Simulation results for RSFQ/AQFP interface at 5 GHz.

Fig. 2 shows the circuit schematic of the RSFQ/AQFP interface circuit, which transmits signals from the RSFQ circuits to the AQFP gates. The RSFQ/AQFP interface consists of an RSFQ delay flip-flop (DFF) and an AQFP buffer. The inductor in the storage loop of the DFF, L_t, is magnetically coupled to the input inductor of the AQFP buffer, L_{in}. As the input current to the AQFP buffer, I_{in}, should be always bidirectional so as to determine the logic state, a dc offset current, I_{offset}, is coupled to the input branch. In the initial state, there is no SFQ in the storage loop of the DFF, and I_{in} is negative due to the magnetic flux generated by I_{offset}. As a result, the logic state of the AQFP buffer is determined to be '0' when the excitation current, I_x, is activated. On the other hand, if an SFQ is stored in the storage loop of the DFF, I_{in} is positive due to the magnetic flux generated by the current through L_t, I_{hold}, and the logic state of the AQFP buffer is determined to be '1' when I_x rises. Thus, the AQFP buffer in the RSFQ/AQFP interface reads out the internal state of the DFF in a nondestructive manner. When an SFQ pulse is applied to the clock port, CLK, the flux state of the storage loop is reset. Fig. 3 shows the simulation results for the RSFQ/AQFP interface

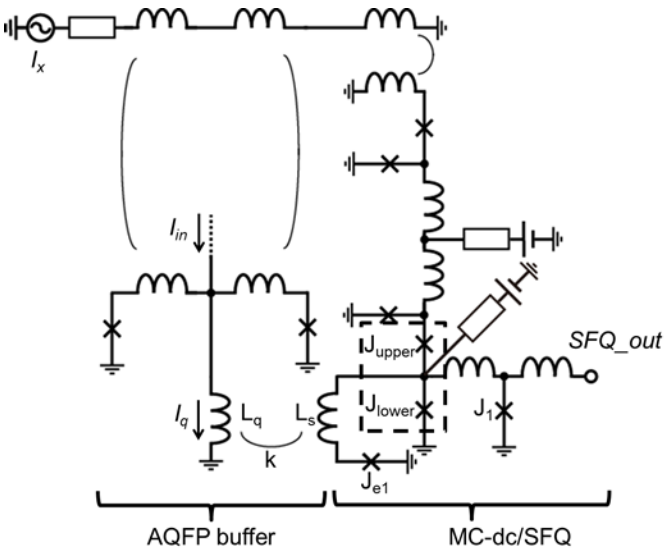

Fig. 4. Circuit schematic of AQFP/RSFQ interface. The part surrounded by the dashed line is a Josephson comparator. J_{upper} = J_{lower} =100 μA, J_e = 50 μA, J_l = 140 μA L_q = 13.1 pH, L_S = 22.6 pH, k = -0.573.

assuming the use of STP2, where V_{in} is the voltage at D_{in}, V_{CLK} is the voltage at CLK, and I_q is the output current of the AQFP buffer gate. When an SFQ pulse arrives at D_{in}, the DFF stores the SFQ and I_{hold} increases. The stored SFQ is expelled from D_{out} and I_{hold} decreases, after an SFQ pulse is applied to CLK. The Fig. shows that the internal state of the DFF is successfully transmitted to the AQFP buffer because the sequence of I_q corresponds to that of the internal state. Circuit simulations determined the bias current margin of the RSFQ DFF to be 0.682 mA ±49.5%, the excitation current margin of the AQFP buffer to be 1.65 mA ±24.0%, and the margin of I_{offset} to be 205 μA ±71.6%.

B. AQFP/RSFQ interface

Fig. 4 shows a circuit schematic of the AQFP/RSFQ interface circuit, which transmits a signal from the AQFP gates to RSFQ circuits. The AQFP/RSFQ interface consists of an AQFP buffer gate and a magnetically coupled dc/SFQ converter (MC-dc/SFQ) [19], [20]. The operation principle was reported in our previous study [14]. In this present study, we slightly modified the circuit parameters of the AQFP/RSFQ interface for wider operation margins. Through circuit simulations, the bias current margin of MC-dc/SFQ and the excitation current margin of the AQFP buffer were found to be 0.644 mA ±21.9% and 1.95 mA ±36.1%, respectively.

III. Long-Distance Interconnection between AQFP Gates

Fig. 5(a) shows a micrograph of the test circuit including long PTLs, in which the AQFP/RSFQ interface generates SFQ pulses traveling along the PTLs according to the input data applied to the input AQFP part, and the RSFQ/AQFP interface receives the SFQ pulses and determines the logic state of the

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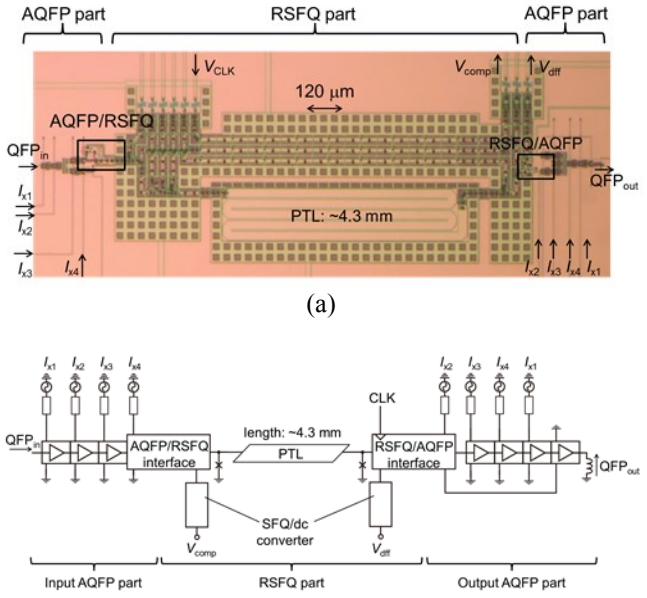

Fig. 5. (a) Micrograph and (b) equivalent block diagram of test circuit including long PTL between AQFP/RSFQ and RSFQ/AQFP interfaces.

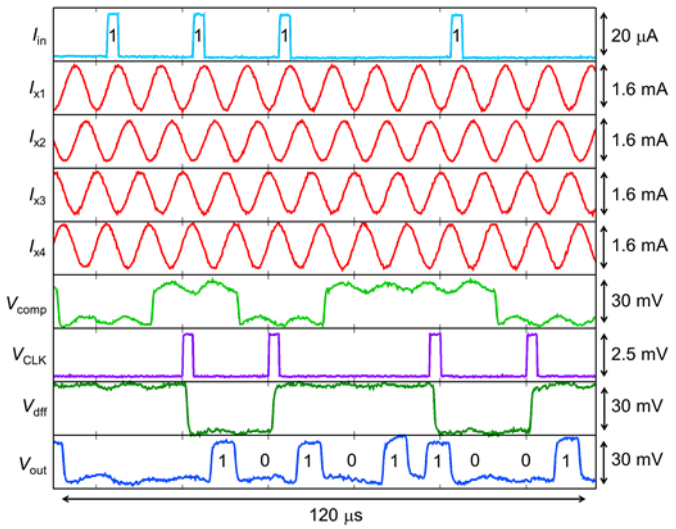

Fig. 6. Measurement results for test circuit at 100 kHz.

output AQFP part. Fig. 5(b) shows the equivalent block diagram. The length of the PTL is approximately 4.3 mm, which is longer than the maximum length of direct interconnections between AQFP gates [13]. The AQFP parts are driven by four-phase excitation current, I_{x1} through I_{x4}. The input and output AQFP parts include three AQFP buffer gates each. The AQFP/RSFQ interface is activated by I_{x4}, and the RSFQ/AQFP interface is activated by I_{x2}. Therefore, output voltages appear at the output port, QFP_{out}, two excitation cycles and one phase after the input currents are applied to the input port, QFP_{in}. We inserted a number of SFQ/dc converters to monitor the internal states of the test circuit. V_{comp} monitors the output port of the AQFP/RSFQ interface (SFQ_out in Fig. 4). V_{dff} monitors the output port of the DFF of the RSFQ/AQFP interface (D_{out} in Fig. 2).

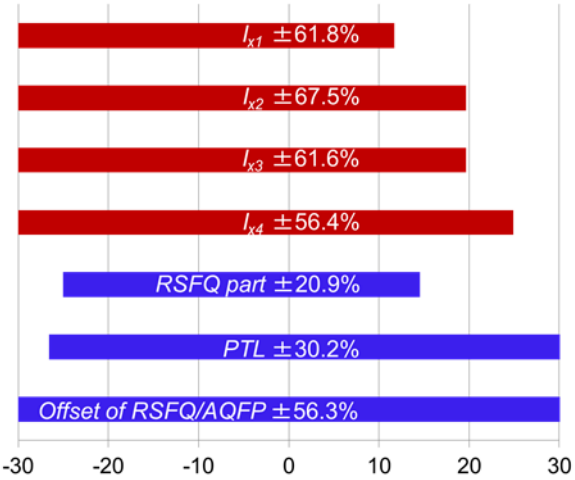

Fig. 7. Measured bias margins of test circuit. The margins are normalized by simulated bias margins.

Fig. 6 shows the measurement results for the test circuit at 100 kHz. I_{in} is the input current applied to QFP_{in}, V_{clk} is the input voltage used to generate clock signals for the DFF in the RSFQ/AQFP interface, and V_{out} is the output voltage at QFPout, which was detected by using dc superconducting quantum interference devices (SQUIDs). V_{comp} is toggled only when logic 1, or a positive I_{in}, is applied to QFP_{in}, which indicates that the AQFP/RSFQ interface correctly generates SFQ pulses according to I_{in}. V_{dff} is toggled when a clock signal is applied to the AQFP/RSFQ interface after V_{comp} is toggled, which indicates that the clock signal correctly resets the flux state of the storage loop of the DFF in the RSFQ/AQFP interface. The entire measurement sequence in Fig. 6 shows that, once logic 1 is applied to the input AQFP part, the logic state of the output AQFP part is kept at 1 until a clock signal is applied, and the input signal to QFP_{in} successfully travels along the long PTL through the AQFP/RSFQ interface and changes the internal state of the DFF in the RSFQ/AQFP interface, which is observed by the output AQFP parts. Fig. 7 shows the measured bias margins of the excitation currents (I_{x1} through I_{x4}), the offset current of RSFQ/AQFP interface, the RSFQ part and the PTL driver/receiver. The bias margins were normalized by the simulated bias margins. The critical margin was ±20.9% of the RSFQ part.

IV. Conclusion

We investigated interface circuits between RSFQ circuits and AQFP gates—the RSFQ/AQFP and AQFP/RSFQ interfaces—so as to realize a hybrid computing system using RSFQ and AQFP logic. These interface circuits also enable us to make long-distance interconnection between AQFP gates. We fabricated and demonstrated AQFP circuits including PTL long interconnections between AQFP gates using the interface circuits. In the experiment, we confirmed correct operations, in which input data applied to the AQFP gates were converted into SFQ pulses on the PTL by the AQFP/RSFQ interface and were

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stored in by the DFF in the RSFQ/AQFP interface, which is observed by the AQFP buffer gates.

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