Developing a commercial superconducting quantum annealing processor

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Mark W Johnson
D-Wave Systems Inc.

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Overview

- Introduction to quantum annealing
- D-Wave 2000Q & technology
- What can it do?
- What’s next?
D-Wave
The Quantum Computing Company

- Founded 1999
- H. Q. in Burnaby, BC
- 150 U.S. Patents
  "Portfolio ranked 4th in 2016 in Computer Systems Industry by IEEE Spectrum"
- 160 employees (45 w/ PhDs)
- Fourth generation of commercially available quantum annealing systems

Customers Include:

- Lockheed Martin
- USC University of Southern California
- NASA
- Google
- Los Alamos National Laboratory
- TDS Temporal Defense Systems
- Oak Ridge National Laboratory

$50 Million in Quantum Systems deployed to customer facilities
The goal of quantum annealing (QA): model the Hamiltonian

\[ H_S(s) = -\frac{1}{2} A(s) \sum_i \sigma_{x,i} + B(s) \left[ -\sum_i h_i \sigma_{z,i} + \sum_{i<j} J_{ij} \sigma_{z,i}\sigma_{z,j} \right] \]

D-Wave 2000Q quantum annealing processor
Quantum processing unit = QPU

128,472 Josephson junctions
18,305 composite flux DACs
10,960 QFP shift register stages
Extreme environmental control affects many aspects of system design

Superconducting IC (QPU) held at $\leq 15$ mK
- pulse tube dilution refrigerators (PTDR) commercially available
- modify PTDRs: make more suitable to our requirements and customer setting
- have achieved run times over 2 years
- QPU, wiring, filter designs constrained with power budget

Magnetic field on QPU $|B| < 1$ nT during cool-down
- passive shielding
- active field compensation
QC is analog computing: controlling parameters in a Hamiltonian

- manufacturing variation in device parameters leads to unacceptably large error in problem specification

- integrated control circuitry enables device homogenization

- requires measuring device parameters first (scalable calibration)

- time scale for calibration consistent across many generations and independent of device count
Classical integrated superconducting control circuitry

A 2048 Q processor requires \( \sim18,000 \) bias signals to operate,

- only \( \sim150 \) bias lines passed to the chip via wirebonds
- local static (programmable) flux biases applied by on-chip flux-DACs

Use on-chip DACs to:

- program \( \{h_i\}, \{J_{ij}\} \)
- homogenize devices
- coerce Ising behaviour

\[ X/Y/Z \text{ addressing scheme uses } \sim82 \text{ wires to address } \sim36,000 \text{ DAC “loops”} \]
\[ \sim22 \text{ kilobytes of on-chip memory } \sim1 \text{ megabyte/s} \]

See Bunyk et al., arXiv:1401.5504 (2014),

Reading out the processor

Shift register using quantum flux parametron\textsuperscript{1} and 4 NDROs

Superconductor fabrication at a commercial semiconductor foundry

- Nb/Al/AlOx/Nb trilayer process
- Six Nb wiring layers
- PE-CVD SiO₂ dielectric (with CMP)
- 0.25µm lines & spaces
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Can quantum tunneling accelerate computation?

- synthetic problem designed to highlight quantum tunneling
- locally hard, globally easy
- did not include stronger heuristic solvers in comparison

Quantum annealer quickly samples low-energy states
Quantum annealing accelerates machine learning

- Significant recent progress in supervised machine learning
- Unsupervised learning benefits from fast sampling of problem energy spectrum
- Sampling from diverse low-energy configurations enables efficient construction of accurate ML models
- Accurate models can be attained with fewer model updates during learning

Quantum simulation of transverse field cubic Ising lattice (R. Harris)

\[ \mathcal{H}_{3D}(s) = -\frac{\Gamma(s)}{2} \sum_i \sigma_i^x + J(s) \sum_{\langle i,j \rangle} J_{ij} \sigma_i^z \sigma_j^z \]

- 3D transverse Ising models embedded in D-Wave QA processor
- Quantitative agreement with locations of phase transitions:
  vs. disorder (doping p) & transverse field \( \Gamma \)
Summary

- D-Wave 2000Q processor
- Quantum computing as a product
- Next generation significant increase connectivity