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Invited presentation ED6-4-INV was given at ISS 2017, December 13-15, 2017, Tokyo, Japan.

ISS 2017
Tokyo
Dec. 15, 2017

Cryogenic Digital Electronics - Challenges for Practical Use -

Akira Fujimaki and Masamitsu Tanaka
Nagoya University

Acknowledgment
The authors thank many researchers who gave us the slides.

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Outline

- History of superconducting digital electronics at a glance
- Four challenges for practical use
  - Higher-speed processing and lower power consumption
  - Larger-scale integration
  - Large capacity and/or high-speed cryogenic memories
  - Operation under cryocoolers
- Future prospect
- Summary

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History of SDE for Past 30 Years
- Circuit Scheme -

- 1960s

  Latching logic

  Higher energy-efficiency and/or higher speed

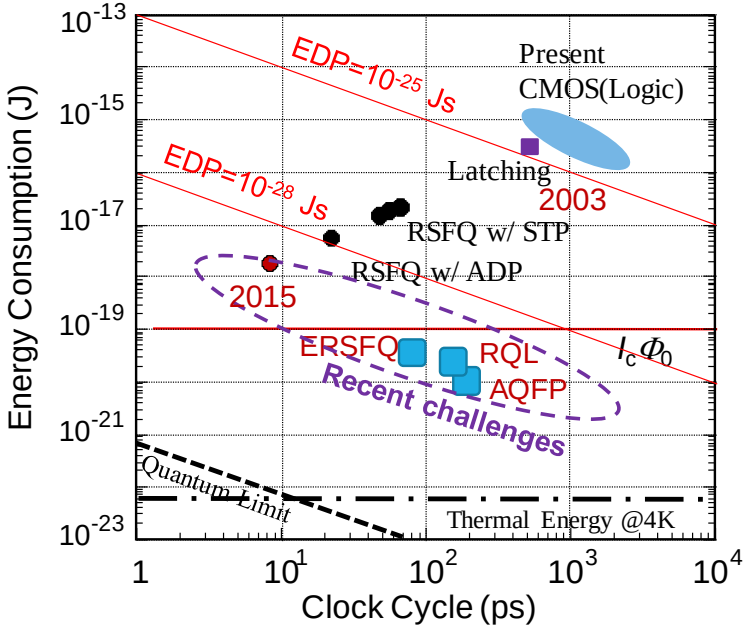
- 1990s

  Rapid Single Flux Quantum Logic

  Higher energy-efficiency and/or higher speed

- 2010s

  Energy-efficient SFQ



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History of SDE for Past 30 Years - Materials and Devices -

Materials

- 1960s
  - Lead alloy
  - **Higher stability**
- 1980s
  - Nb
  - **Elevated T_c, but small I_cR_n product, large spread, and low reproducibility**
  - HTS ($YBa_2Cu_3O_y$ etc.)

Devices

- 1950s
  - Cryotron
  - **Higher energy-efficiency and/or higher speed**
- 1960s
  - Josephson junction
- 2000s
  - Magnetic Josephson junction (π junction)
  - **Function added**
  - nano-cryotron (nTron)
  - **Function added**

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Possible Applications

Application	Advantages	Issues left
Post processing for SC detectors	➢ No penalty for using low temperature ➢ Effective multiplexing for reducing the number of cables	➢ Need larger-scale integration with small power consumption
Digital RF transceivers	➢ Increased flexibility with high-precision broad-band ADCs and DACs	➢ Need broadband cryogenic amplifiers for higher performance
High-end servers/ High-performance computers	➢ High throughput and low power consumption ➢ Cooling penalty hidden	➢ Need demonstration of the system ➢ Need much larger-scale integration with small power consumption
Reconfigurable circuits	➢ Increased flexibility with high throughput or low latency	➢ Need much larger-scale integration with small power consumption

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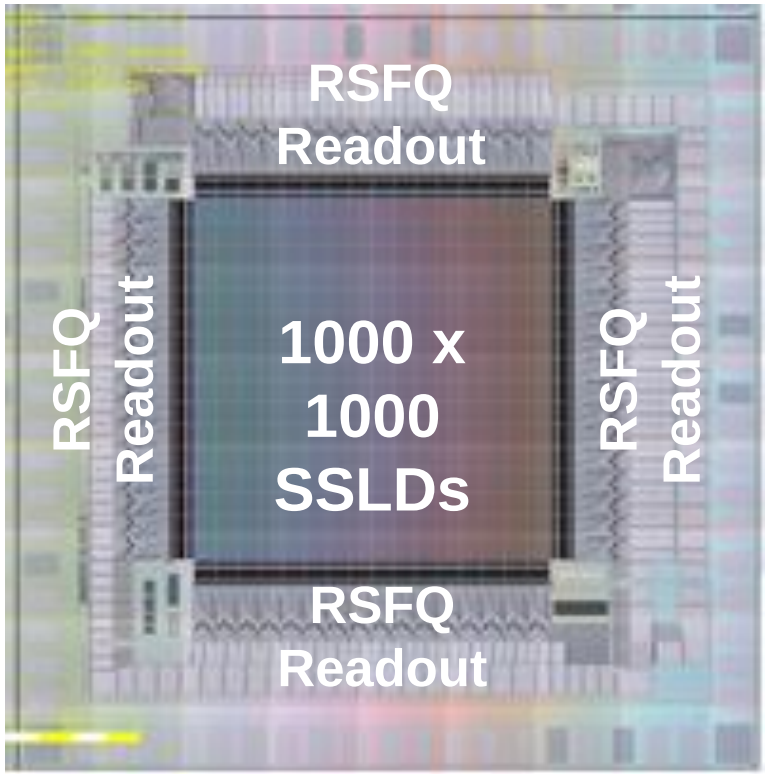
Post Processing of Detectors



1 Mega pixel neutron detector chip

JJ counts : 20000

Made with the special fabrication process based on AIST ADP2.

Collaborative study with Nagoya Univ. AIST and Osaka Pref. Univ.

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Twente, Super ADC

Delta-Sigma modulator was made of the HTS JJs.

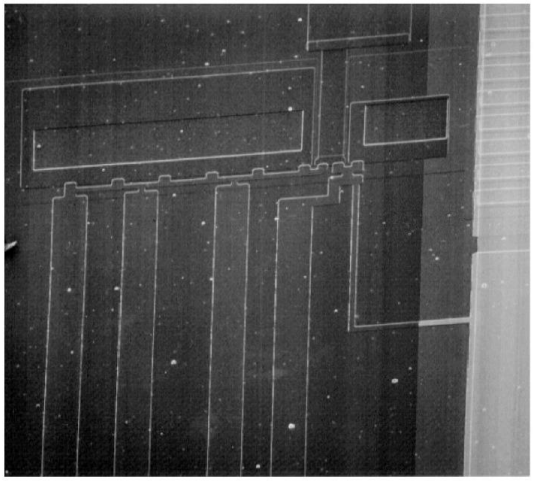

Fig. 11 A first order σ-δ modulator realized in a multilayer high-T technique.

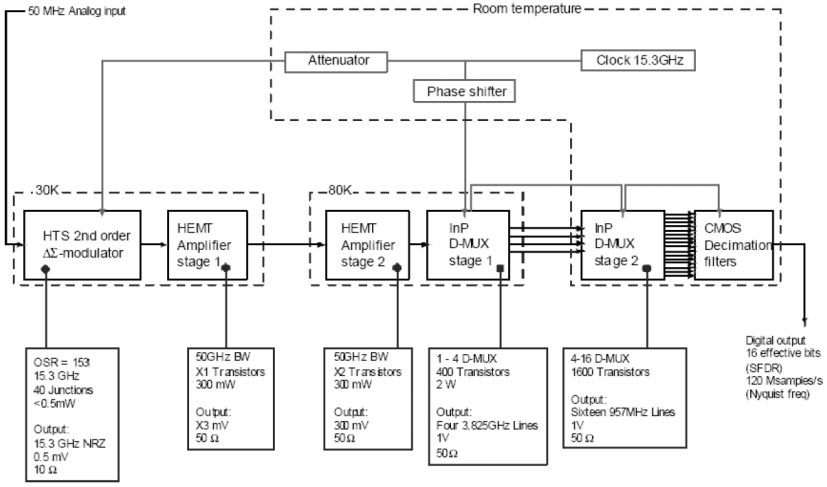

Fig. 12 Block diagram of the 2nd-order σ-δ-ADC of the SUPER-ADC project.

H. Rogalla, IEICE Trans. Electron., E91-C, 272 (2008)

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Why SC servers?

Electric power consumed in 100 searches in the internet

=

Electric power consumed in ironing a shirt

Courtesy of Yoshikawa

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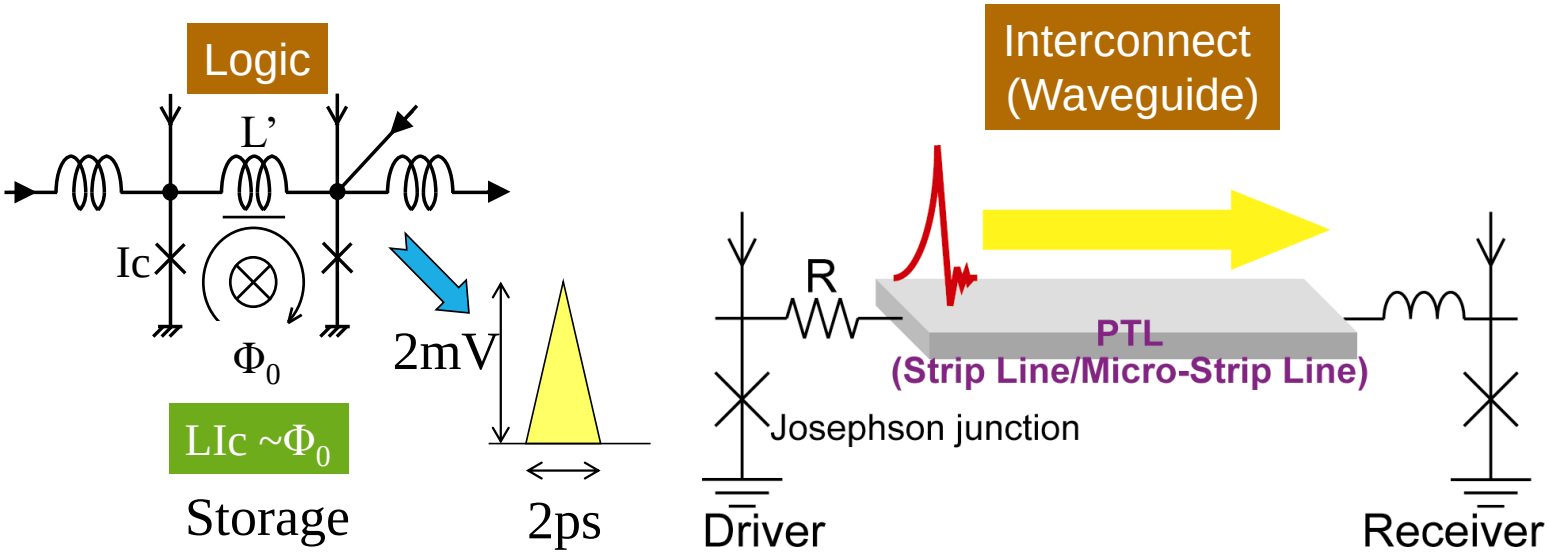
Special Features of SFQ Circuits



- Signal propagation at the speed of light with small distortion in interconnects based on waveguides.
- No recharge process both in logic operation and interconnects.
- Scaling law

➡ High-speed & low power

➡ Suitable to LSIs

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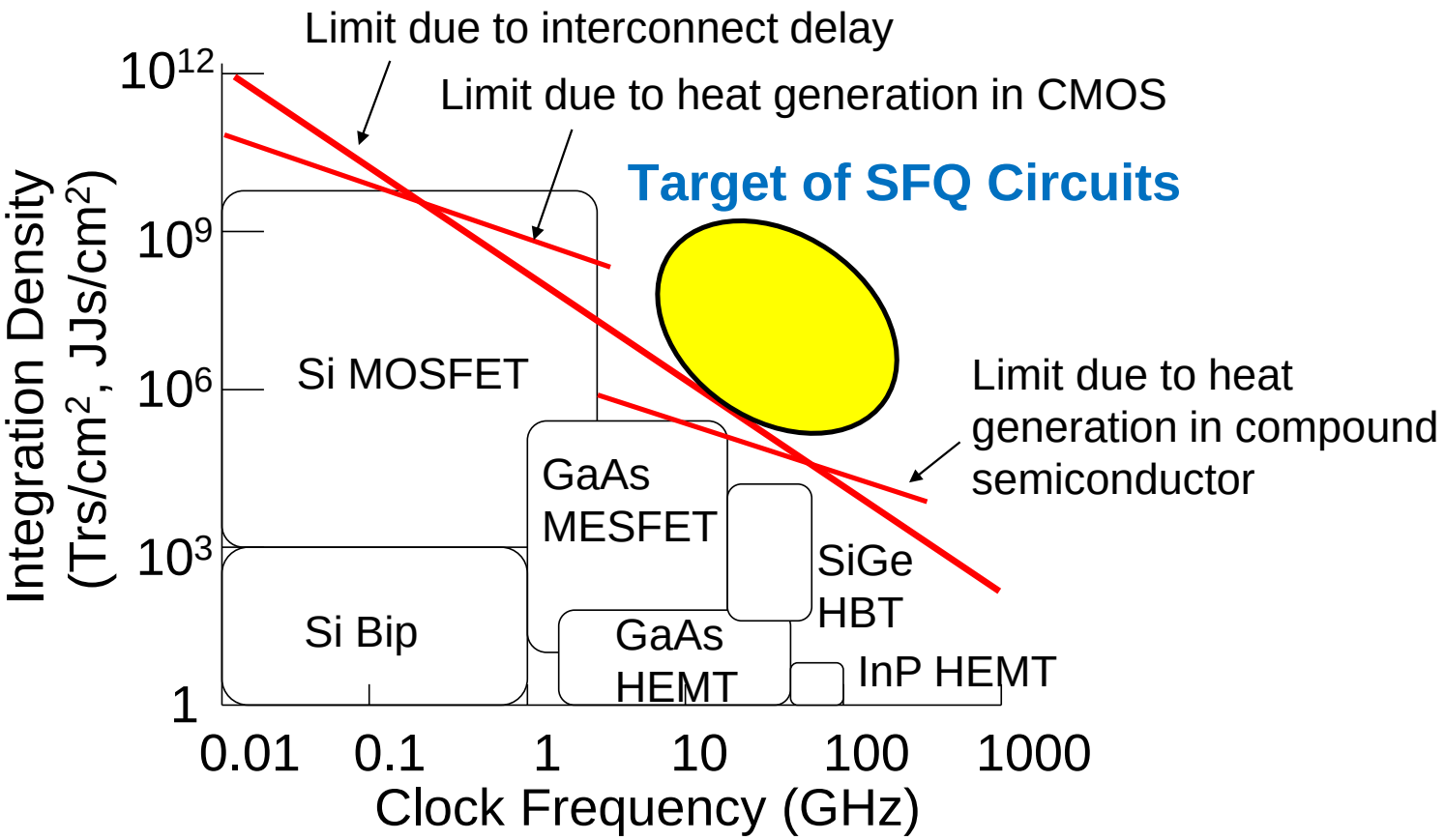
Appealing Feature of SFQ Circuits



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Subjects Done/Doing for High-Speed & Low-Power

- Energy-efficient SFQ circuits
- CAD tools
- Suitable microarchitecture
- Efficient AC-DC converters for dc-powered circuits

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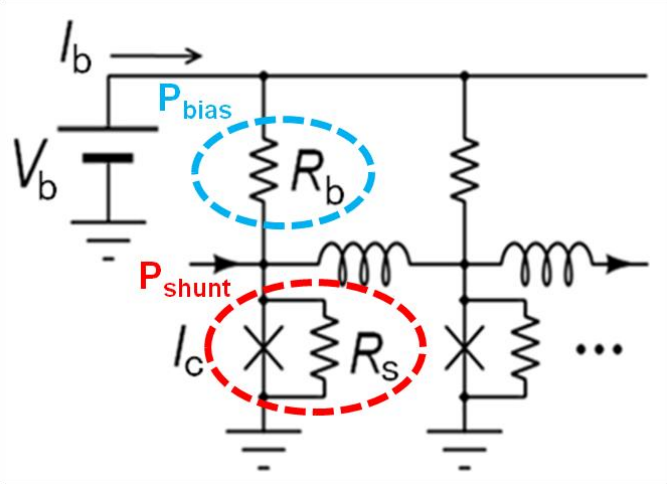
Issue for Energy-Efficiency



R_b is used for providing a constant current to each Josephson junction.

Power consumption at R_b
(Static power consumption)

$$P_{\text{bias}} = \frac{V_b^2}{R_b} \approx 0.7 I_c V_b$$

Example: DFF
$P_{\text{bias}} = 1.8\mu\text{W}$

Power consumption at R_s
(Dynamic power consumption)

$$P_{\text{shunt}} = f I_c \Phi_0$$

f: operating frequency

Example: DFF
$P_{\text{shunt}} = 36n\text{W}$

Typically, $I_c \Phi_0 \approx 2 \times 10^{-19} (J)$

Necessity for eliminating static power consumption.

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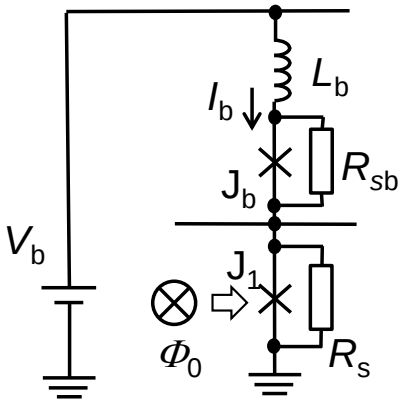
Energy-Efficient SFQ Circuits

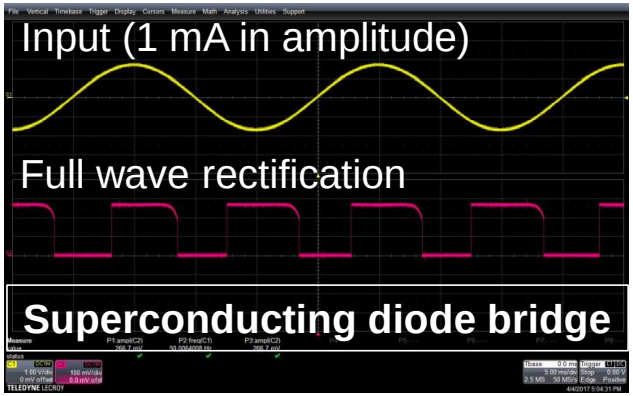
Bias resistors are replaced with inductors and junctions.

DC-powered circuit
Ex: ERSFQ (Hypres)

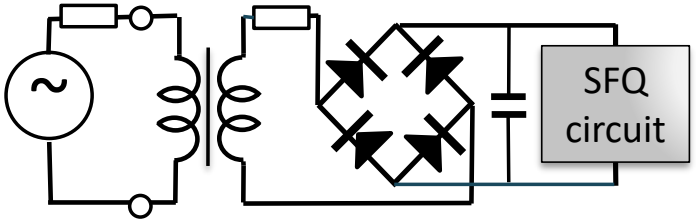


A. Kirichenko, et al., IEEE Trans. Appl. Supercond., **21**, 776(2011).

AC(RF)/DC converter based on superconducting diodes enables energy-efficient power distribution.



100 mV, 2 mA ⟹ 1 mV, 200 mA

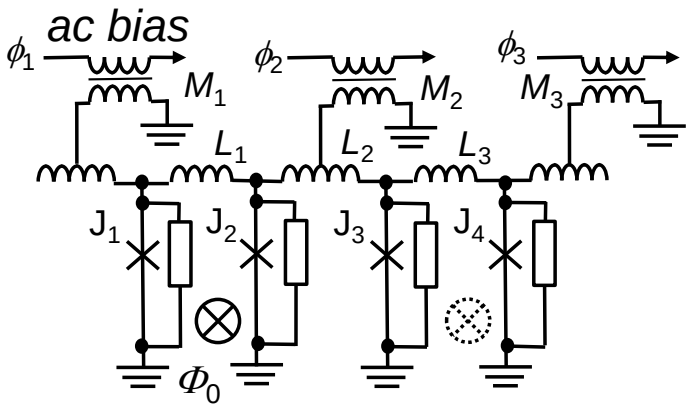


Impedance transform

Energy-Efficient Power Distribution

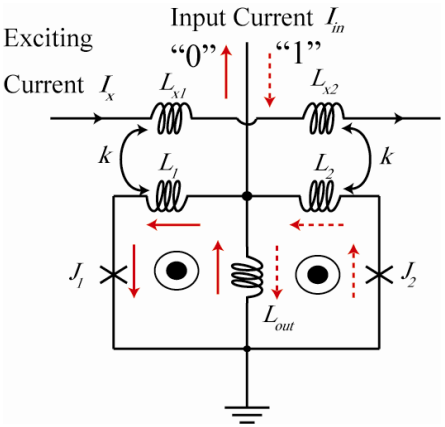
Circuits are driven by ac(rf) bias currents provided through transformers.

AC(RF)-powered Reciprocal Quantum Logic (Northrop Grumman)



Q. P. Herr, et al., J. Appl. Phys., **109**, 103903 (2011).

RF-powered Adiabatic Quantum Flux Parametron (Yokohama National University)



Measured bit energy : 10 zJ

N. Takeuchi, *et. al.*, Appl. Phys. Lett., 102, 052602 (2013).

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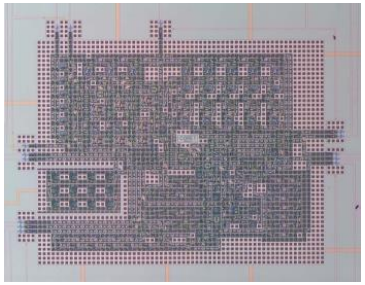
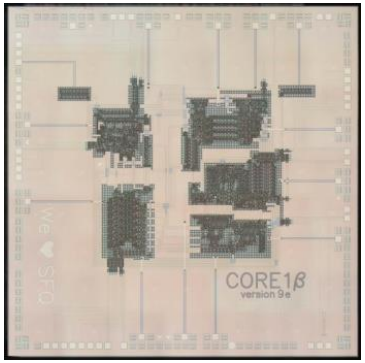
History of SFQ Microprocessors





More Powerful

More Energy-Efficient

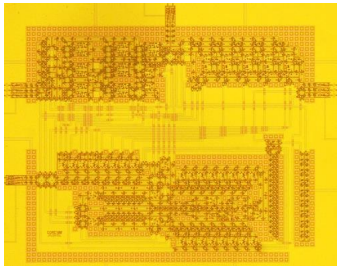
CORE1α (2003)
4999 JJs
15 GHz
167 M Instructions/s
1.6 mW

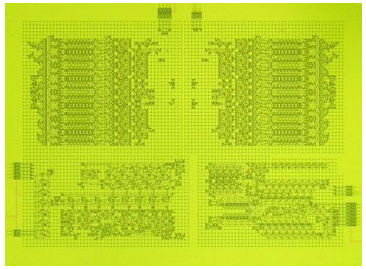
CORE1β (2006)
10955 JJs
25 GHz
1400 Million Operations/s
3.3 mW

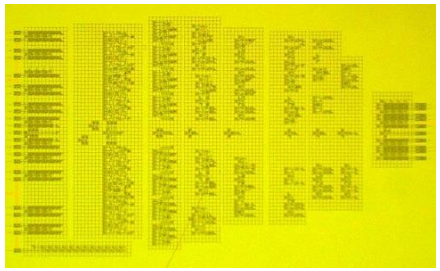
NAGOYA UNIVERSITY YOKOHAMA National University

Recent Topics in SFQ Microprocessor

Bit-serial μP	Bit-serial μP	Bit-Parallel ALU
100 GHz	50 GHz	50 GHz
μP w/o Memory	Memory Embedded	ALU







CORE100 (2015)	**COREe2 (2017)**	**GLP (2017)**
3073 JJs	10655 JJs	4868 JJs
800 MIPS	500 MIPS	50 GIPS
1.0 mW	2.4 mW	1.4 mW
800 GIPS/W	210 GIPS/W	36000 GIPS/W
New Fabrication	Programs Executed	Gate-Level Pipelining

NAGOYA UNIVERSITY CRAVITY AIST NAGOYA UNIVERSITY 京都大学 KYOTO UNIVERSITY NAGOYA UNIVERSITY KYUSHU UNIVERSITY

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Subjects Done/Doing for Larger-Scale Integration

- Smaller junctions with increased Jc
- Increased number of wiring layers
- Vertical stack of junctions or double active layers
- Introduction of kinetic inductances
- Introduction of magnetic Josephson junctions

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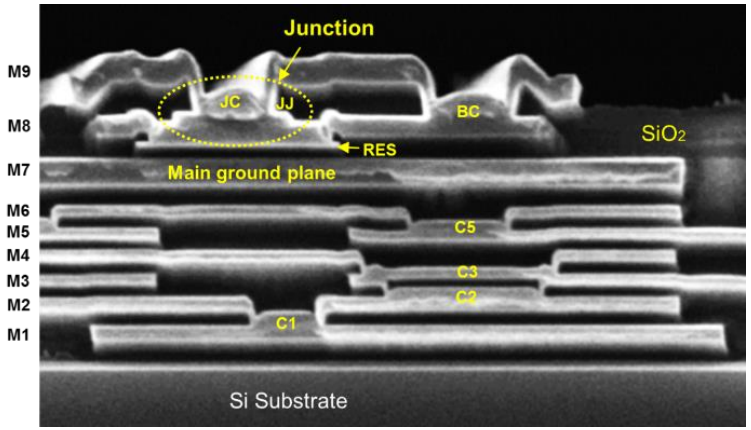
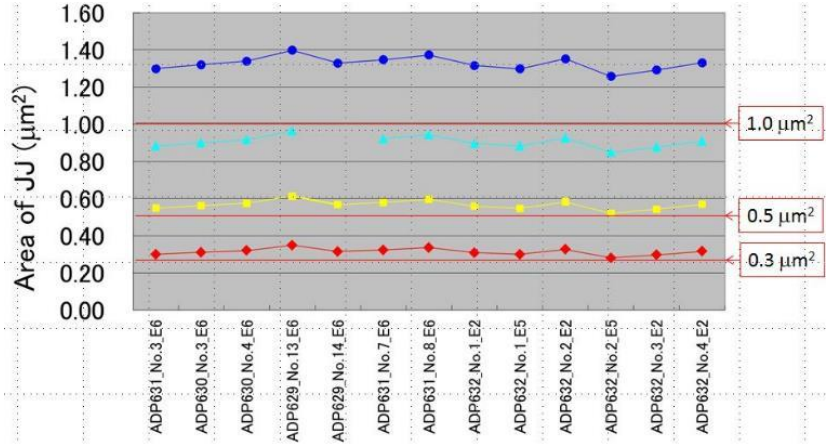
AIST Nb 9-Layer Fabrication Process



Cross section of Nb 9-layer device



Measured I_c reproducibility

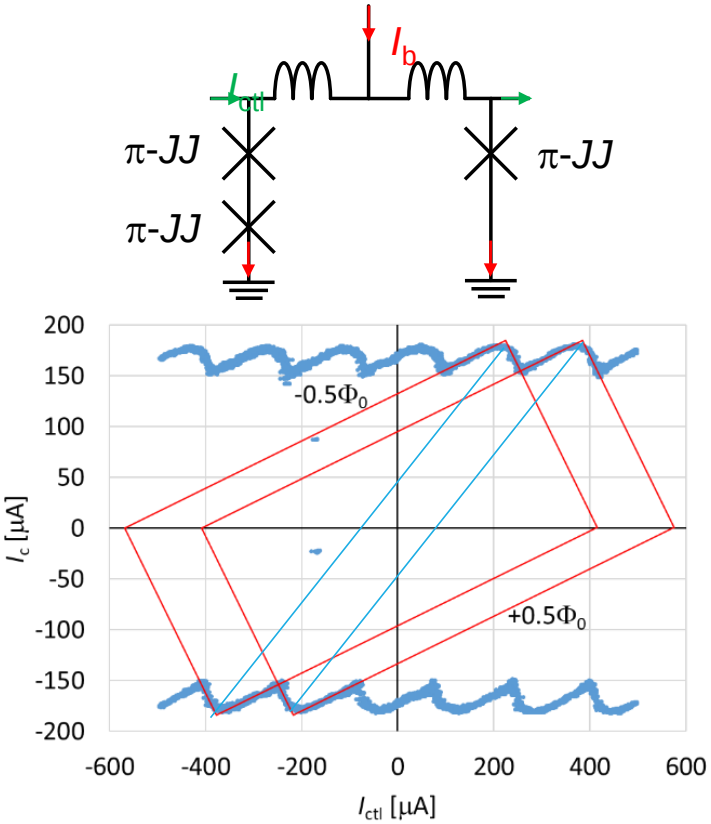
Controllability and uniformity of their I_c have been measured for more than 10 wafers.

Since J_c of the process is 10 kA/cm^2, I_c of the 0.3 μm^2 JJ is 30 μA.

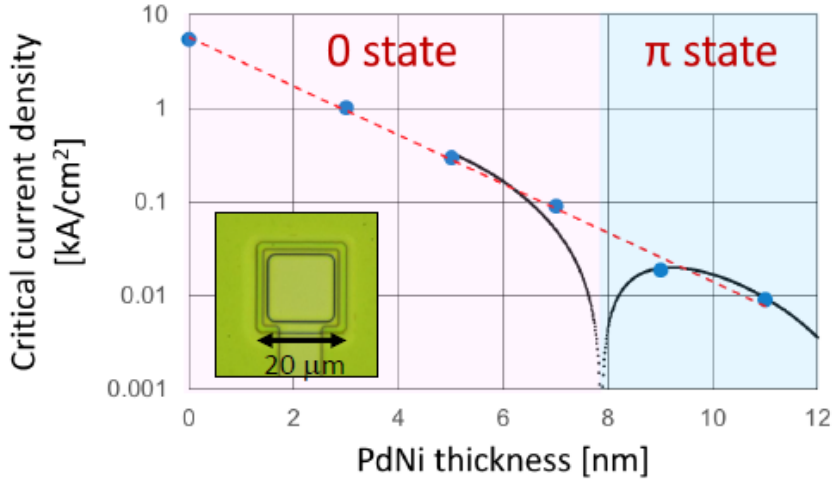
CRAVITY AIST

Courtesy of M. Hidaka & S. Nagasawa (AIST)

Magnetic Josephson junctions



I_c-I_{ctl} characteristics ($Pd_{89}Ni_{11}$ 9nm 20μm-sq.)



I_c spread of π junctions is small enough for integration

H. Ito, et al., Appl. Physics Ex. Vol. 18, 033101 (2017)

Subjects Done/Doing for Large-Capacity and/or High-Speed Memories

- Vortex-transitional memory (Nagasawa Memory)
- JJ-CMOS hybrid memory
- Magnetic-junction-based memories
- nTron-based drivers and sense gates

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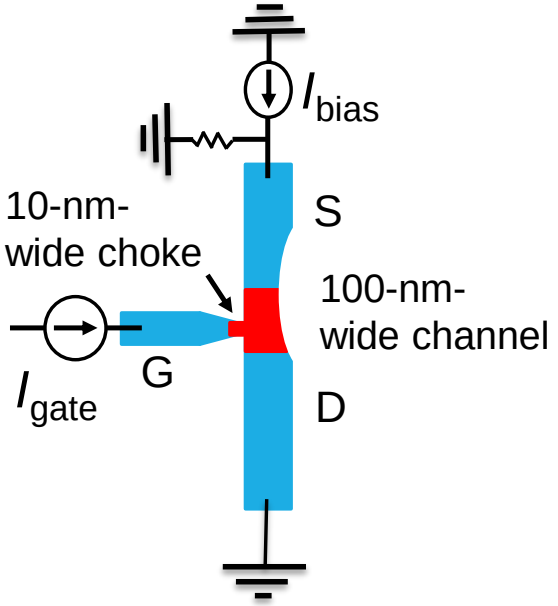
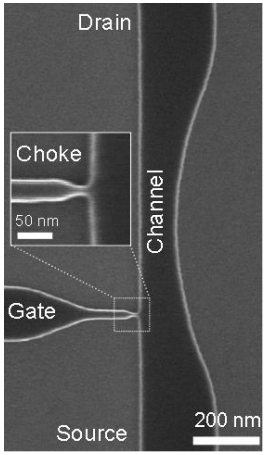
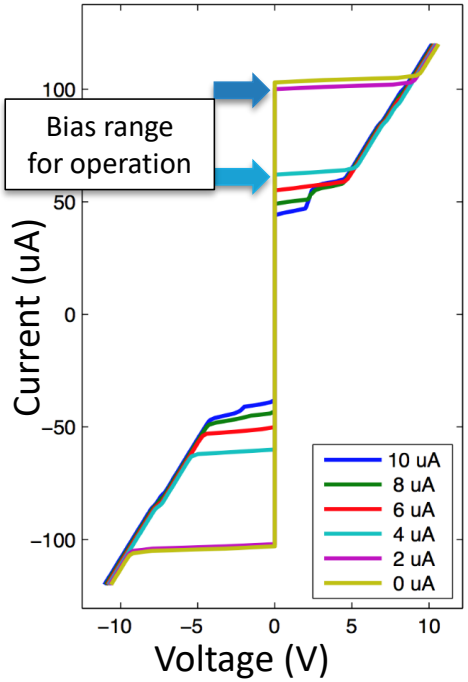
Broadband Amplifier

Nano-cryotrons (nTrons)

- Invented by MIT
- Generate relatively large voltage around 1 V.
- Potentially act as an amplifier with the Gain-Band product of 0.1-1 THz.

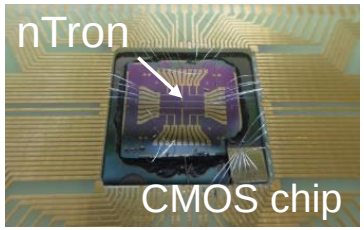


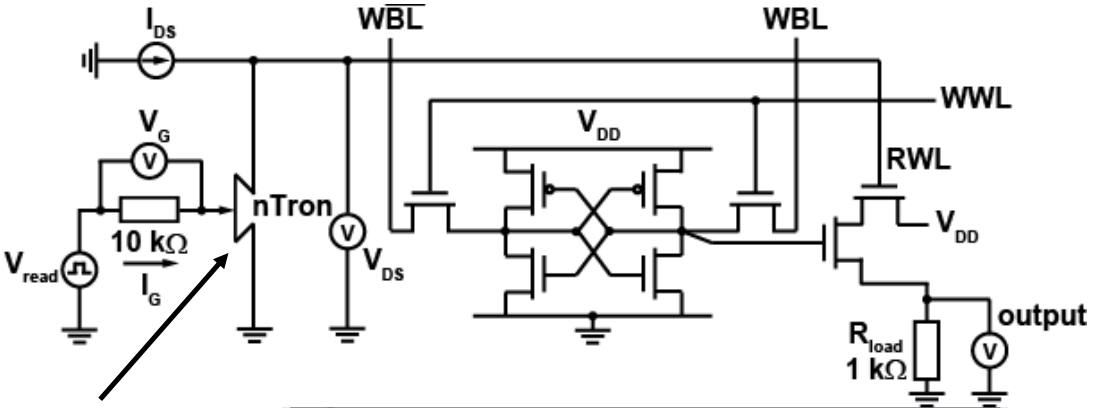


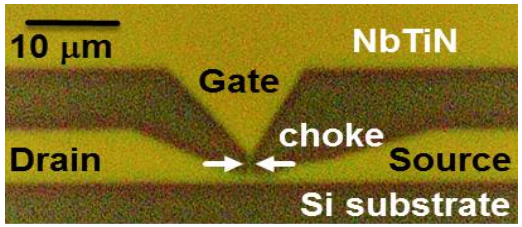


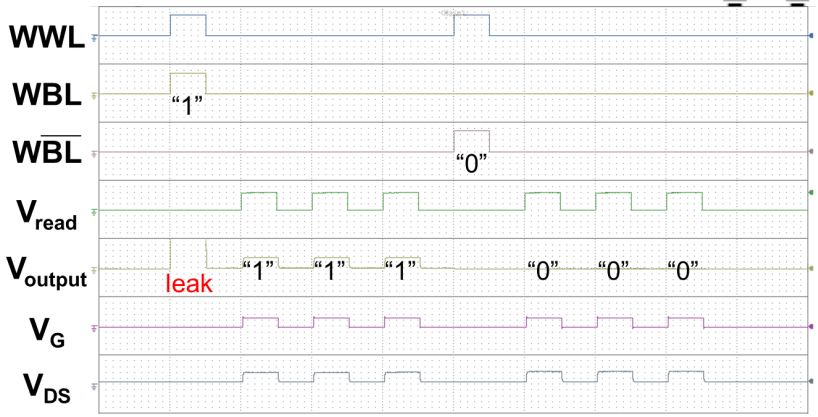
Courtesy of Zhao (MIT)

nTron-based CMOS SRAM Driver









- nTron generates V_{SD} of 0.2 V.
- nTron can drive the FET of RWL.

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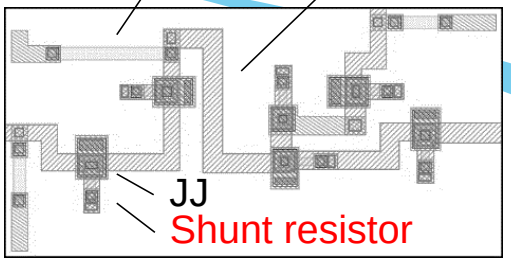
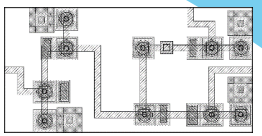
Issues for Larger-Scale Integration



D Flip-Flop: 40 x 80 μm
(Assuming Min. I_c = 50 μA)

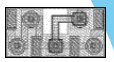
- Shunt-resistor-free JJs
- ERSFQ/eSFQ

(Elimination of resistors)



20 x 40 μm

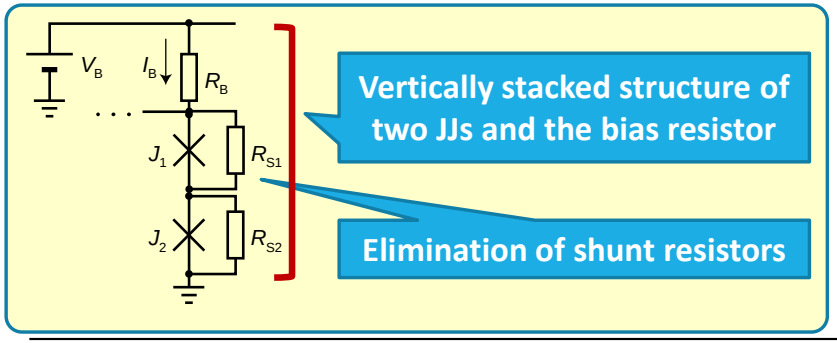
- High Sheet Inductance (NbN, etc.)
- JJ Stack



8 x 16 μm

- Equipment update

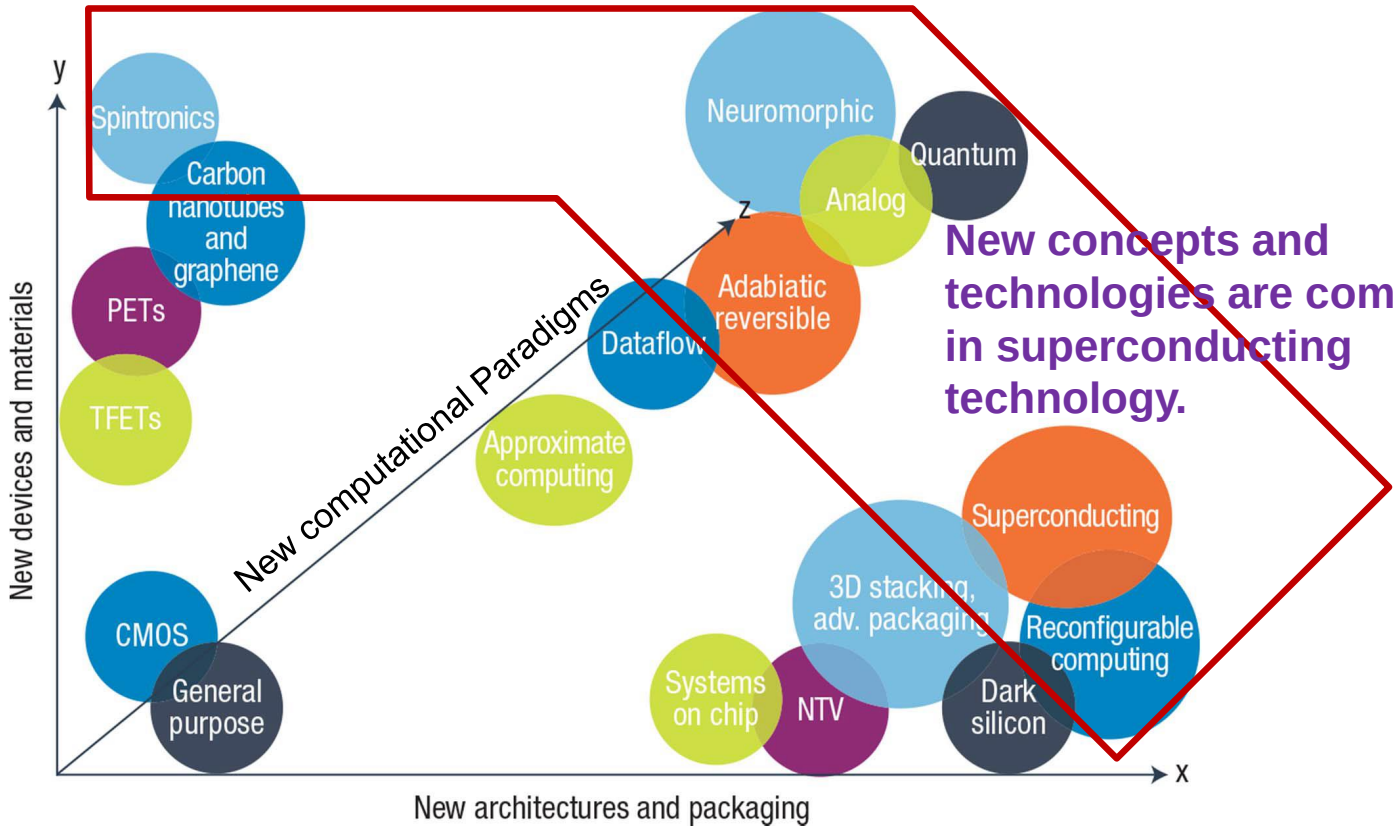
2 x 4 μm



Line and space: 1μm

0.25μm

Future Prospects



New concepts and technologies are combined in superconducting technology.

J. M. Shalf, et al., Computer, 2015

Courtesy of Jie Ren (SIMIT)

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), February 2018.
Invited presentation ED6-4-INV was given at ISS 2017, December 13-15, 2017, Tokyo, Japan.

Summary

- Superconducting digital technology based on the SFQ circuits has greatly advanced in the past 30 years, particularly in the last 10 years.
- I believe SDE technology or SFQ ICs come to the market soon because almost all the issues for practical use have been overcome.