30 Years of History and Future Perspectives of Superconducting Electronics

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and

IEEE Council on Superconductivity
30 years of history don’t seem long seen the age of superconductivity of 106 years.

But: a lot happened in these last 30 years:

- Commercial LCD Flat Screen TVs
- Blue LEDs
- The High-Tc “Revolution”
- The International Superconductivity Technology Center was founded
- New Applied Superconductivity Conferences started:
  - ISS in 1988
  - EUCAS in 1993
- Qubits
- Josephson π-junctions
- Magnetic Josephson junctions
- ...

- 1 November 1987: I became Physics Professor at the University of Twente in The Netherlands.

- Some of you were born in the last 30 years.
30 years of history don’t seem long seen the age of superconductivity of 106 years

But so much happened in these last 30 years in Superconductive Electronics that it would take hours to review the achievements.

Session ED6 (Electronic Devices) - 30 Years of

- SQUIDs R.J. Ilmomiemi
- Detectors J.N. Ullom
- Microwave Devices S. Ohshima
- Digital Circuits A. Fujimaki
- Quantum Information J.-S. Tsai

A subjective (re-) view without any claim of completeness
Prof. Hasuo
EUCAS 2011

Research flow of superconducting digital electronics*

* This chart was drawn with a help of Dr. Bedard, Dr. Mukhanov, Prof. Rogalla, and Prof. Van Duzer.

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Plenary presentation PL6-INV was given at ISS 2017, December 13-15, 2017, Tokyo, Japan.
HTS
First ‘HTS’ (Nb$_3$Ge) Applications

Serial array of Nb$_3$Ge nanobridges

H. Rogalla, M. Mueck et al. (1985)

Integrated Nb3Ge nano-bridge dc-SQUID operated in liquid hydrogen above 20K
Critical Temperature as Function of Time

Critical Temperature [K] (logarithmic scale)


1
10
100
1000

Hg
Pb
Nb
Nbo
NbN
Nb3Sn
Nb-Al-Ge
Nb2Ge
MgB2
BiSrCaCuO
HgBaCaCuO
YBaCuO
La-Ba-Cu-O
The Begin: How to fabricate an HTS–SQUID

Press and sinter powder into the form of a bulk cylinder,
drill a hole and cut partially with a thin saw.

Break the link and press it together again with an adjustable screw or taper.

Voilà – the SQUID is ready !!


Polycrystalline junctions

R. Koch, IBM; Twente (1987)
Bi-crystal Grain Boundary Junctions

\[ J_c (A/cm^2) \]

\begin{align*}
J_c &\quad (A/cm^2) \\
T &\quad 4.2 K
\end{align*}

\begin{align*}
0 &\quad 10 &\quad 20 &\quad 30 &\quad 40 \\
10^3 &\quad 10^4 &\quad 10^5 &\quad 10^6 &\quad 10^7
\end{align*}

\[ \theta \quad \phi \quad \gamma \]


The Begin: Thin Film Josephson Junctions

Template Junctions

Step-edge junctions

L.P. Lee, K. Char, et al. (Conductus Inc.)

Jia et al. Physica C 175, 545 (1991)

Ramp–type Junctions with Ga–doped PBCO barrier

Barrier thickness and Ga-doping of PBCO are design parameters

SuperADC

OSR = 153
15.3 GHz
40 Junctions
<0.5mW
Output:
15.3 GHz NRZ
0.5 mV
10 Ω

50 MHz Analog input

50Mhz BW
X1 Transistors
300 mW
Output:
X1 mV
50 Ω

1 - 4 D-MUX
400 Transistors
2 W
Output:
Four 3.025GHz Lines
1V
50 Ω

4:16 D-MUX
1000 Transistors
Output:
Sixteen 957MHz Lines
1V
50 Ω

CMOS
Decimation filters

Digital output
16 effective bits
(SFDR)
120 Samples/s
(Nyquist freq)

0K

30K

Phased shifter

Attenuator

Clock 15.3GHz

Room temperature
Multi-Layer HTS Integration with Ramp-Type Junctions (ISTEC)

- Deposition of gold for decreasing contact resistance
- Via hole for oxidizing ground plane
- Smooth surface with Ra=1.2 nm
- Standard deviation of Ic: 8.1% for Ic=0.5 mA junctions
- V-Ti resistor with sheet resistance of 20\(\Omega\)

Hasuo, ISTEC, Summerschool on Superconducting Electronics (2005)
HTS 100 JJ circuit (ISTEC)

Circuit including 101 JJs

dc-SFQ Conv.          JTL(16JJx6)          SFQ-dc Conv.

Signal (1mA/div)  Reset (100µA/div)  Output (0.2mV/div)

Operation at 29 K   \(\Sigma\Delta AD\) modulator (13 JJ, Hitachi) 100 GHz @20K

Ref: H.Wakana et al (ISTEC), ISS2004

Ring Oscillator (21 JJ, Toshiba) 57 GHz @20K

R&D of thin films and electronic devices at ISTEC in the first decade (‘88-'97)

- High-quality Nd123 thin films with atomically flat surfaces
- Grain-boundary junctions and device physics
- Hg-1212 GB JJ and SQUID which can be operated at > 110 K


Dr. K. Tanabe
HTS multilayer technology developed at ISTEC for SFQ circuits (2000’s)

3 RE-123 layers with SrSnO₃ (SSO) insulator
$R_a$ of sputtered multilayer < 2 nm
Ramp-edge JJs with $1\sigma I_c$ spread 5-10 %
Minimum junction width of 1.5 $\mu$m

HTS Sampler circuit with a potential bandwidth over 100 GHz
(15 JJs integrated)

Dr. K. Tanabe
Superconducting sampling oscilloscope

Sampling Oscilloscope Prototype

Chip and Package

Ref: M. Hidaka (NEC) et al., ASC 2000

Waveform of 20GHz
HTS SQUIDs with multilayer structure and ramp-edge JJs (2007～)

Features
* Integrated circuit structure with several oxide layers
* High-angle GB is eliminated from JJs and coils

Advantages
* Stable operation at 77 K
* Easy to fabricate multi-channel array sensor
* Robust against application of magnetic field
* High field sensitivity approaching LTS SQUIDs

Dr. K. Tanabe
Development of HTS-SQUID systems at ISTEC and SUSTERA

FY2010

- JST S-innovation (magnetic immunoassay)
- JOGMEC SQUITEM (for metal)
- JOGMEC EM logging (for oil)

FY2015

- JST SIP (NDE for infrastructure)
- JOGMEC improved SQUITEM

SUSTERA is the mutual aid organization (nonprofit organization) in which members conduct collaborative research on the sensing technology based on HTS-SQUIDs.

Members:
+ Fujitsu Ltd.
+ The Chugoku Electric Power Co., Inc.
+ Mitsui Mining & Smelting Co., Ltd.
  (MINDECO until March 2017)
+ (ISTEC until June, 2016)

Products: HTS-SQUID chip (module), compact cryostat, etc.

Dr. K. Tanabe
SQUITEM-III system
for exploration of metal resources

15 kg
10.6 kg
2.5 kg
60 cm

# Compact design
# Vacuum maintenance free
# Keep LN$_2$ for 17 h
# > x 10 higher slew rate
   (> x 20 higher S/N)

Commissioned by JOGMEC

Actual exploration in Peru

Development of improved SQUITEM-III
(FY2015-FY2016)

x, y, z 3-component SQUID sensors
tested in Australia field

Development of long-range EM logging system
- Application to oil field -

Target: monitoring of CO₂ frontend in EOR
- Insufficient sensitivity of conventional induction coil sensor → short distance
- Owing to high sensitivity of SQUID even at low frequencies
  EM in steel-cased wells with the distance > 1000 m expected

Technical challenges:
- Analysis technique to compensate influence of steel casing
- High-power transmitter & injection coil
- HTS-SQUID receiver (magnetometer) usable in high pressure (30-70 MPa) and high temperature (200 °C) environment
- Remote control of SQUID magnetometer

Image of crosshole EM (logging) system with HTS-SQUID magnetometer (Resistivity tomography between two wells)

Development of elementary technologies started in 2012
FY2012  JOGMEC “Innovative technology in oil and gas development field” program
FY2013-2015  JOGMEC “Technical solution project”

Dr. K. Tanabe
SQUID receiver system for use in a test well

Field test at JOGMEC Kashiwazaki TF

/ Stable operation at 300 m depth in a steel-cased well
/ Detection of magnetic signal from 800 m distant emitter
/ Control of SQUIDs through 3 km long optical fiber

Pressure tightness > 70 MPa confirmed
MCG (Hitachi)

HTS 16ch MCG

Harold Weinstock, 2005
A central device in Superconductive Electronics:

SQUID

You can read everything about it in:

Photograph of typical DC SQUID sensor based on the Ketchen-Joycox (IBM) design.
Planar dc-SQUID

Integrated planar SQUID gradiometer with baseline length of 50 mm.

Spectral densities of the magnetic flux noise at $T = 4.2$ K:
(a) planar SQUID gradiometer
(b) SQUID magnetometer
Magnetic field noise: 3.0 fT/$\sqrt{\text{Hz}}$
Gradient spectral noise: 0.6 fT/(cm· $\sqrt{\text{Hz}}$).
Magnetoencephalography with multichannel SQUID systems

Neuromag System

Response to right thumb stimulation (Romani)
Department Quantum Detection: FTMG system
Heliborne system set-up

- Tow body
- SQUID
- Cryostat
- Flux-locked loop
- Controller
- Laptop for system control and data storage
- Data transmission via optical fiber
- Power supply, data acquisition, DGPS, INS, pressure controller

Δ2 m
Sensors

- Transition Edge Detector (TES)
- Superconducting Single Photon Detector (SSPD)

M. Kaniber, F. Flassig, G. Reithmaier, R. Gross, and J. J. Finley, TU München
Programmable Josephson Voltage Standard (DAC)

Individual bits are switched via the dc current bias.

\[ V_{Array} = nN \frac{h}{2e} f \]

(First shown by Hamilton, Burroughs and Kautz in 1995)
Fabrication & Design of Superconducting Circuits

- Boulder Micro Fabrication Facility
- Superconducting integrated circuits
  - Uniform junctions, barrier materials
  - Power dissipation
- Microwave circuit design
  - Lumped element inductors & capacitors, power splitters, coplanar waveguides
  - Simulation & modelling

(12 x 17) mm² 10 V PJVS Chip

Microwave Input

Arrays with 265,116 JJs

DC Input/Output Pads
Japanese LTS device national projects and ISTEC

ISTEC
1988

METI
Scientific computing system
81’ – 91’

Basic technology of LTS devices
• Latching circuits
• Nb 3-layer process (NEC)

ISTEC Tsukuba
1992

LTS device

HTS device

NEDO
JJ hybrid system
95’ -97’

Compilation of latching circuits
• 100 Mbps I/O

ISTEC
1997

LTS device

1992 1997

ISTEC Tsukuba

NEC
100 Mbps I/O

Ring network demo. with 2 GHz operation (NEC)

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100 Mbps I/O

Ring network demo. with 2 GHz operation (NEC)

NEDO
JJ hybrid system
95’ -97’

Compilation of latching circuits
• 100 Mbps I/O

ISTEC
1997

LTS device

2 × 2 switch (NEC)

MEXT
Information processing by SFQ
97’ -01’

Basic technology of SFQ circuits
• Design technology
• Start of cell base design
• Start of SFQ fabrication

MEXT
Information processing by SFQ
97’ -01’

Basic technology of SFQ circuits
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• Start of cell base design
• Start of SFQ fabrication

ISTEC
2001

8 bit microprocessor
770MHz operation (Fujitsu)
Japanese LTS device national projects and ISTEC

SFQ development and packaging technology
- Planarized Nb 6-layer device
- SFQ cell library
- SFQ automatic design system
- Wide band packaging technology with cryo-cooler (10Gb/s)

Result example
- SFQ processor with 21 GHz operation (ISTEC, Nagoya U., YNU)
- Video transfer demonstration by SFQ 4×4 switch (ISTEC)

Development toward SFQ small system
- Development of SFQ A/D converter
- Packaging technology for SFQ circuits

Result example
- 50GS/s SFQ A/D converter (ISTEC)
- 40 Gb/s optical input to SFQ circuits (ISTEC)
Japanese LTS device national projects and ISTEC

2006 – 2011

JST/CREST
RDP processor
06’ – 11’

SFQ circuits by Nb 9-layer process and SFQ speed-up
- Construction of Nb 9-layer process
- SFQ cell library for the Nb 9-layer process
- High-speed SFQ processor using the Nb 9-layer process

Cross-section of Nb 9-layer device (ISTEC)

50GHz SFQ processor
(ISTEC, Nagoya U., YNU, Kyoto U.)

Starting from 2008:
Cooperation between ISTEC and AIST
LTS device developments AIST and ISTEC

2008
Collaboration start

2012
CRAVITY establishment

2013
AIST/ISTEC unification

2017

AIST

10 V programmable voltage standard

SFQ RDP

100-pixels STJ array

Nb 9-layer device

SFQ A/D converter

ISTEC

Digital devices

100 GHz SFQ processor

100k gate AQFP SFQ microprocessor with memory

SFQ-SSPD monolithic device

Analog devices

3D-1024 pixels STJ array

Microwave SQUID multiplexer

CRAVITY: Clean room for analog-digital superconductivity

Supply destinations of CRAVITY devices
The Jaguar XT5 supercomputer at Oak Ridge National Laboratory (on left) and the conceptual superconducting supercomputer (on right) both perform at 1.76 petaflops, but the Jaguar XT5 consumes over 7 MW; whereas, the superconducting one consumes 25 kW. (Jaguar XT5 image credit: Cray Inc.)

From Marc A. Manheimer in "The Next Wave, Vol. 20, No. 2 (2013)"
Power Consumption of Supercomputers => C3–Project

Replace RSFQ logic with energy-efficient logic like:
- RQL (Northrop Grumman),
- ERFSQ/eFSQ (Hypres)

Very low power alternative:
- Adiabatic Quantum Flux Parametron AQFP
  (e.g. Yokohama National University)

Most urgent problem: Superconducting Memory
Nanopillar Hybrid JJs

Current-induced switching (Ni/Cu/Ni)

H = 0

Higher threshold

Lower threshold

4 K

75 nm x 150 nm


Thinner layer as FL:
Regular STT effect
Future

- Combination of Qubits with Superconductive Readout (like DWave Co.)
- Secure transmission over long distances
- Storage Elements (magnetic JJs or nano-loops)
- Scaling!!!
- Digital: Fast and Low Energy (Low Power SFQ and Reversible Computing)
- Neuromorphic circuits with superconductors
Future

**HTc Superconductive Electronics**

-> NO widespread applications with LTS!!

-> multilayer thin film techniques

-> reproducible junction technology

-> needs (big) investment in fabrication technology
Largest SQIF array with SEJs, \( N=100,200 \)
Best sensitivity to date: \( V_B = 23,000 \text{ V/T} \)

- 100200 junctions
- 45% spread area
- \( \beta_L \sim 0.42 \) when \( I_c = 20 \text{ \mu A} \)
- \( R_N \sim 50 \text{ \Omega} \)
- \( I_b = 280 \text{ \mu A} \)
- Voltage modulation \( \sim 20.5 \text{ mV} \)
- Sensitivity \( \sim 23,000 \text{ V/T} \)
He ion-damage junctions

Maskless direct-write ion implantation

![Image of implantation of a YBCO crystal](image1.jpg)

Carl Zeiss Orion Nanofab: He-ion 35 keV 0.5 nm

<table>
<thead>
<tr>
<th>Voltage (µV)</th>
<th>Current (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>500</td>
<td>100</td>
</tr>
<tr>
<td>1000</td>
<td>200</td>
</tr>
</tbody>
</table>

$R_0 = 5.25\Omega$

$2\times10^{16}$ ions/cm²

S. A. Cybart et al.,
Nature Nanotechnology 10.
p 598, 2015
Future

We need to make the step from scientific to engineering operation.
Future

Without technology advances and the step from scientific to engineering operation:

Superconductive Electronics will stagnate.
Future

With technology advances and the step from scientific to engineering operation:

Superconductive Electronics will flower!!
Happy 30th anniversary to the ISS!