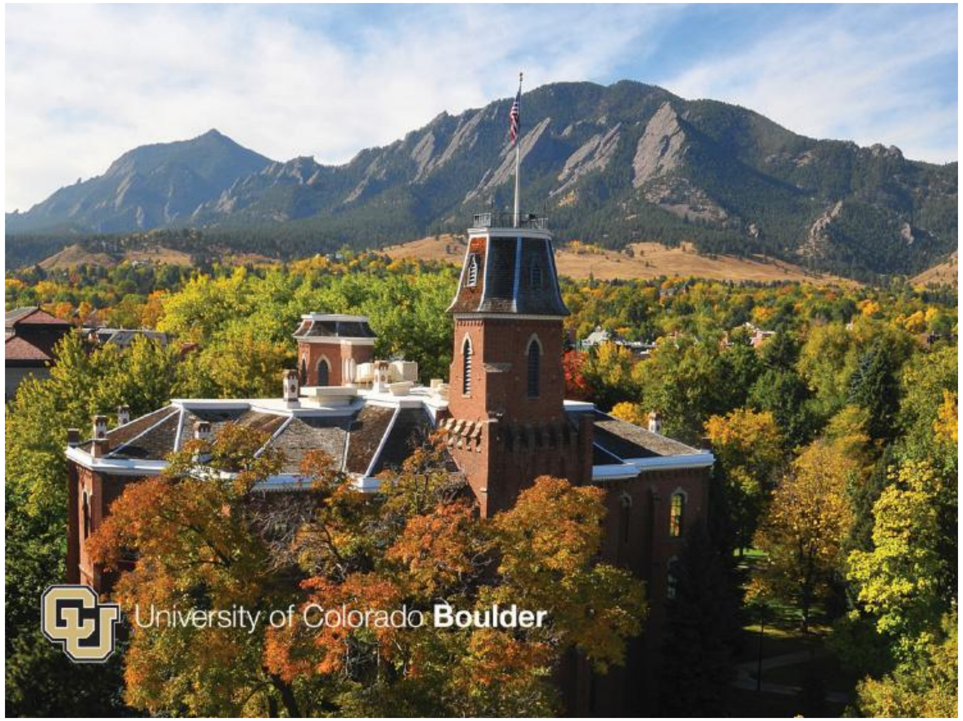
IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), February 2018.
Plenary presentation PL6-INV was given at ISS 2017, December 13-15, 2017, Tokyo, Japan.

30 Years of History and Future Perspectives of Superconducting Electronics



Horst Rogalla

University of Colorado at Boulder
(ECEE Department),
Boulder, USA

NIST
(Superconductive Electronics)
Boulder, USA

and

IEEE Council on Superconductivity

University of Colorado
Boulder

IEEE

NIST
National Institute of Standards and Technology

30 years of history don't seem long seen the age of superconductivity of 106 years.

But: a lot happened in these last 30 years:

- Commercial LCD Flat Screen TVs
- Blue LEDs
- The High-Tc "Revolution"
- The International Superconductivity Technology Center was founded
- New Applied Superconductivity Conferences started:
  ISS in 1988
  EUCAS in 1993
- Qubits
- Josephson π-junctions
- Magnetic Josephson junctions
- ...

- 1 November 1987: I became Physics Professor at the University of Twente in The Netherlands.

- Some of you were born in the last 30 years.

30 years of history don't seem long seen the age of superconductivity of 106 years

But so much happened in these last 30 years in Superconductive Electronics
that it would take hours to review the achievements.

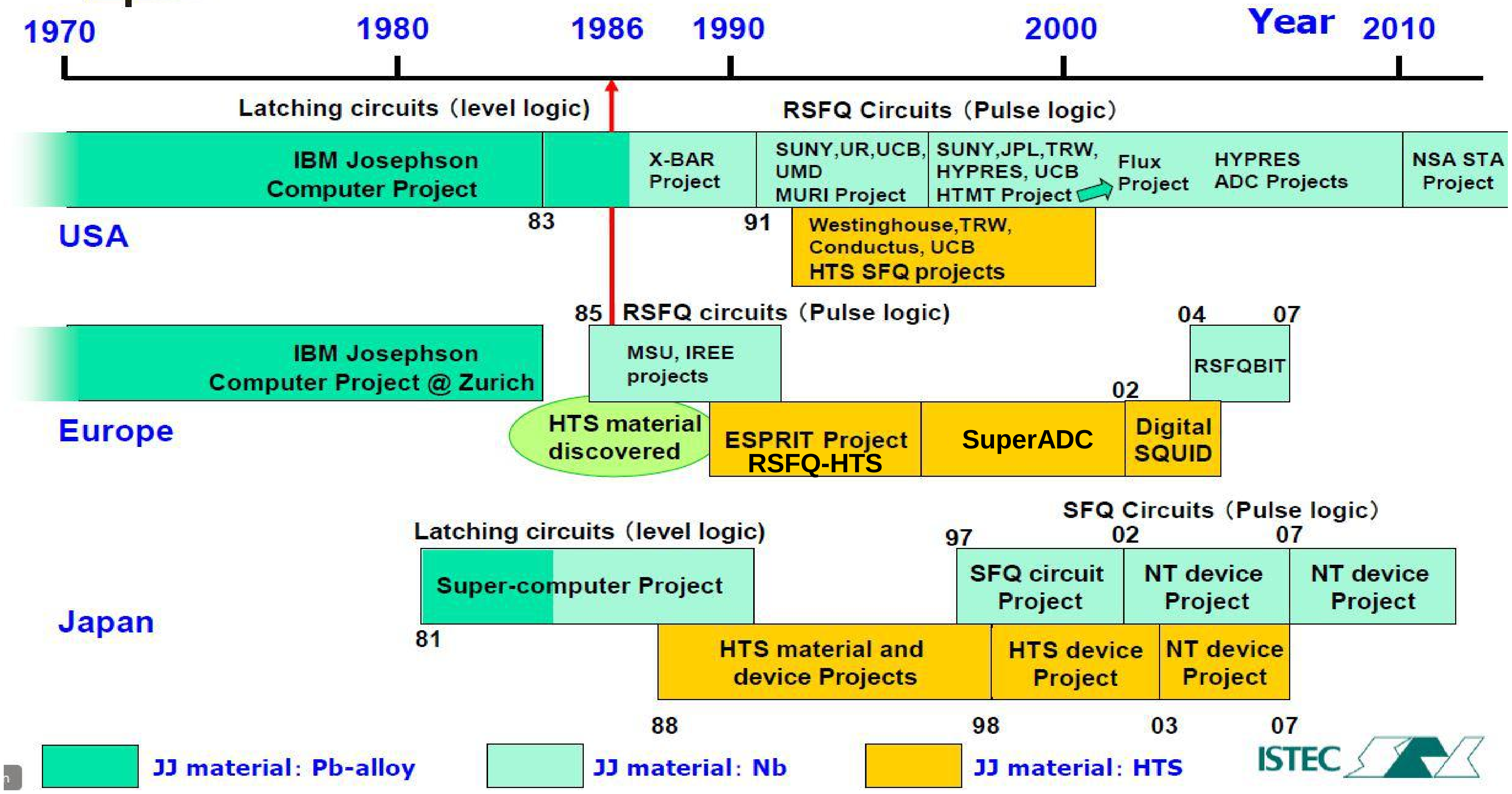
Session ED6 (Electronic Devices) - 30 Years of

SQUIDs	R.J. Ilmomiemi
Detectors	J.N. Ullom
Microwave Devices	S. Ohshima
Digital Circuits	A. Fujimaki
Quantum Information	J.-S. Tsai

→ A subjective (re-) view without any claim of completeness

Research flow of superconducting digital electronics*

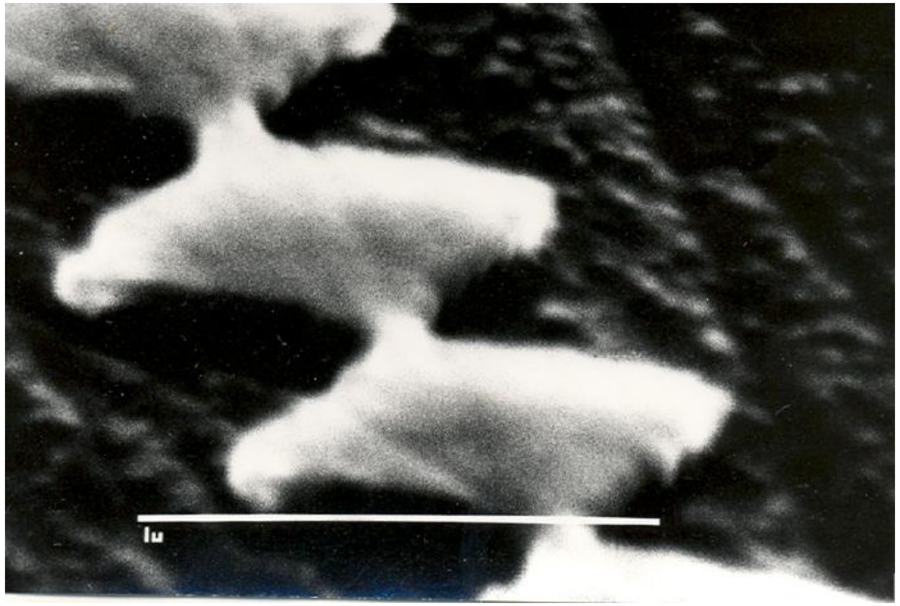
* This chart was drawn with a help of Dr. Bedard, Dr. Mukhanov, Prof. Rogalla, and Prof. Van Duzer.



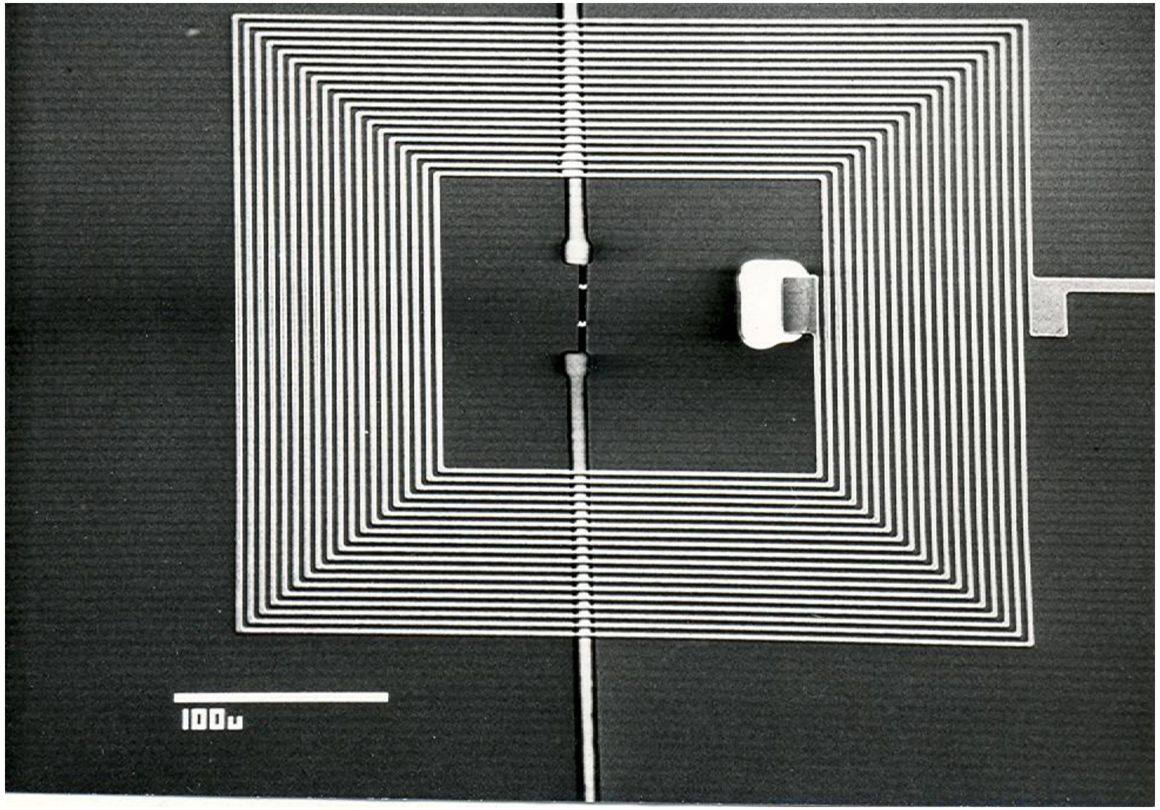
Prof. Hasuo
EUCAS 2011

HTS

First 'HTS' (Nb_3Ge) Applications



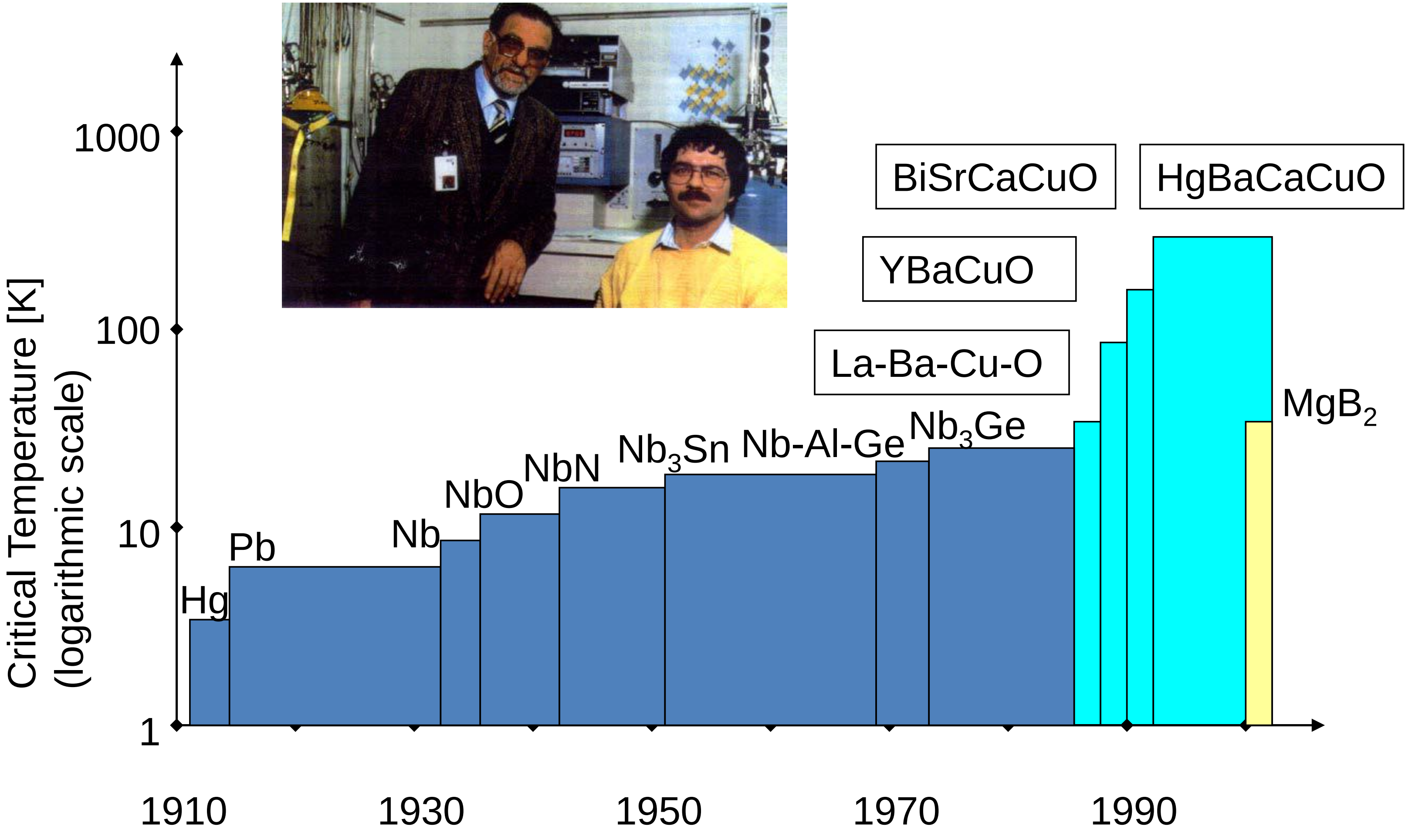
Serial array of Nb_3Ge nanobridges



H. Rogalla, M. Mueck et al. (1985)

Integrated Nb3Ge nano-bridge dc-SQUID operated in liquid hydrogen above 20K

Critical Temperature as Function of Time



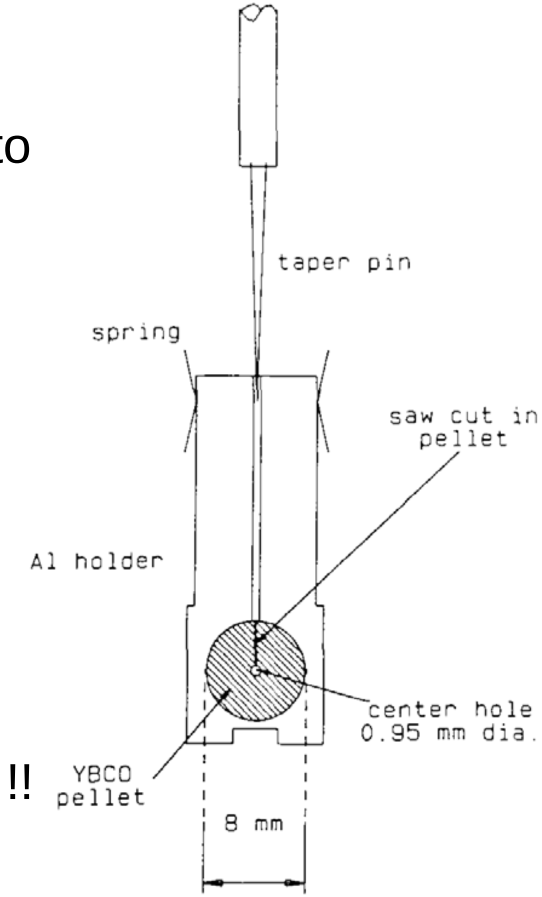
The Begin: How to fabricate an HTS-SQUID

Press and sinter powder into the form of a bulk cylinder,

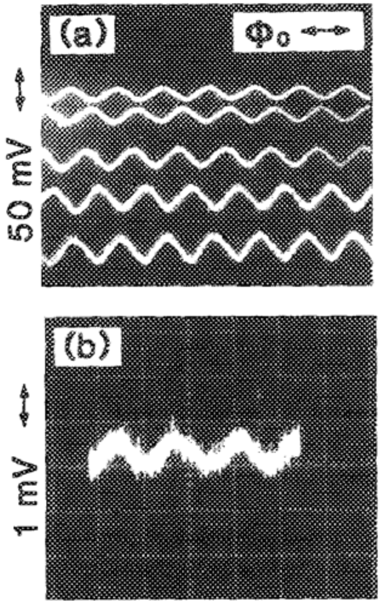
drill a hole and cut partially with a thin saw.

Break the link and press it together again with an adjustable screw or taper.

Voilà – the SQUID is ready !!



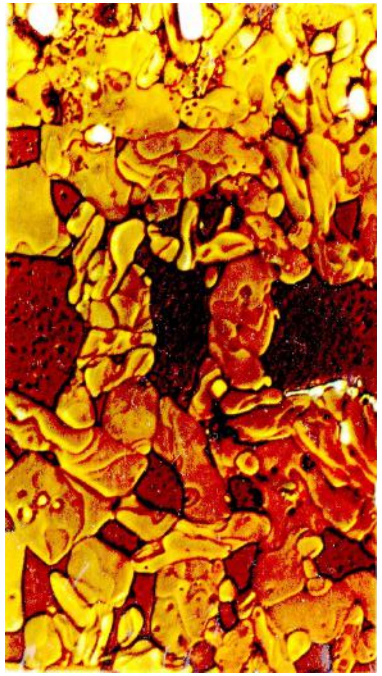
4.2K



81K

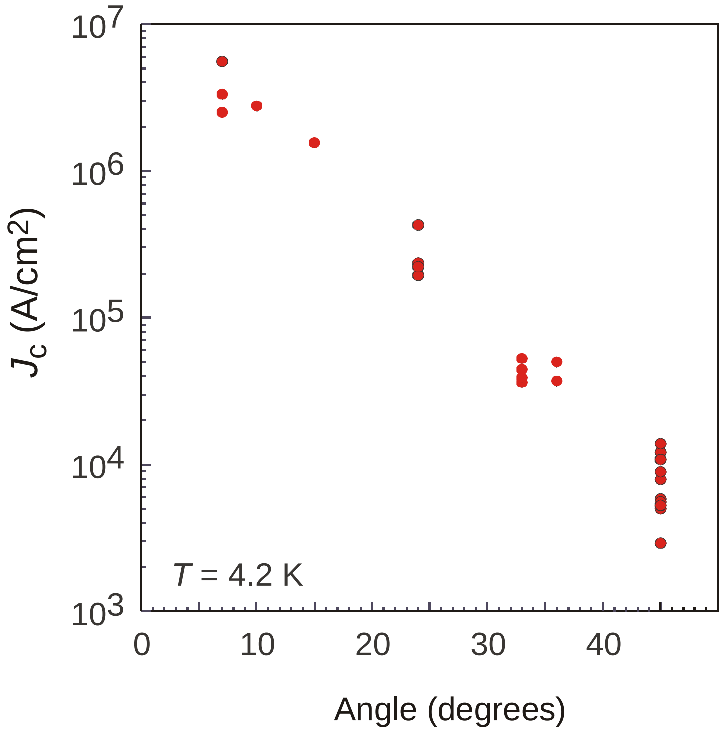
J. E. Zimmerman, J. A. Beall, M. W. Cromar, and R. H. Ono: Appl.Phys.Lett. 51, 617 (1987)

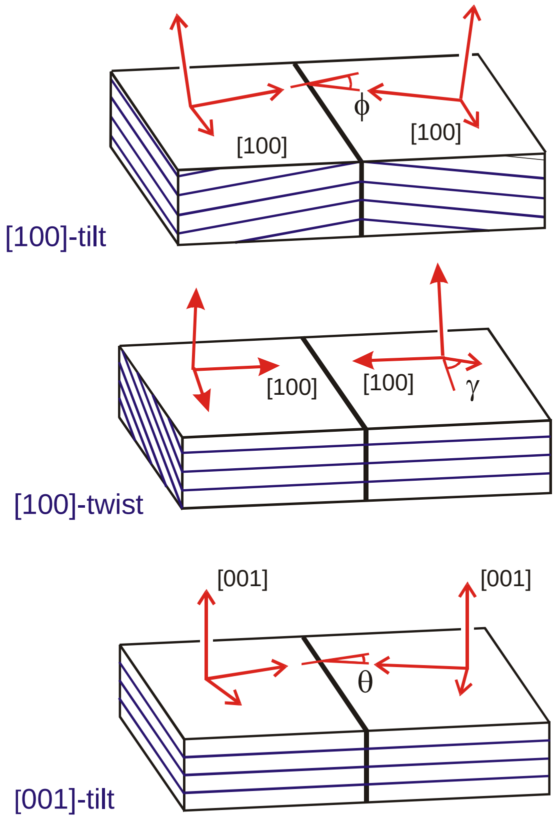
Polycrystalline junctions

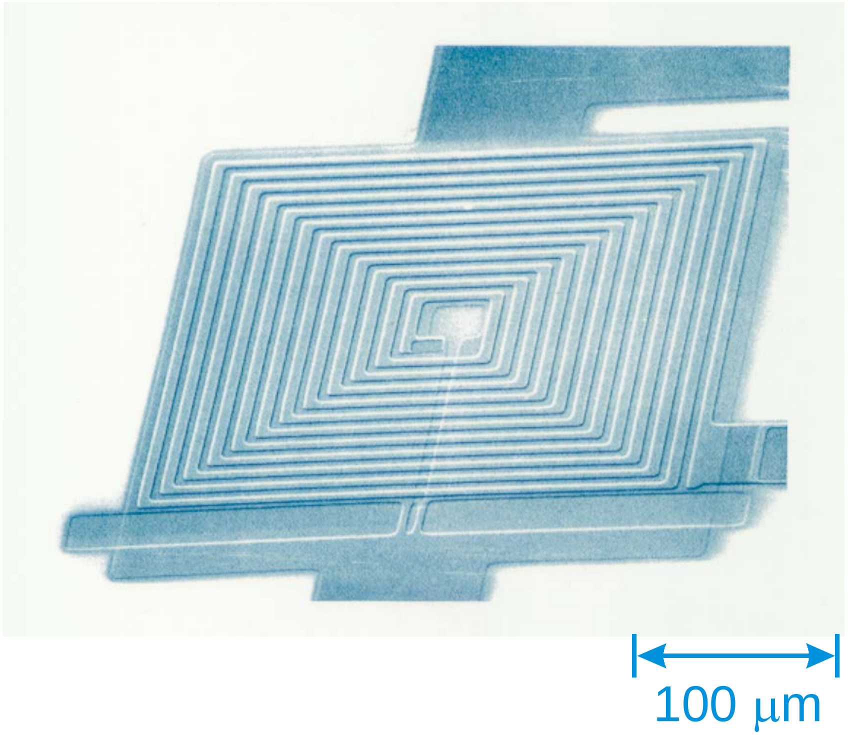


R.Koch, IBM; Twente (1987)

Bi-crystal Grain Boundary Junctions







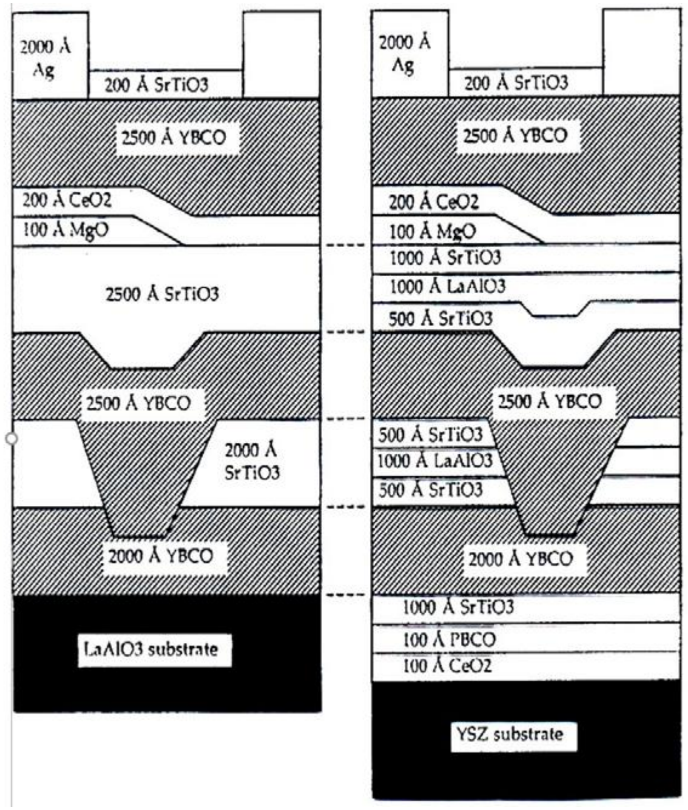
Hilgenkamp & Mannhart, *Appl. Phys. Lett.* **73**, 265 (‘98)

Dimos D., Chaudhari P., Mannhart J., Le Goues F.K.: Phys.Rev.Lett. 61, 219 (1988)

H. Hilgenkamp, H. Rogalla et al., Appl. Phys. Lett. **64**, 3497 (‘94).

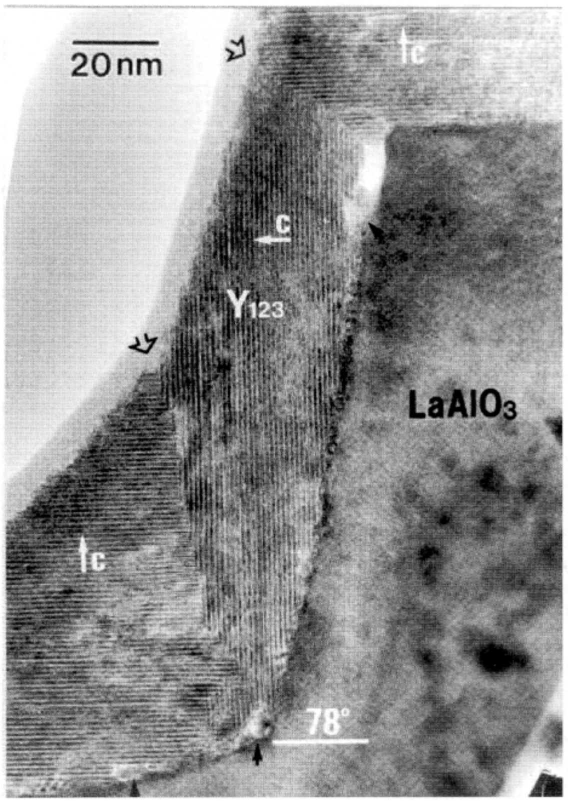
The Begin: Thin Film Josephson Junctions

Template Junctions

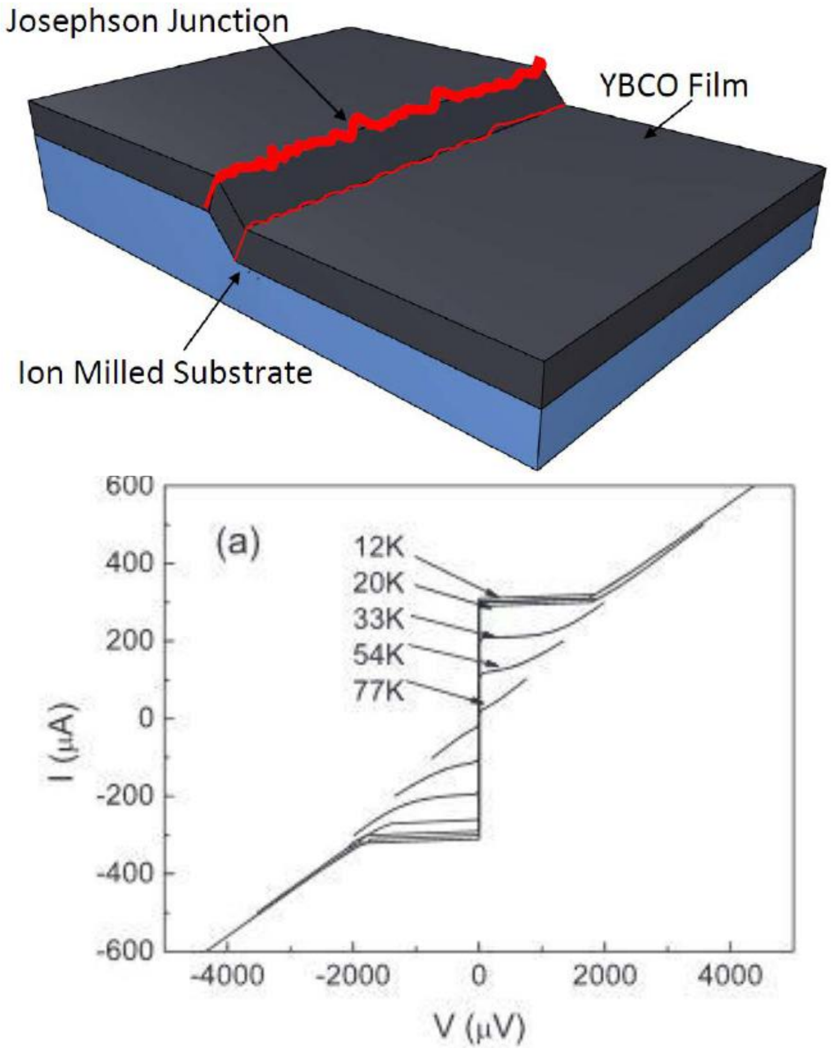


L.P. Lee, K. Char, et al. (Conductus Inc.)

Step-edge junctions

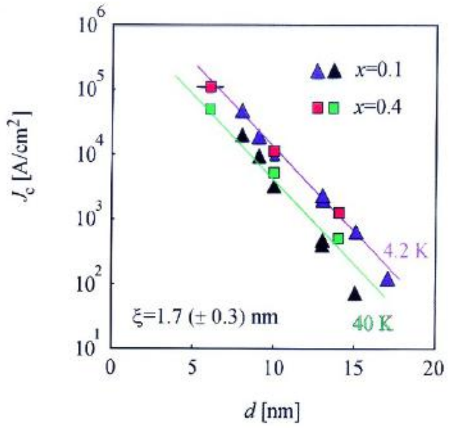


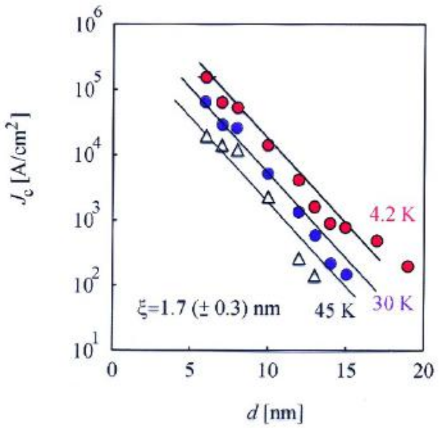
Jia et al. Physica C 175, 545 (1991)

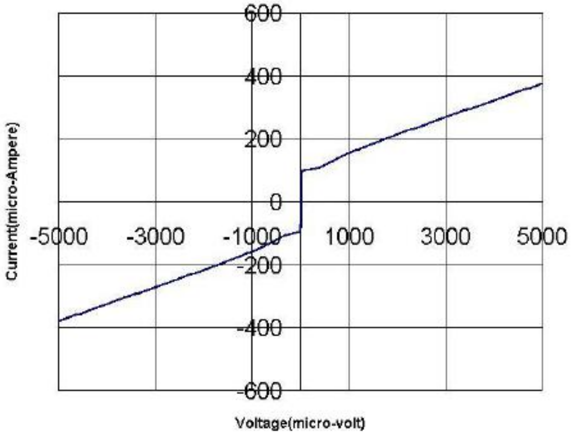


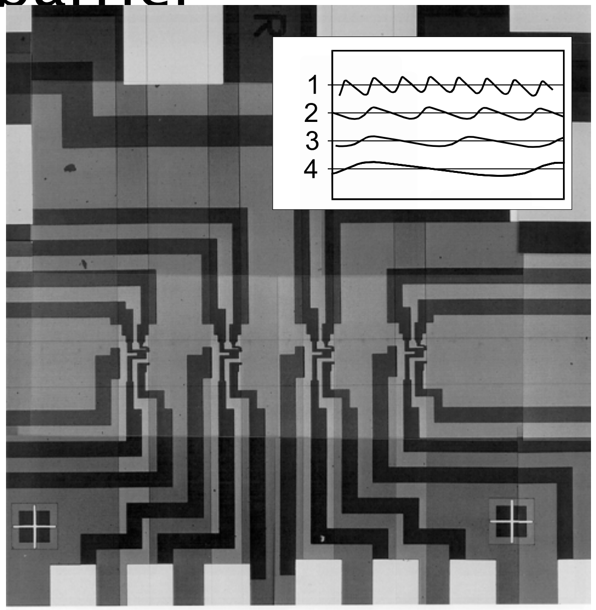
J. Du et al. Supercond. Sci, Technol. **21**, 125025 2008.

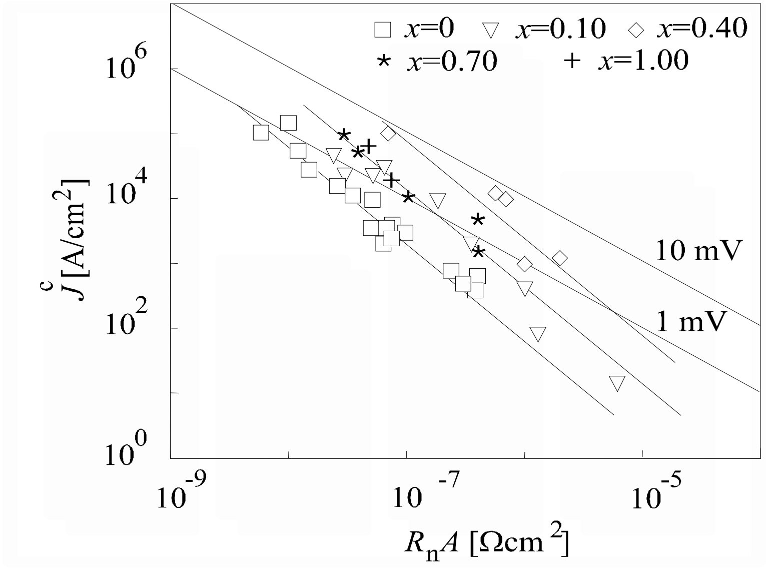
Ramp-type Junctions with Ga-doped PBCO barrier



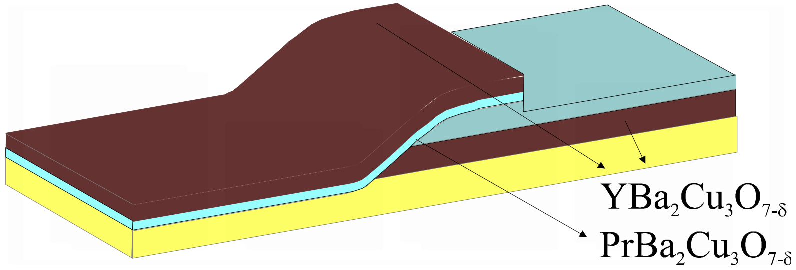


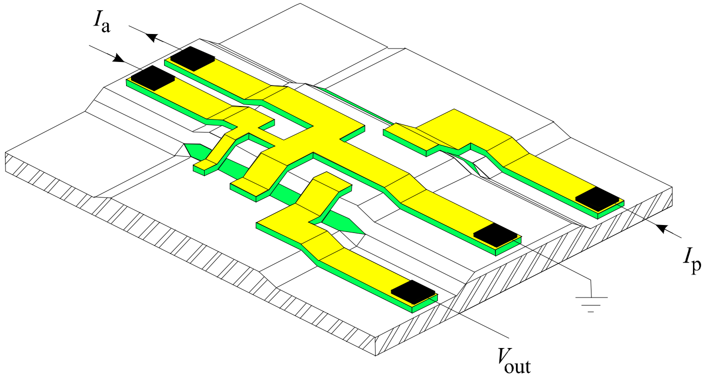






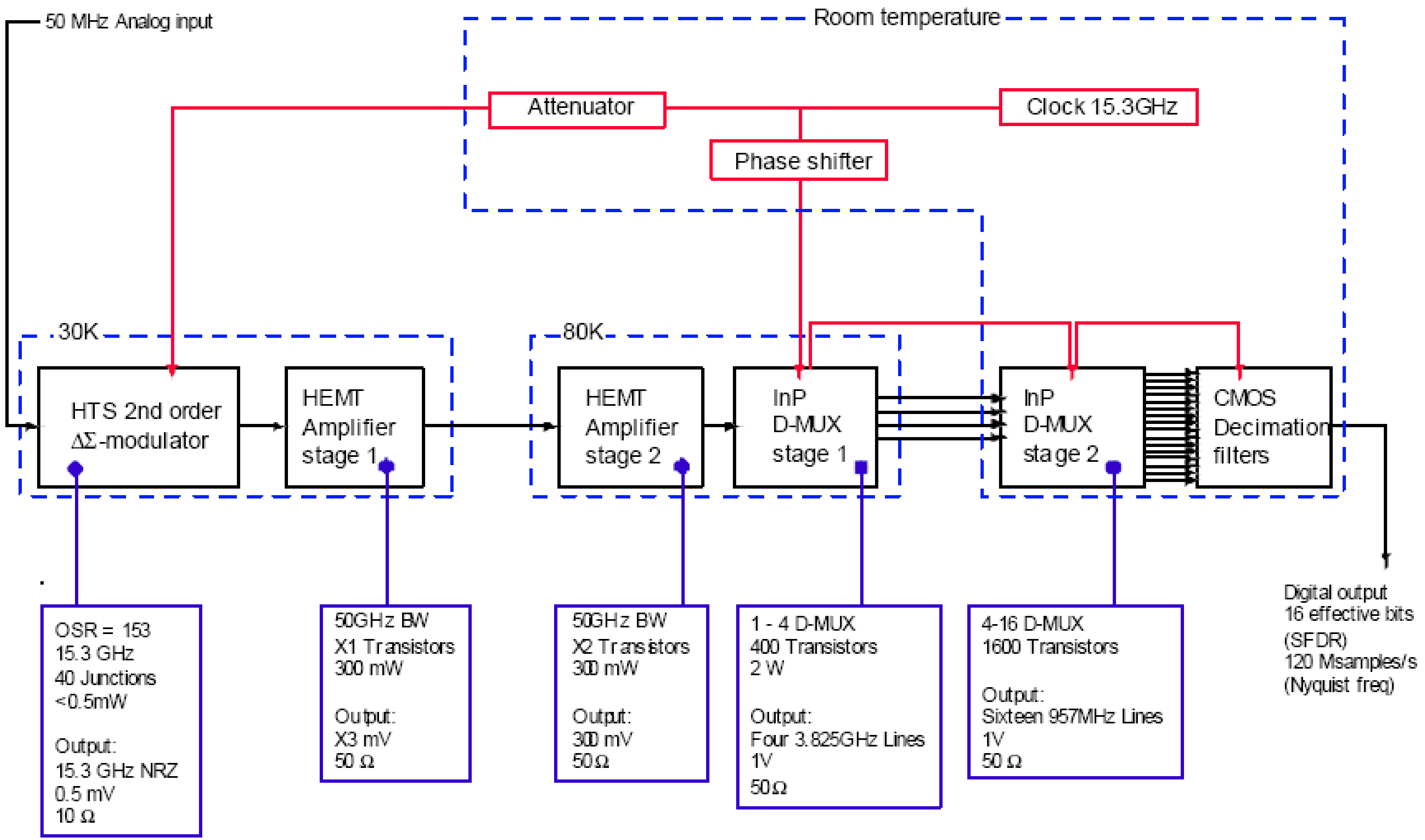
Barrier thickness and Ga-doping of PBCO are design parameters



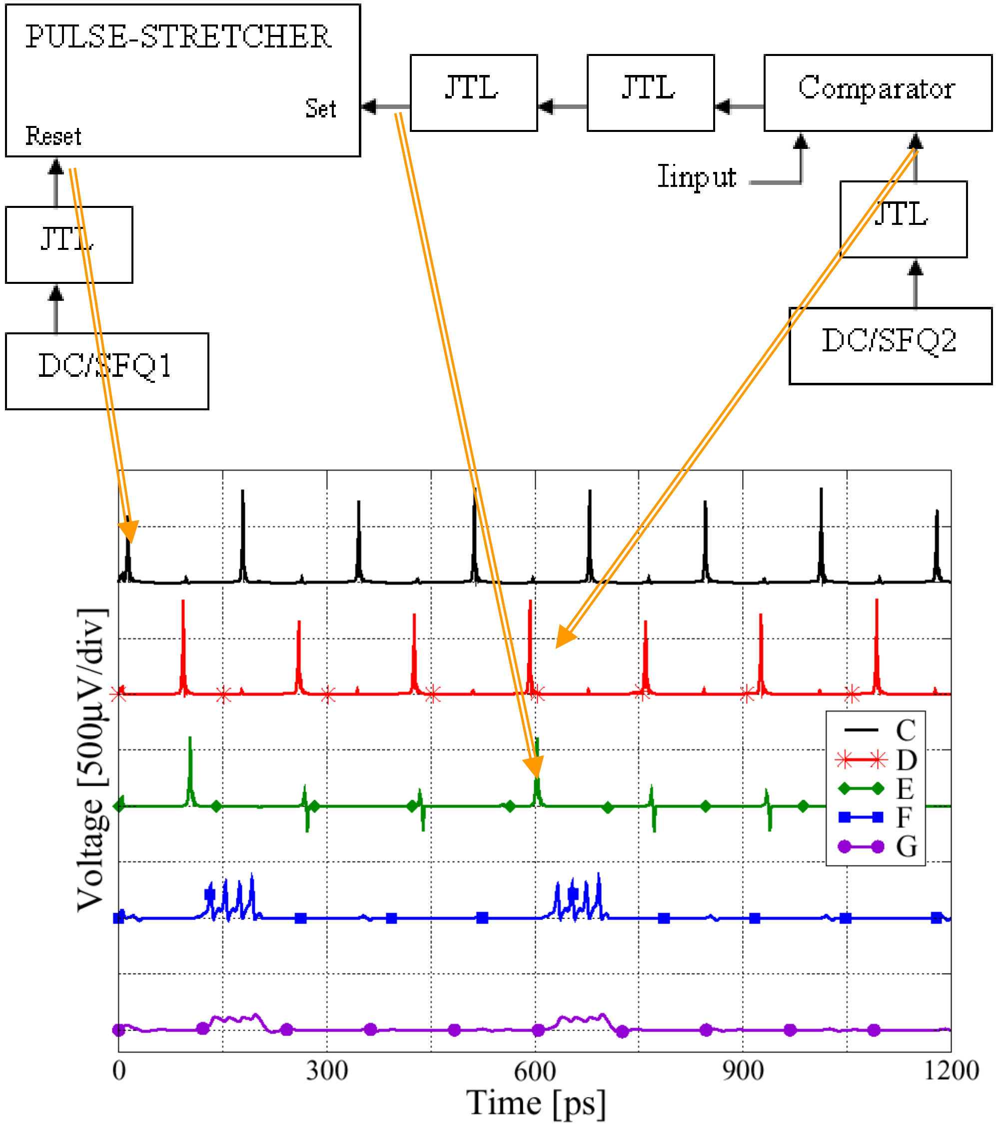


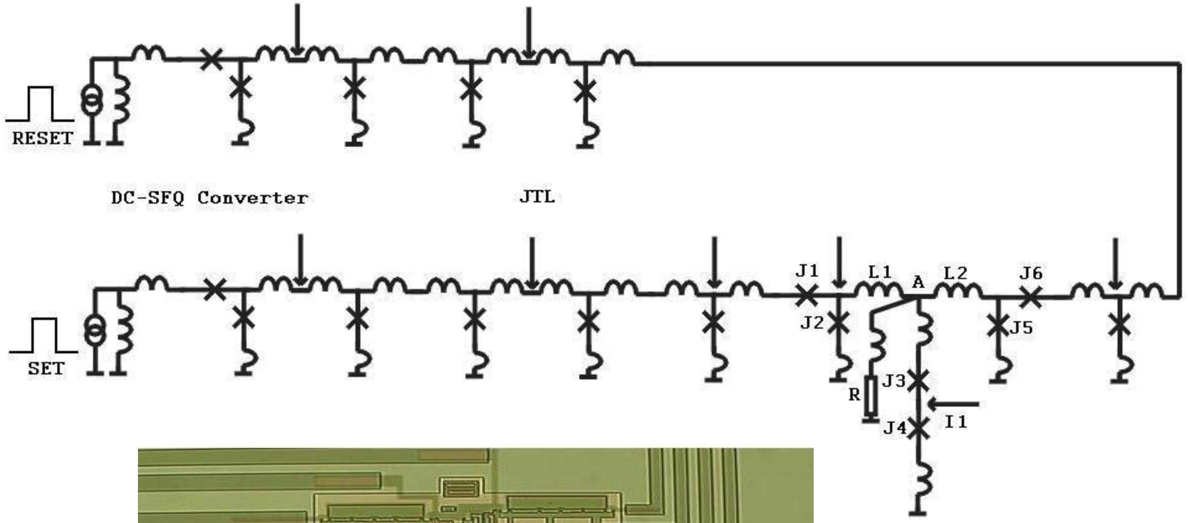
J.Gao, Y.M. Boguslavskij, B.B.G. Klopman, D. Terpstra, G.J. Gerritsma, H. Rogalla , Appl.Phys.Lett 59, 2754 (1991)

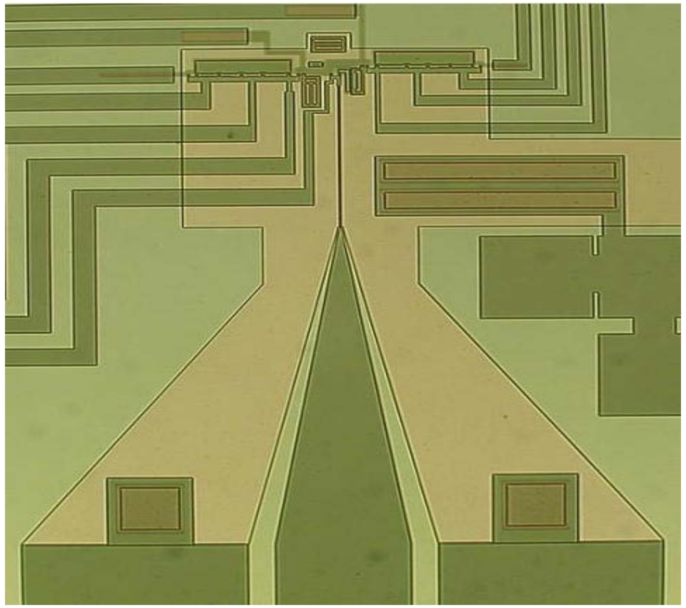
SuperADC


50 MHz Analog input
Room temperature
Attenuator
Clock 15.3GHz
Phase shifter
30K
80K
HTS 2nd order
ΔΣ-modulator
HEMT
Amplifier
stage 1
HEMT
Amplifier
stage 2
InP
D-MUX
stage 1
InP
D-MUX
stage 2
CMOS
Decimation
filters
OSR = 153
15.3 GHz
40 Junctions
<0.5mW
Output:
15.3 GHz NRZ
0.5 mV
10 Ω
50GHz BW
X1 Transistors
300 mW
Output:
X3 mV
50 Ω
50GHz BW
X2 Transistors
300 mW
Output:
300 mV
50Ω
1 - 4 D-MUX
400 Transistors
2 W
Output:
Four 3.825GHz Lines
1V
50Ω
4-16 D-MUX
1600 Transistors
Output:
Sixteen 957MHz Lines
1V
50 Ω
Digital output
16 effective bits
(SFDR)
120 Msamples/s
(Nyquist freq)

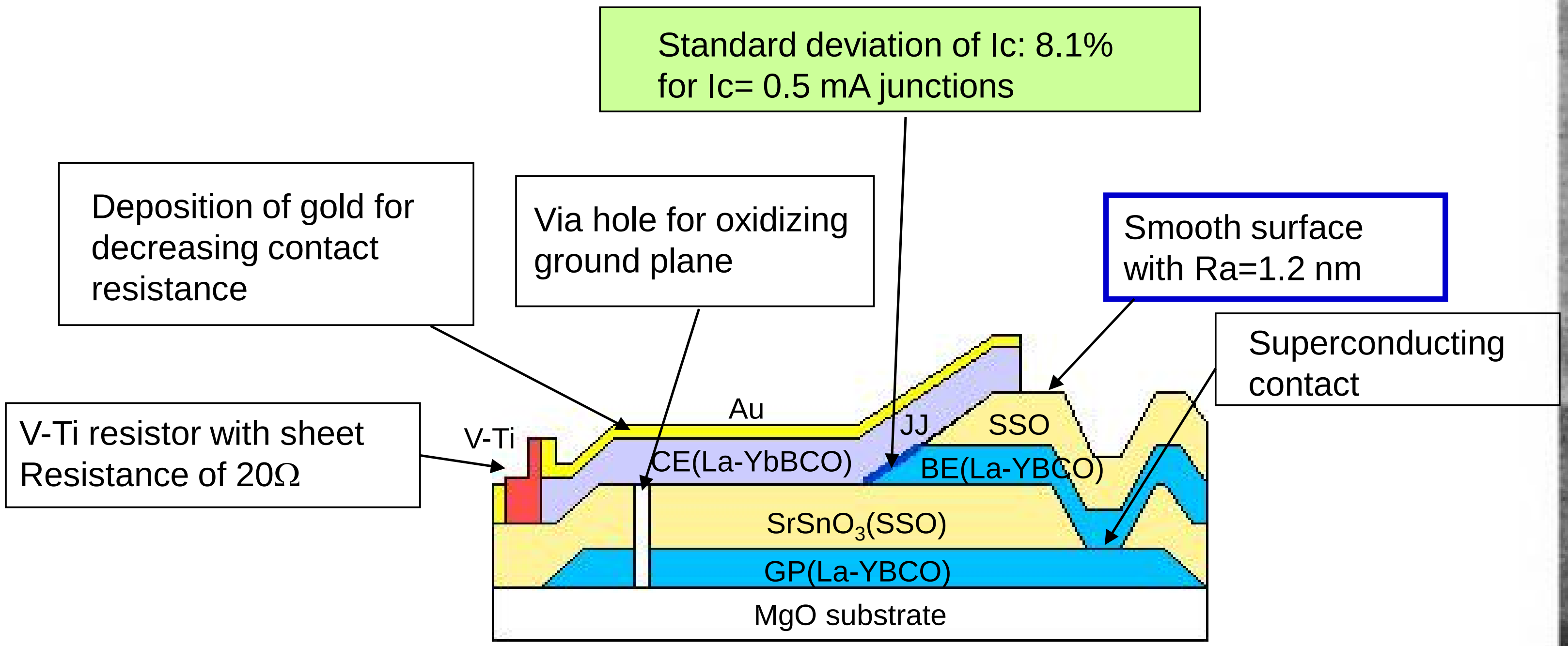
Pulse Stretcher (Twente, SuperADC)

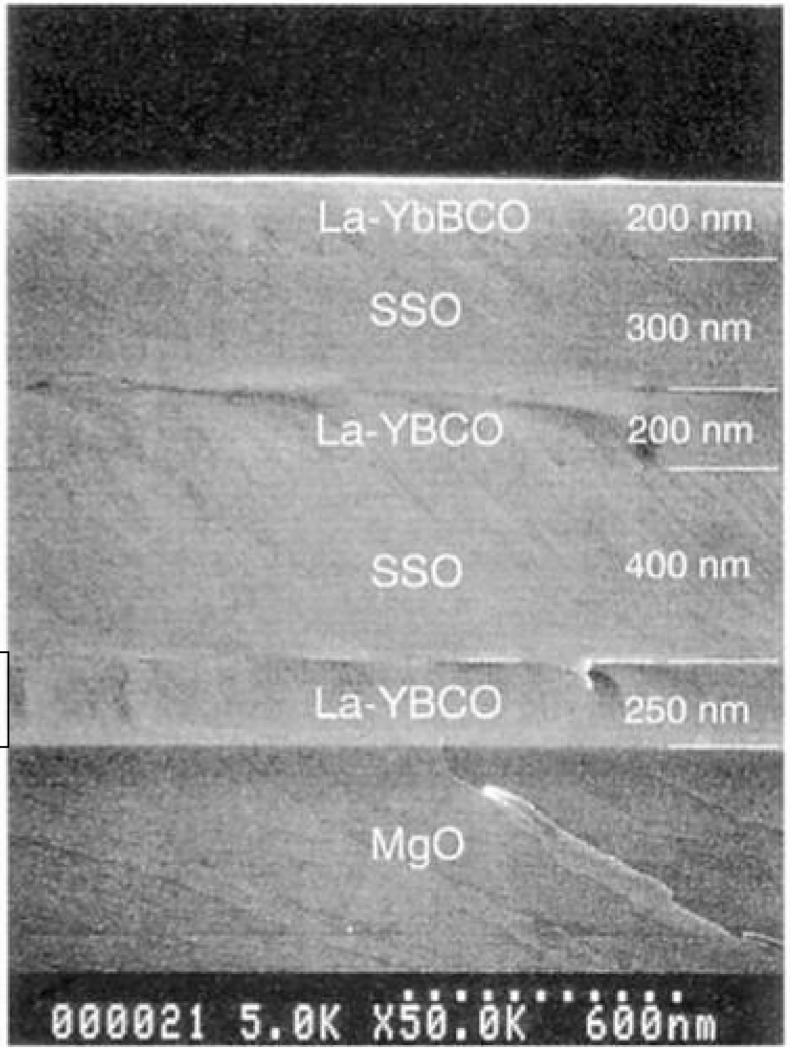






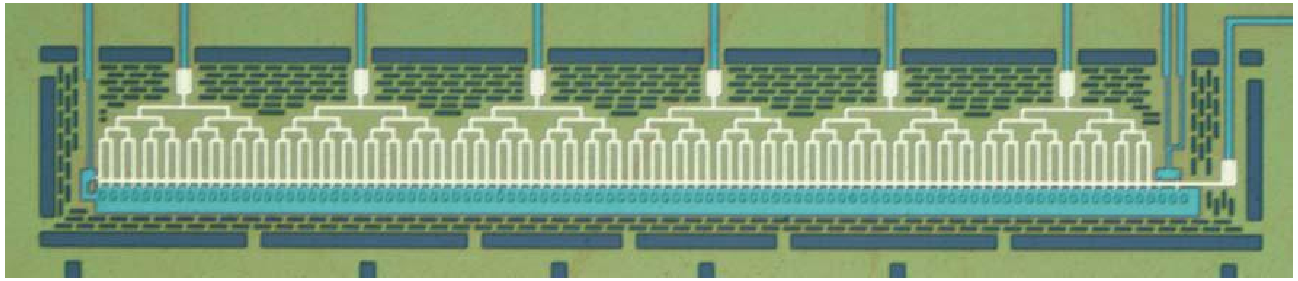
Multi-Layer HTS Integration with Ramp-Type Junctions (ISTEC)



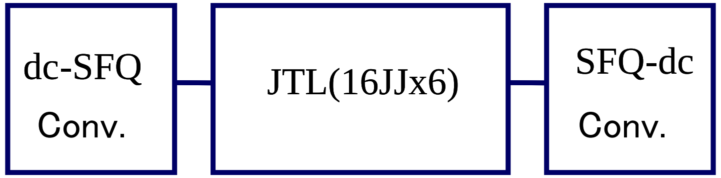


Hasuo, ISTEC, Summerschool on Superconducting Electronics (2005)

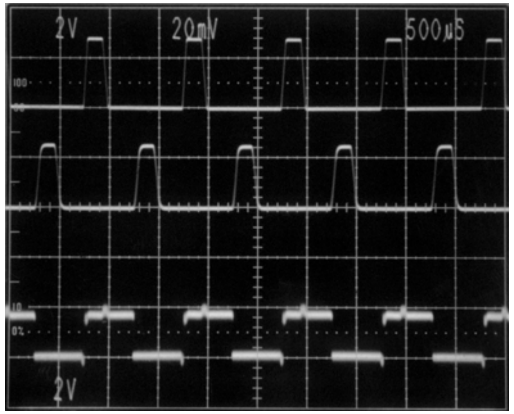
HTS 100 JJ circuit（ISTEC)



Circuit including 101 JJs

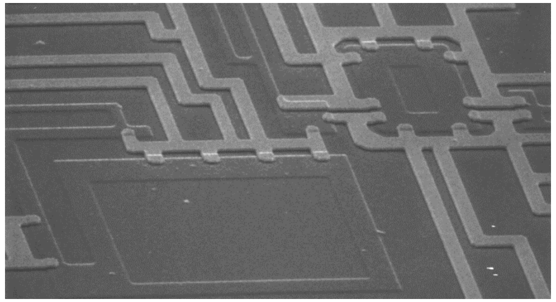


Circuit

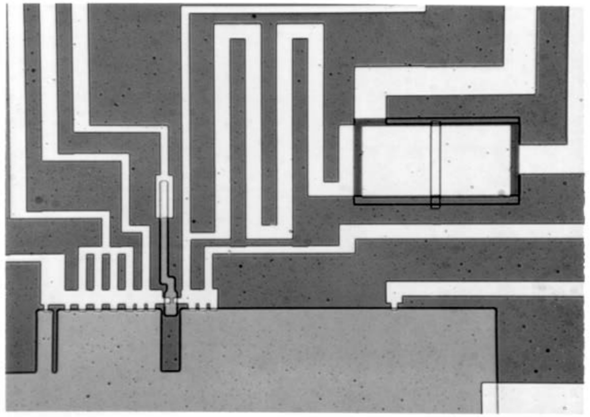


Operation at 29 K

Ref: H.Wakana et al （ISTEC), ISS2004



Ring Oscillator (21 JJ, Toshiba) 57 GHz @20K



∑-Δ AD modulator (13 JJ, Hitachi) 100 GHz @20K

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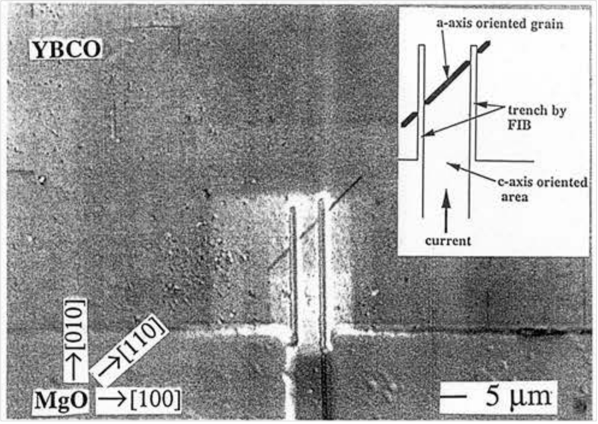
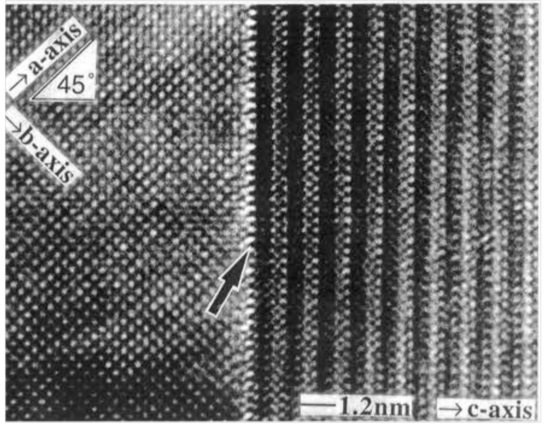
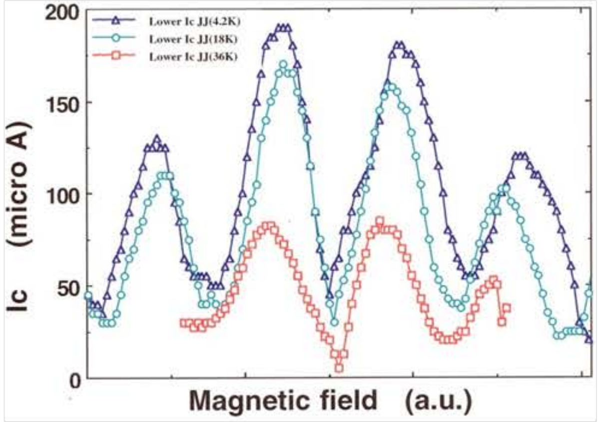
R&D of thin films and electronic devices at ISTEC in the first decade (‘88-’97)

- High-quality Nd123 thin films with atomically flat surfaces
- Grain-boundary junctions and device physics
- Hg-1212 GB JJ and SQUID which can be operated at > 110 K

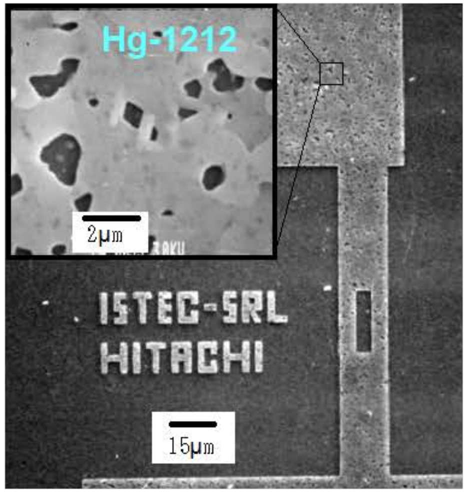


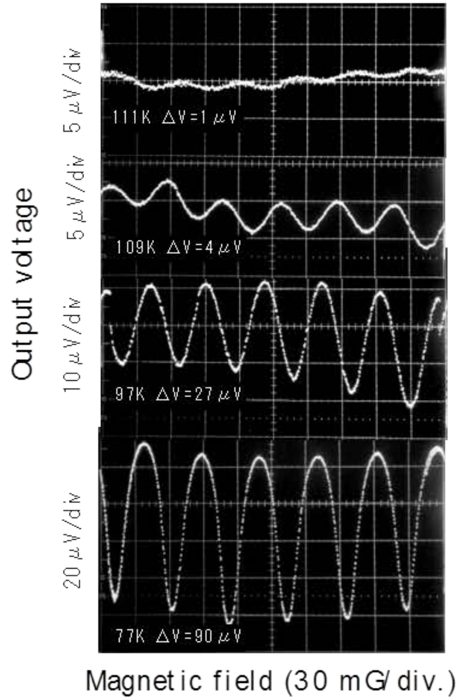


A. Tsukamoto *et al*., Appl. Phys. Lett. **73**, 990 (1998).



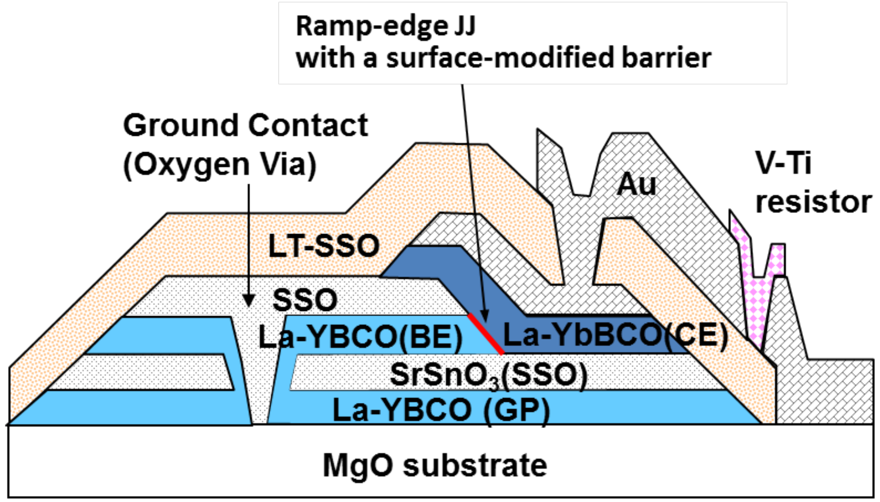
Y. Ishimaru *et al*., Phys. Rev. B **55**, 11851 (1997).





Dr. K. Tanabe

HTS multilayer technology developed at ISTEC for SFQ circuits (2000's)

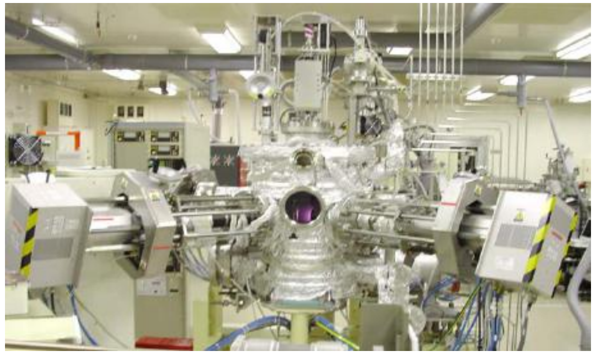


3 RE-123 layers with $SrSnO_3$ (SSO) insulator

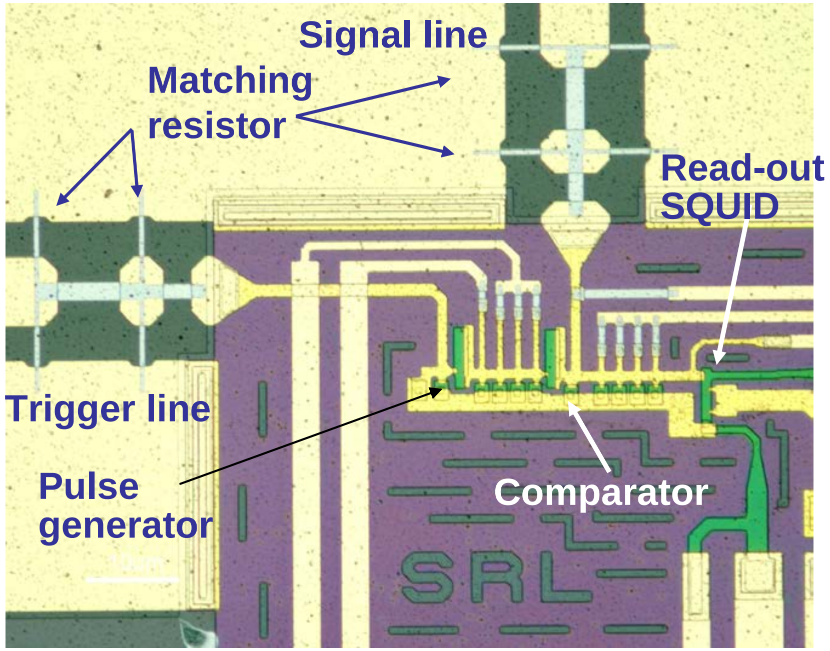
R_a of sputtered multilayer < 2 nm

Ramp-edge JJs with 1σ I_c spread 5-10 %

Minimum junction width of 1.5 μm



ISTEC

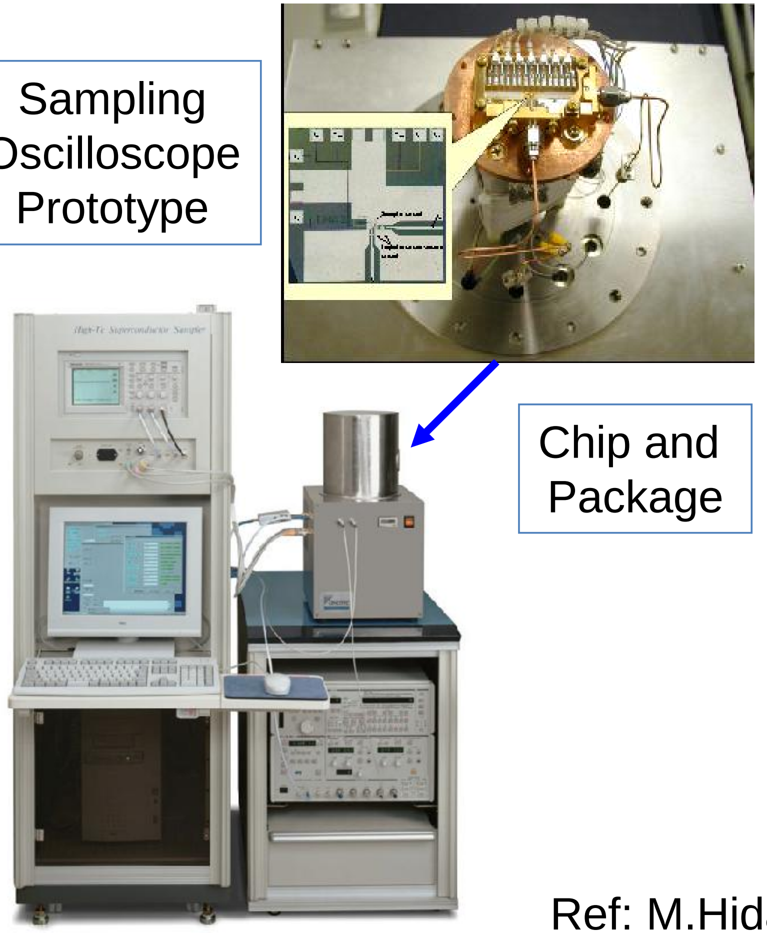


HTS Sampler circuit with a potential bandwidth over 100 GHz
(15 JJs integrated)

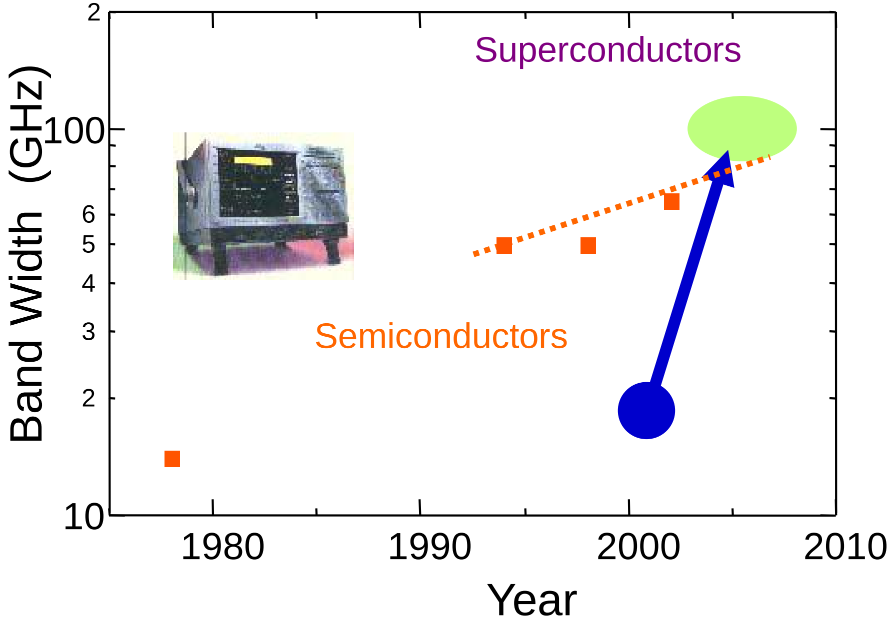
Dr. K. Tanabe

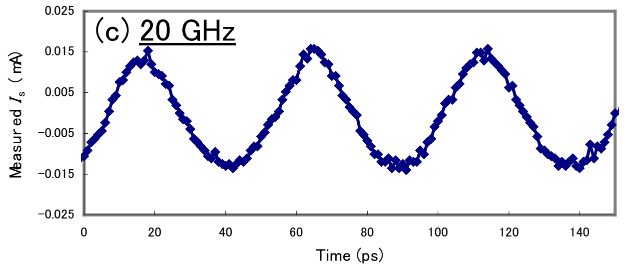
Superconducting sampling oscilloscope

Sampling Oscilloscope Prototype



Chip and Package

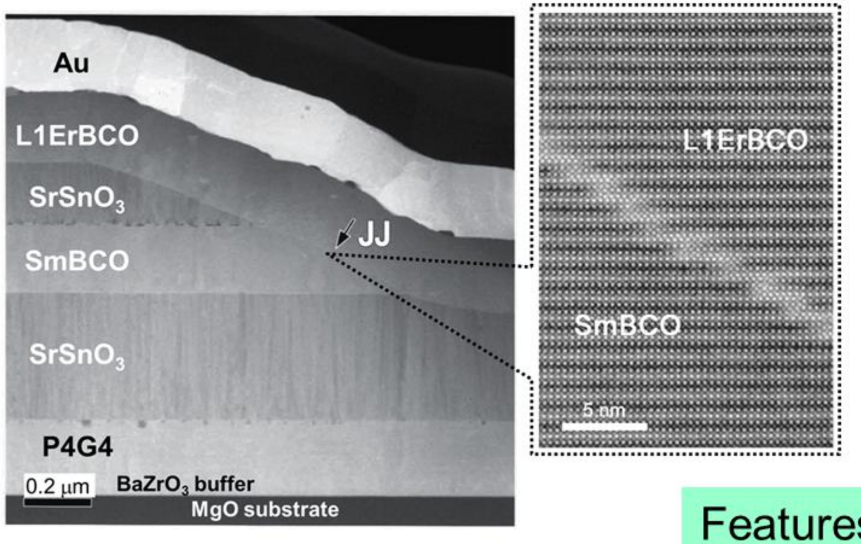


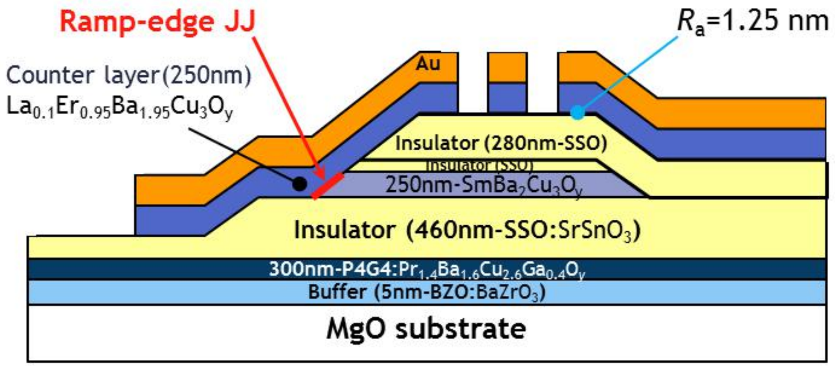


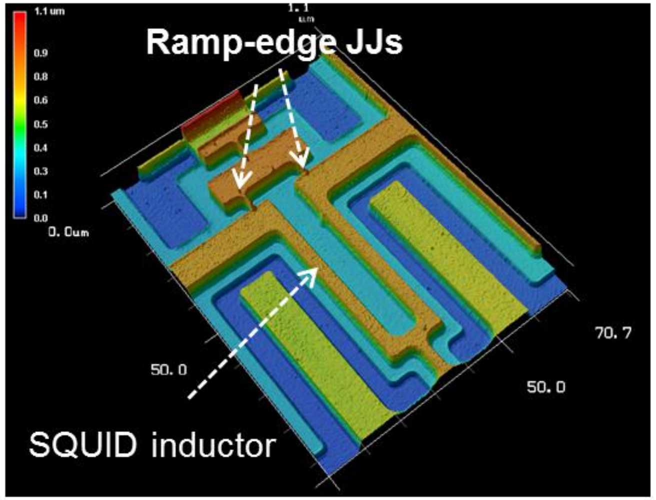
Ref: M.Hidaka (NEC) et al., ASC 2000

Waveform of 20GHz

HTS SQUIDs with multilayer structure and ramp-edge JJs (2007～)







Features

*Integrated circuit structure with several oxide layers

*High-angle GB is eliminated from JJs and coils

Advantages

*Stable operation at 77 K

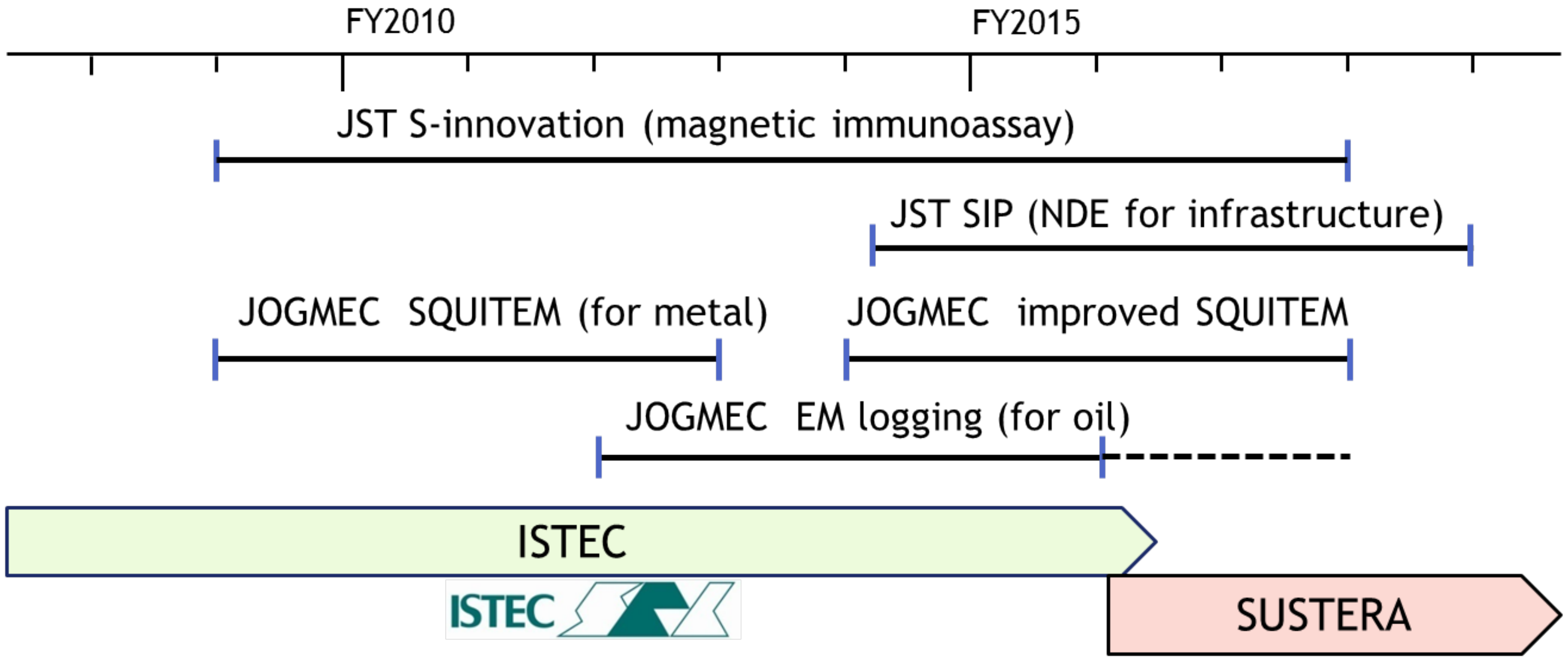
*Easy to fabricate multi-channel array sensor

*Robust against application of magnetic field

*High field sensitivity approaching LTS SQUIDs

Dr. K. Tanabe

Development of HTS-SQUID systems at ISTEC and SUSTERA



SUSTERA is the mutual aid organization (nonprofit organization) in which members conduct collaborative research on the sensing technology based on HTS-SQUIDs.

Members:
+ Fujitsu Ltd.
+ The Chugoku Electric Power Co., Inc.
+ Mitsui Mining & Smelting Co., Ltd. (MINDECO until March 2017)
+ (ISTEC until June, 2016)

Products: HTS-SQUID chip (module), compact cryostat, etc.

Dr. K. Tanabe

SQUITEM-III system
for exploration of metal resources

Commissioned by JOGMEC

- # Compact design
- # Vacuum maintenance free
- # Keep LN_2 for 17 h
- # > x 10 higher slew rate (> x 20 higher S/N)

T. Hato *et al*., SUST **26** (2013) 115003.

Actual exploration in Peru

Development of improved SQUITEM-III (FY2015-FY2016)
x, y, z 3-component SQUID sensors tested in Australia field

JOGMEC ISTEC MINDECO SUSTERA

Development of long-range EM logging system - Application to oil field -

ISTEC MINDECO JOGMEC

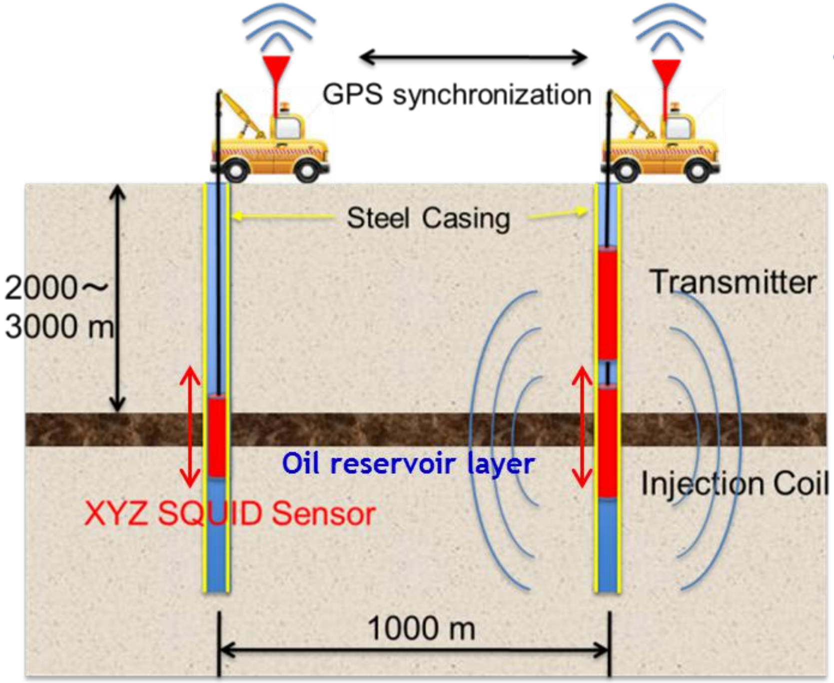


Image of crosshole EM (logging) system with HTS-SQUID magnetometer (Resistivity tomography between two wells)

Target: monitoring of CO_2 frontend in EOR

- Insufficient sensitivity of conventional induction coil sensor ⟹ short distance
- Owing to high sensitivity of SQUID even at low frequencies

EM in steel-cased wells with the distance > 1000 m expected

Technical challenges:

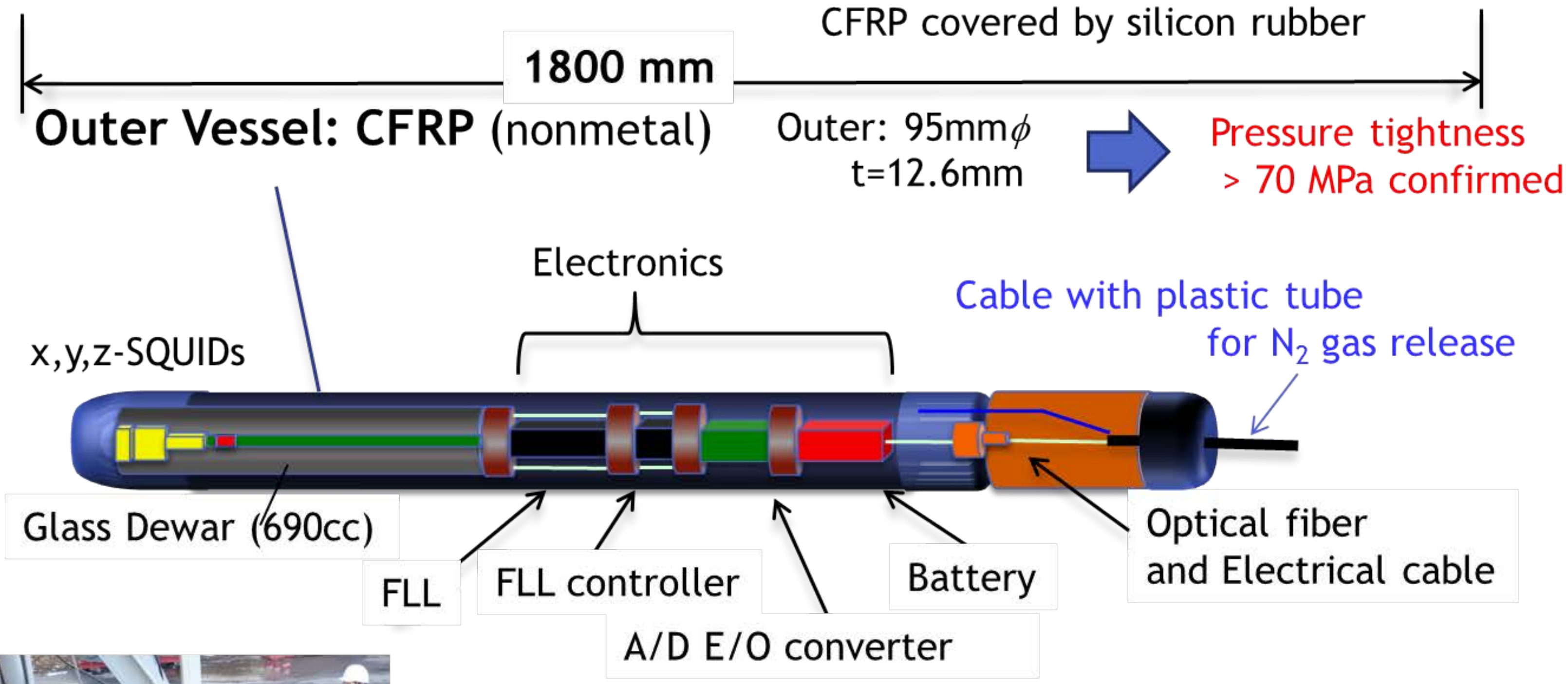
- Analysis technique to compensate influence of steel casing
- High-power transmitter & injection coil
- HTS-SQUID receiver (magnetometer) usable in high pressure (30-70 MPa) and high temperature (200 °C) environment
- Remote control of SQUID magnetometer

Development of elementary technologies started in 2012

FY2012 JOGMEC “Innovative technology in oil and gas development field” program
FY2013-2015 JOGMEC “Technical solution project”

Dr. K. Tanabe

SQUID receiver system for use in a test well

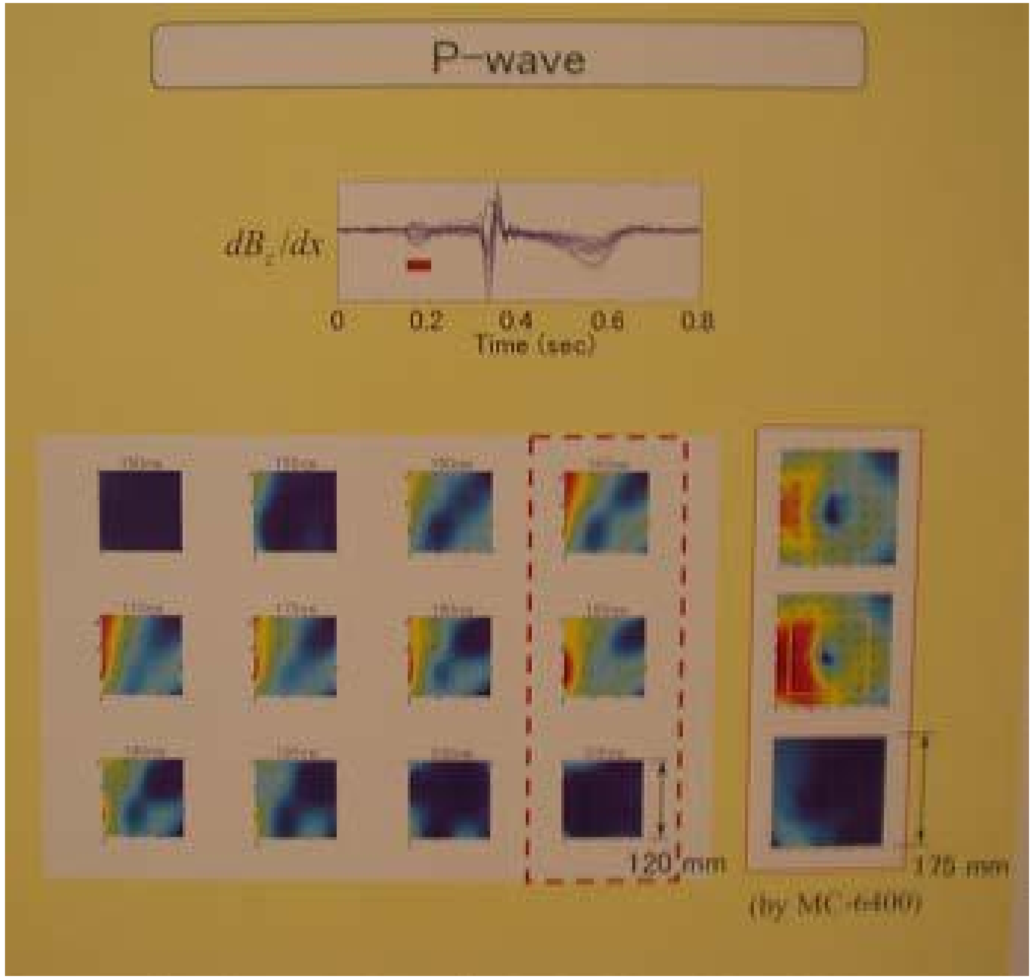


Field test at JOGMEC Kashiwazaki TF

/Stable operation at 300 m depth in a steel-cased well
/Detection of magnetic signal from 800 m distant emitter
/Control of SQUIDs through 3 km long optical fiber
confirmed

MCG (Hitachi)

HTS 16ch MCG



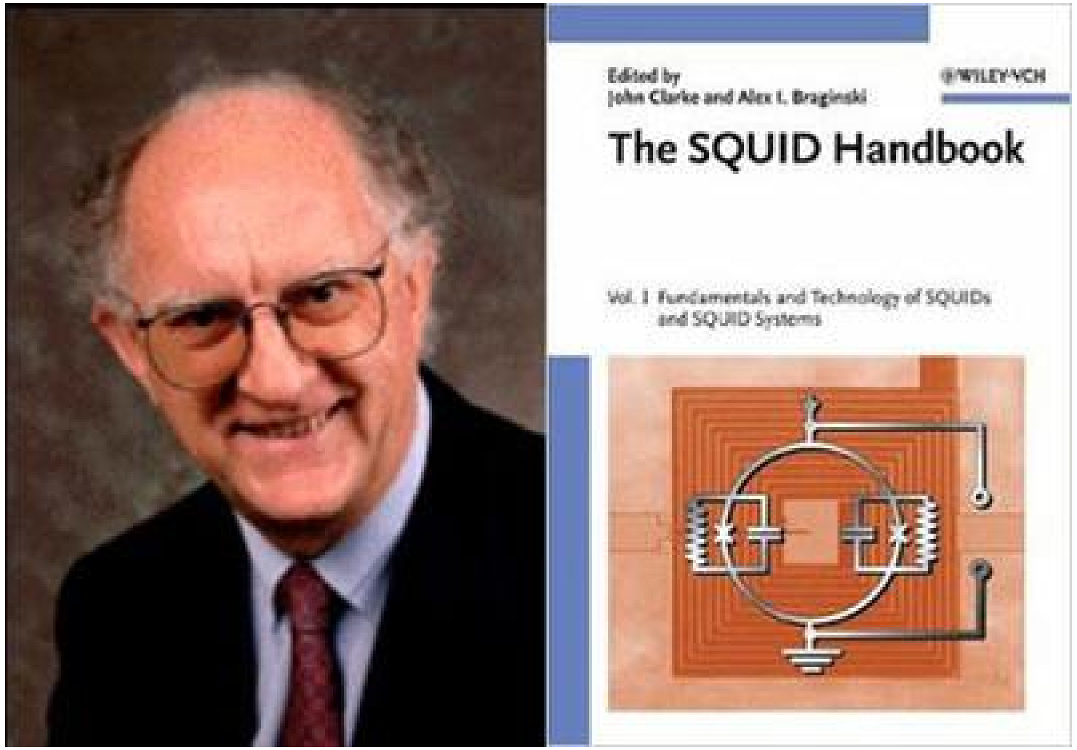
Harold Weinstock, 2005

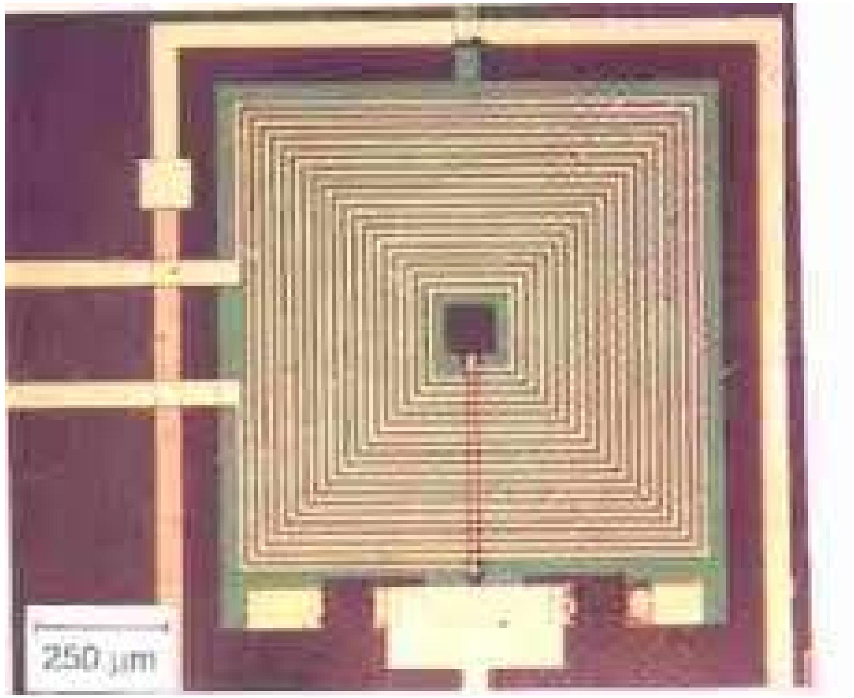
LTS

A central device in Superconductive Electronics:

SQUID

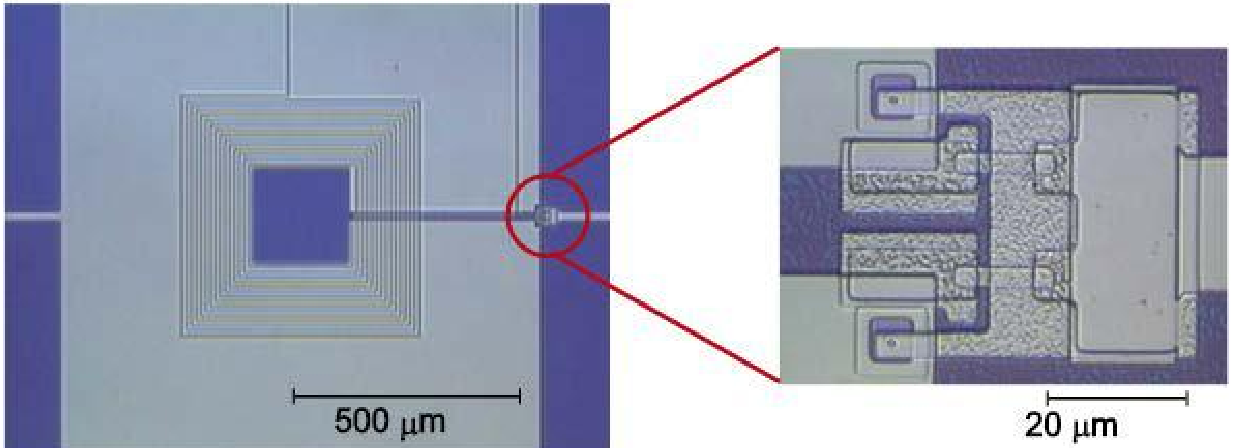
You can read everything about it in:



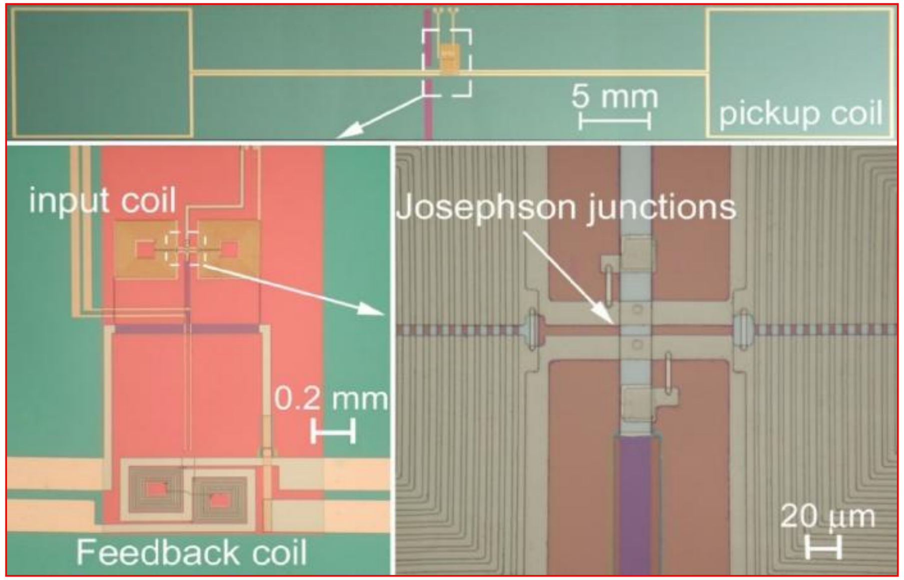


Photograph of typical DC SQUID sensor based on the Ketchen-Joycox (IBM) design.

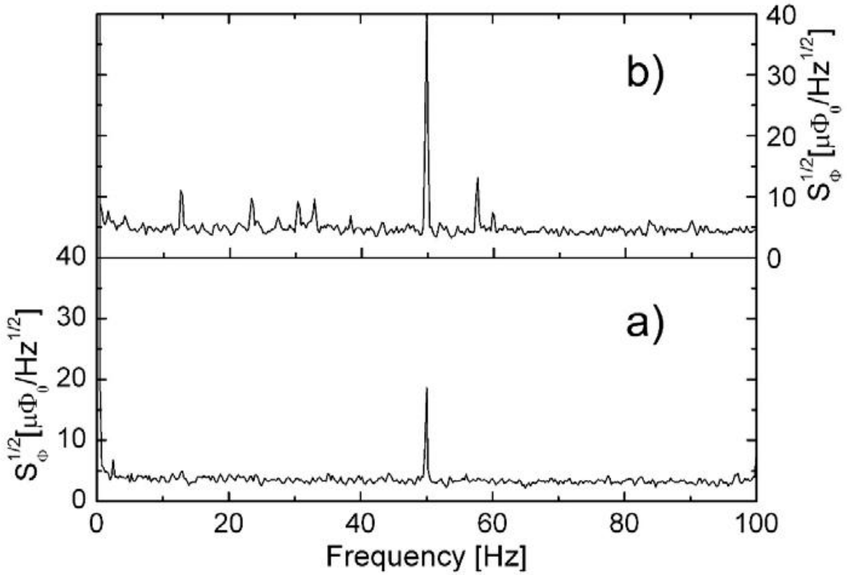
Planar dc-SQUID



SQUID with input coil   Josephson junctions



Integrated planar SQUID gradiometer with baseline length of 50 mm.

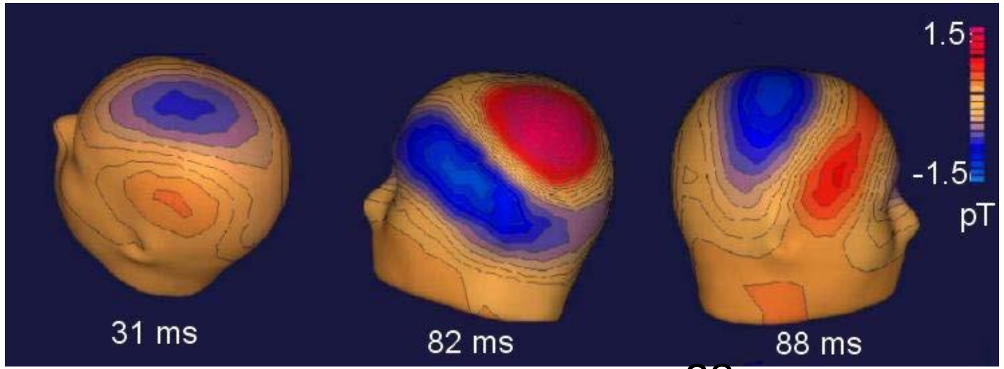


Spectral densities of the magnetic flux noise at T = 4.2 K :
(a) planar SQUID gradiometer
(b) SQUID magnetometer
Magnetic field noise: 3.0 fT/√Hz
Gradient spectral noise: 0.6 fT/(cm· √Hz).

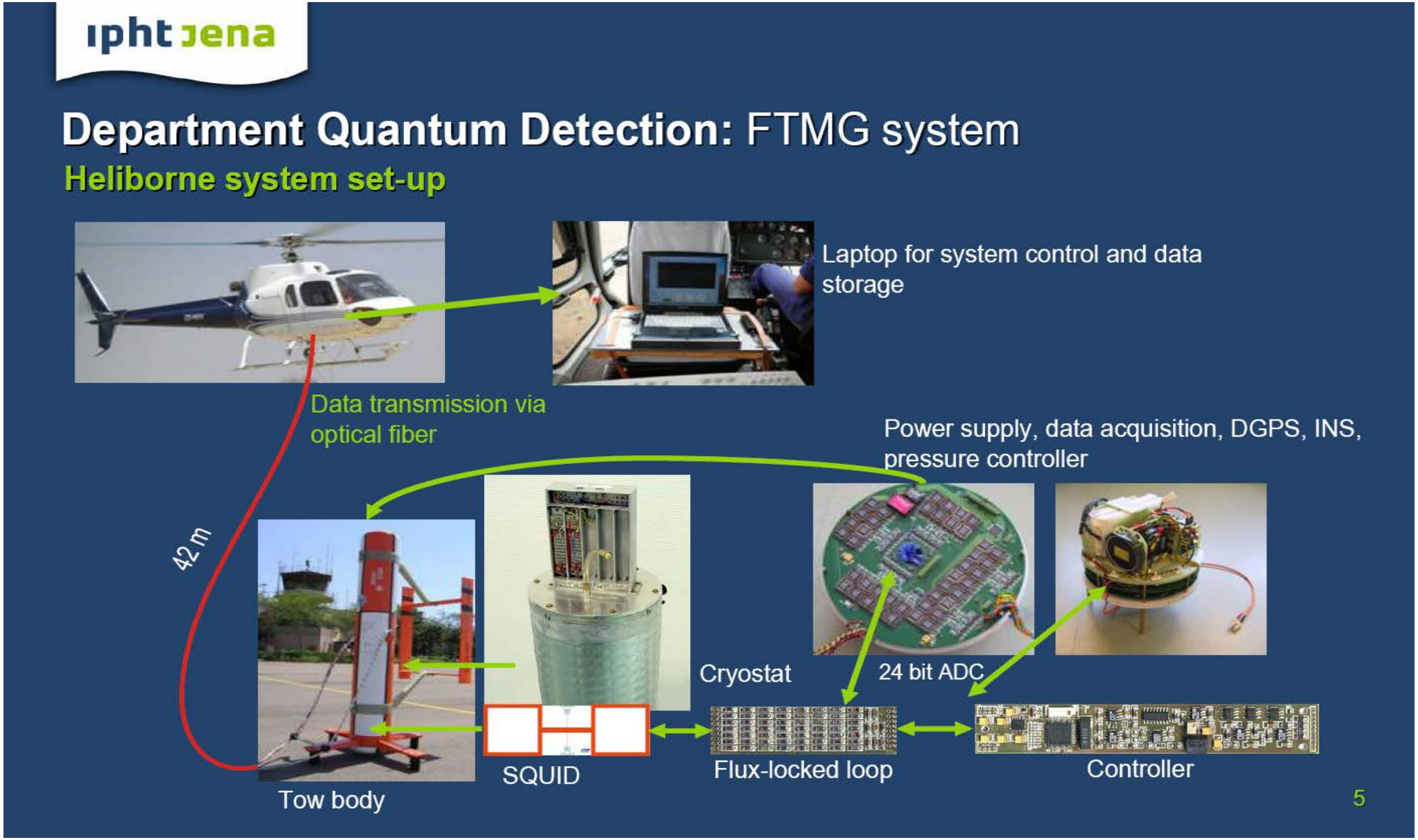
IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), February 2018.
Plenary presentation PL6-INV was given at ISS 2017, December 13-15, 2017, Tokyo, Japan.

Magnetoencephalography with multichannel SQUID systems

Neuromag System



Response to right thumb stimulation (Romani)


ipht jena
Department Quantum Detection: FTMG system
Heliborne system set-up
Laptop for system control and data storage
Data transmission via optical fiber
Power supply, data acquisition, DGPS, INS, pressure controller
42 m
Cryostat
24 bit ADC
SQUID
Flux-locked loop
Controller
Tow body
5

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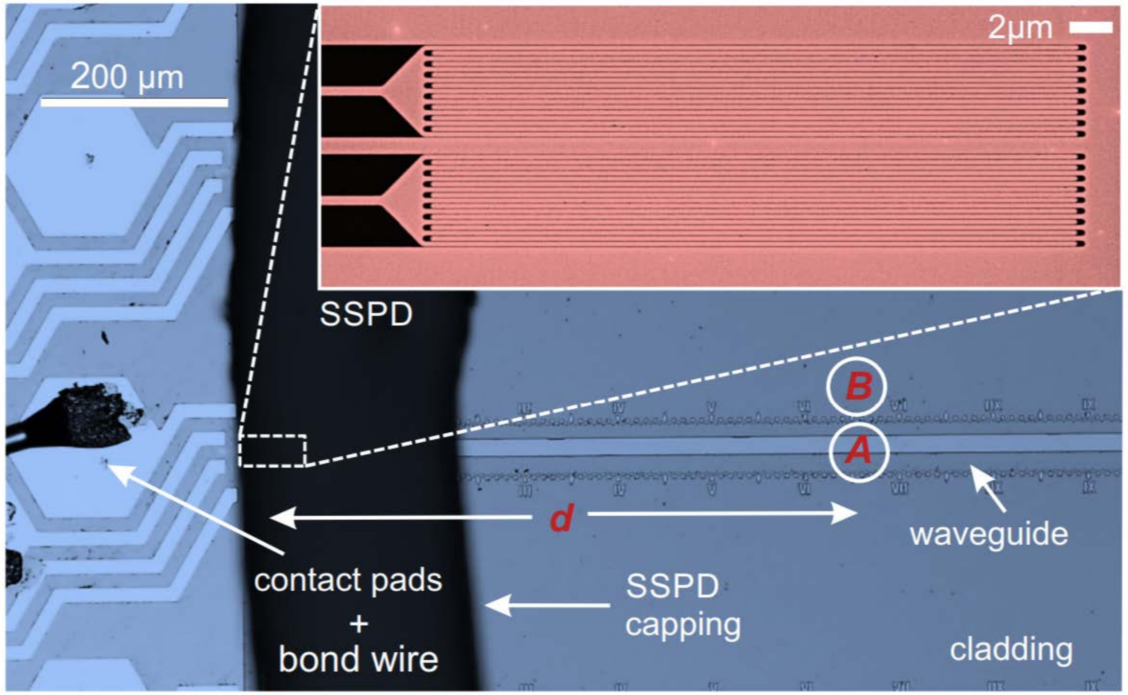
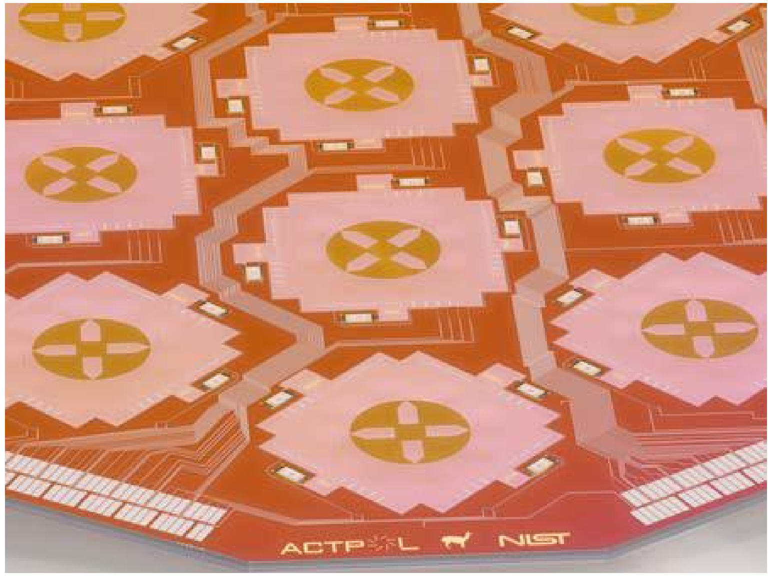
Sensors

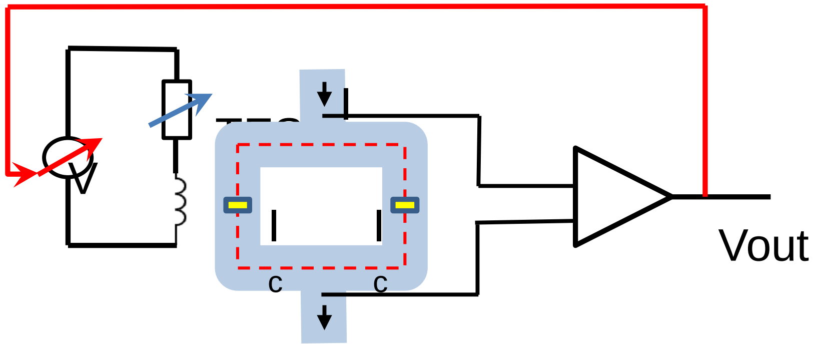
- Transition Edge Detector (TES)
- Superconducting Single Photon Detector (SSPD)



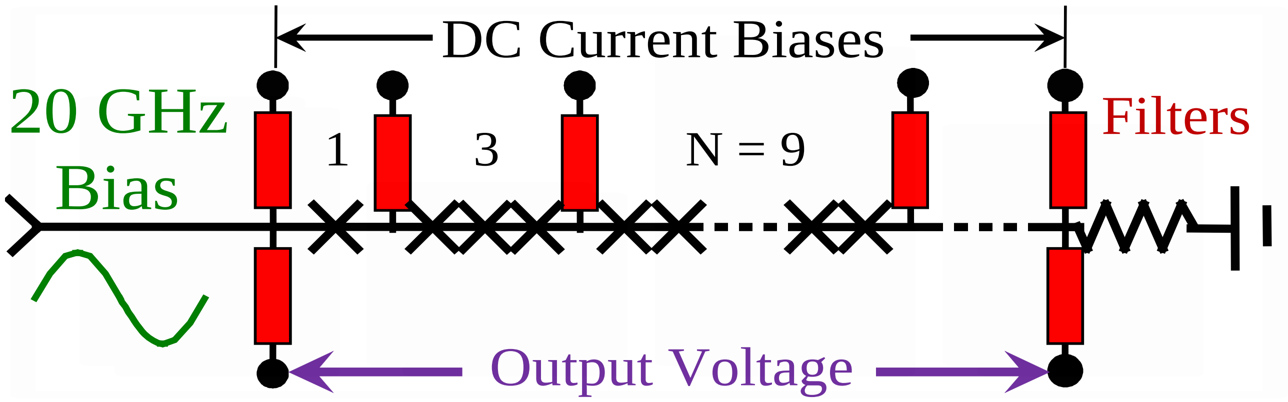
M. Kaniber, F. Flassig, G. Reithmaier, R. Gross, and J. J. Finley, TU München

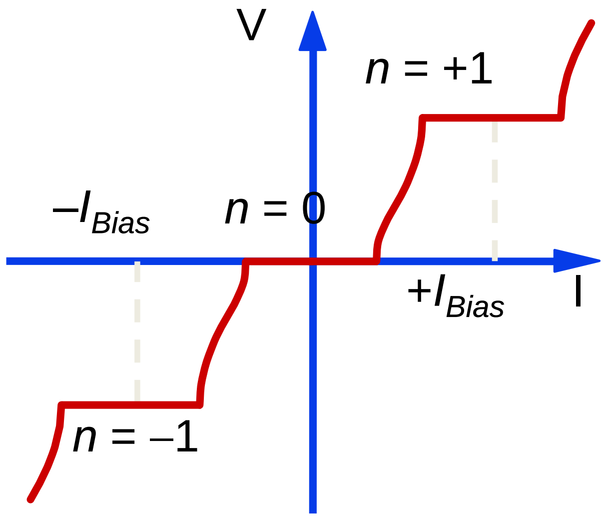


NIST Boulder



Programmable Josephson Voltage Standard (DAC)





Individual bits are switched via the dc current bias.

$$V_{Array} = nN \frac{h}{2e} f$$

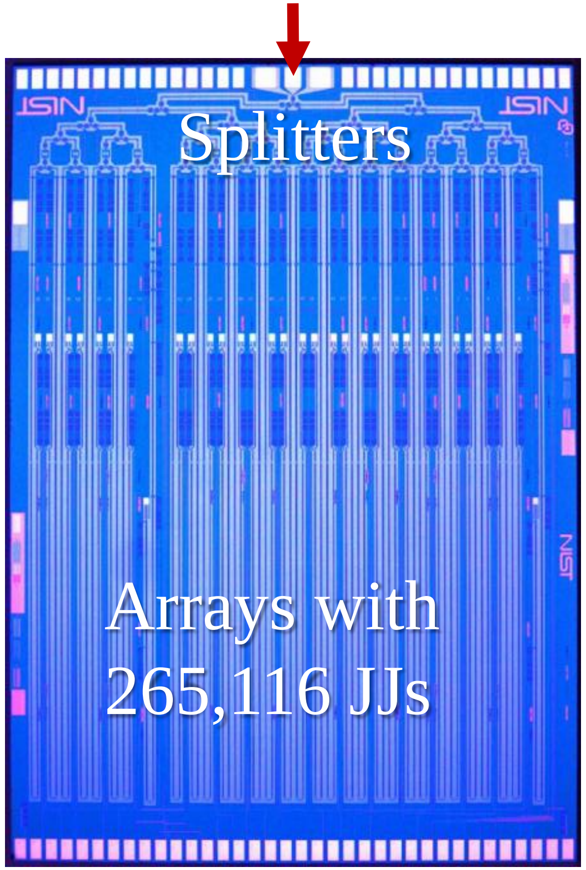
(First shown by Hamilton, Burroughs and Kautz in 1995)

Fabrication & Design of Superconducting Circuits

- Boulder Micro Fabrication Facility
- Superconducting integrated circuits
  - Uniform junctions, barrier materials
  - Power dissipation
- Microwave circuit design
  - Lumped element inductors & capacitors, power splitters, coplanar waveguides
  - Simulation & modelling

(12 x 17) mm^2 10 V PJVS Chip

Microwave Input



DC Input/Output Pads

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Japanese LTS device national projects and ISTEC

ISTEC 1988 → 1992 → LTS device ISTEC Tsukuba → 1997 → 2001

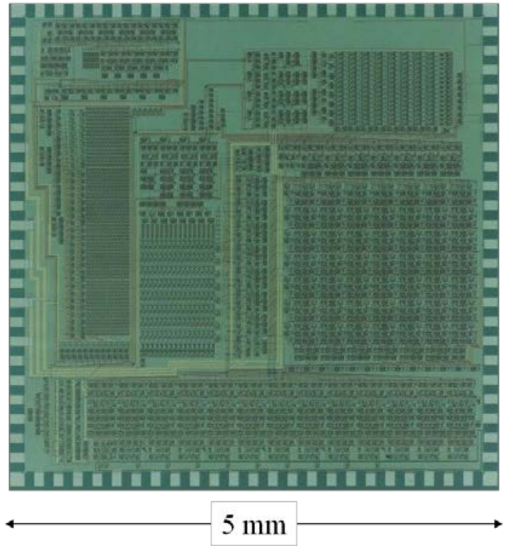
HTS device

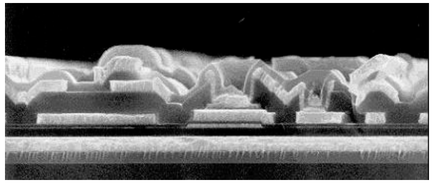
METI
Scientific computing system
81' – 91'

NEDO
JJ hybrid system
95' -97'

MEXT
Information processing by SFQ
97' -01'

Basic technology of LTS devices
- Latching circuits
- Nb 3-layer process (NEC)

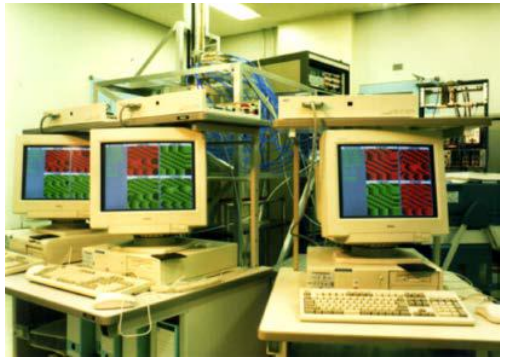




8 bit microprocessor
770MHz
operation (Fijitsu)

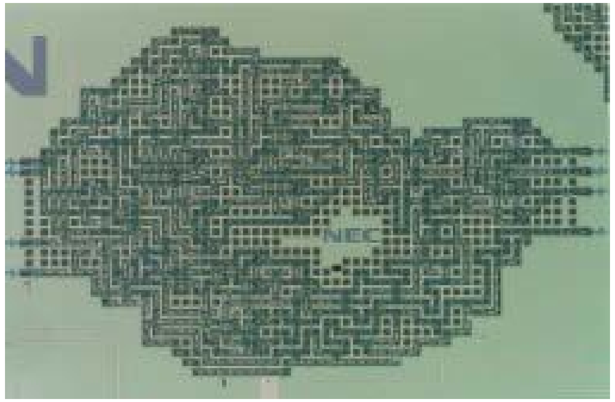
Compilation of latching circuits
- 100 Mbps I/O

Ring network demo.
with 2 GHz operation (NEC)



Basic technology of SFQ circuits
- Design technology
- Start of cell base design
- Start of SFQ fabrication

2×2 switch (NEC)



Japanese LTS device national projects and ISTEC

2002 — 2006 — 2011

NEDO
SC network devices
02' – 06'

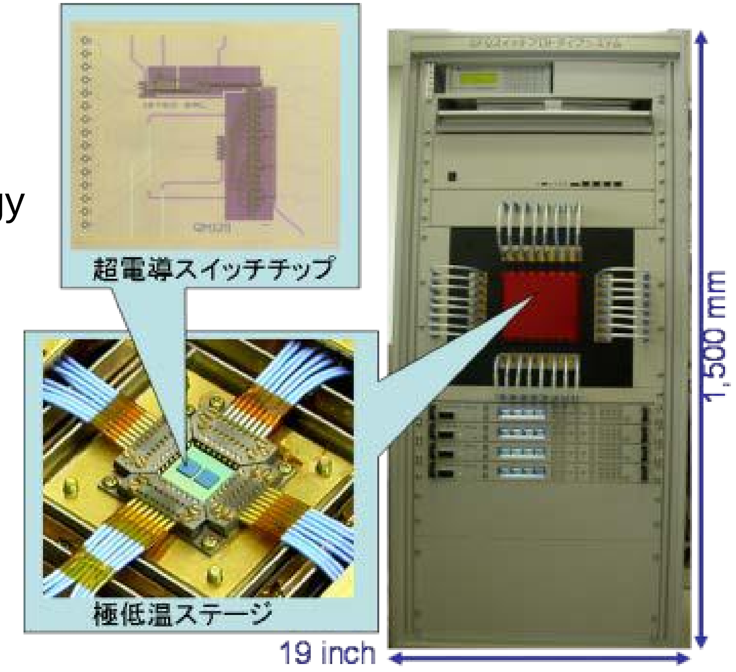
NEDO
Next generation network devices
07' – 11'

SFQ development and packaging technology

- Planarized Nb 6-layer device
- SFQ cell library
- SFQ automatic design system
- Wide band packaging technology with cryo-cooler (10Gb/s)

Result example

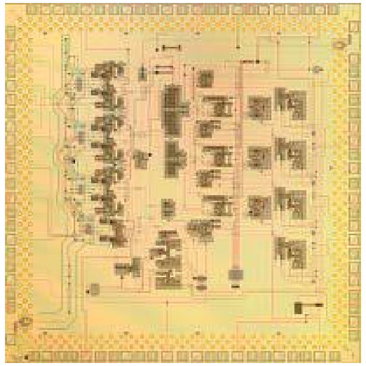
- SFQ processer with 21 GHz operation (ISTEC, Nagoya U., YNU)
- Video transfer demonstration by SFQ 4×4 switch (ISTEC)

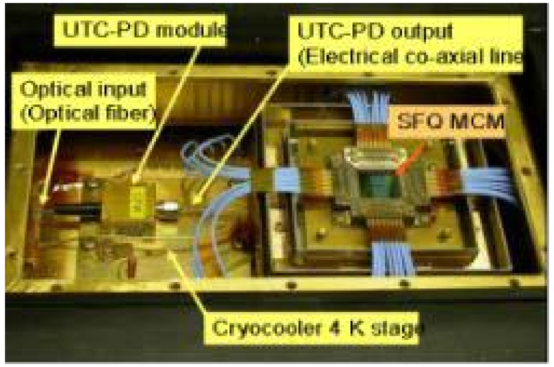


Development toward SFQ small system

- Development of SFQ A/D converter
- Packaging technology for SFQ circuits

Result example
50GS/s SFQ A/D converter (ISTEC)
40 Gb/s optical input to SFQ circuits (ISTEC)





Japanese LTS device national projects and ISTEC

2006 — 2011

JST/CREST
RDP processor
06' – 11'

SFQ circuits by Nb 9-layer process and SFQ speed-up

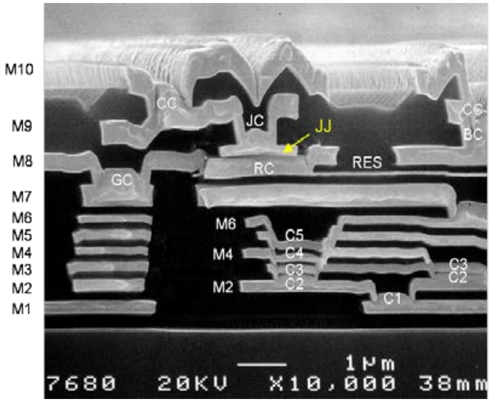
- Construction of Nb 9-layer process
- SFQ cell library for the Nb 9-layer process
- High-speed SFQ processor using the Nb 9-layer process

Starting from 2008:

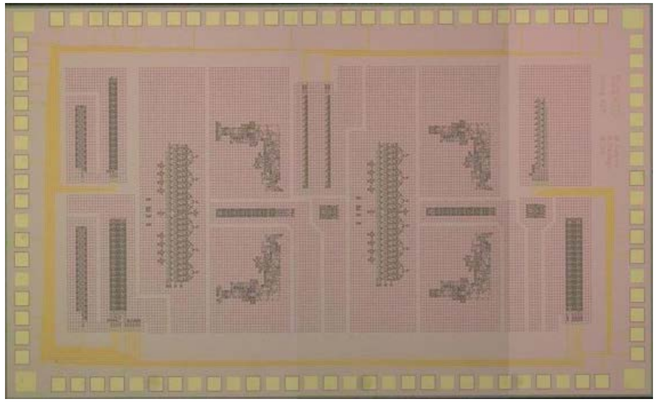
Cooperation between

ISTEC and AIST

Cross-section of Nb 9-layer device (ISTEC)



50GHz SFQ processor (ISTEC, Nagoya U., YNU, Kyoto U.)



LTS device developments AIST and ISTEC

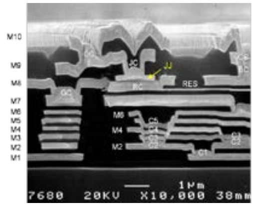
2008 — Collaboration start

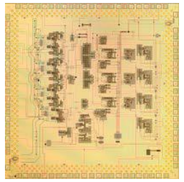
2012 — CRAVITY establishment

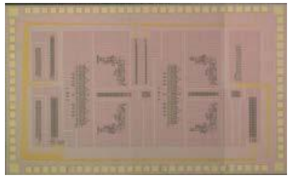
2013 — AIST/ISTEC unification

2017

ISTEC

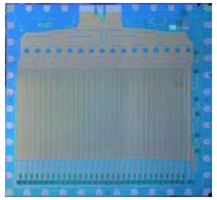

Nb 9-layer device

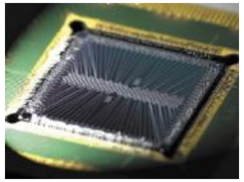

SFQ A/D converter


SFQ RDP

AIST

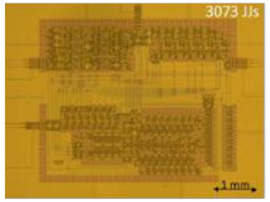
10 V programmable voltage standard



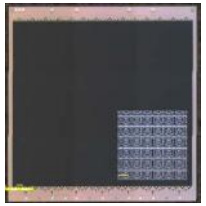

100-pixels STJ array

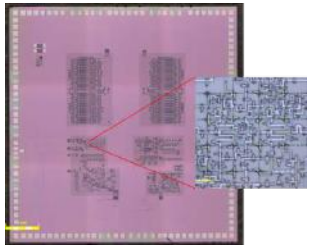
AIST-CRAVITY

Digital devices



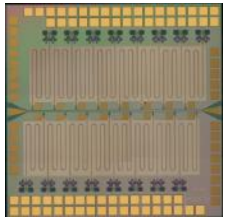
100 GHz SFQ processor

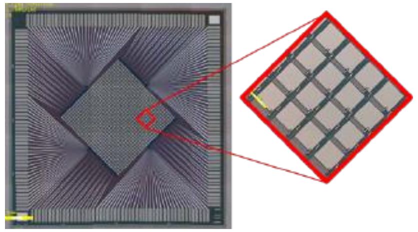

100k gate AQFP

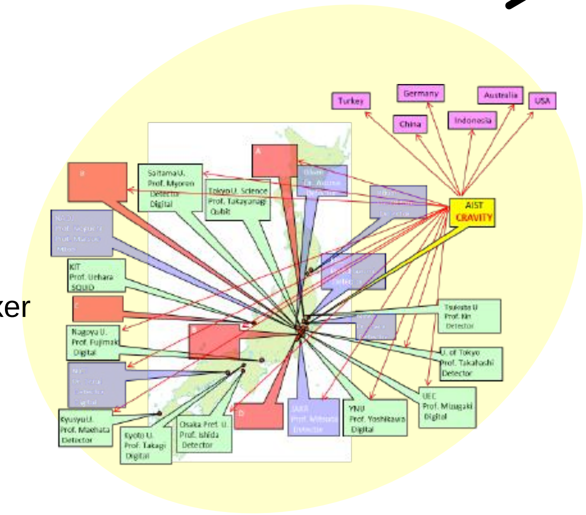

SFQ microprocessor with memory


SFQ-SSPD monolithic device

Analog devices


Microwave SQUID multiplexer

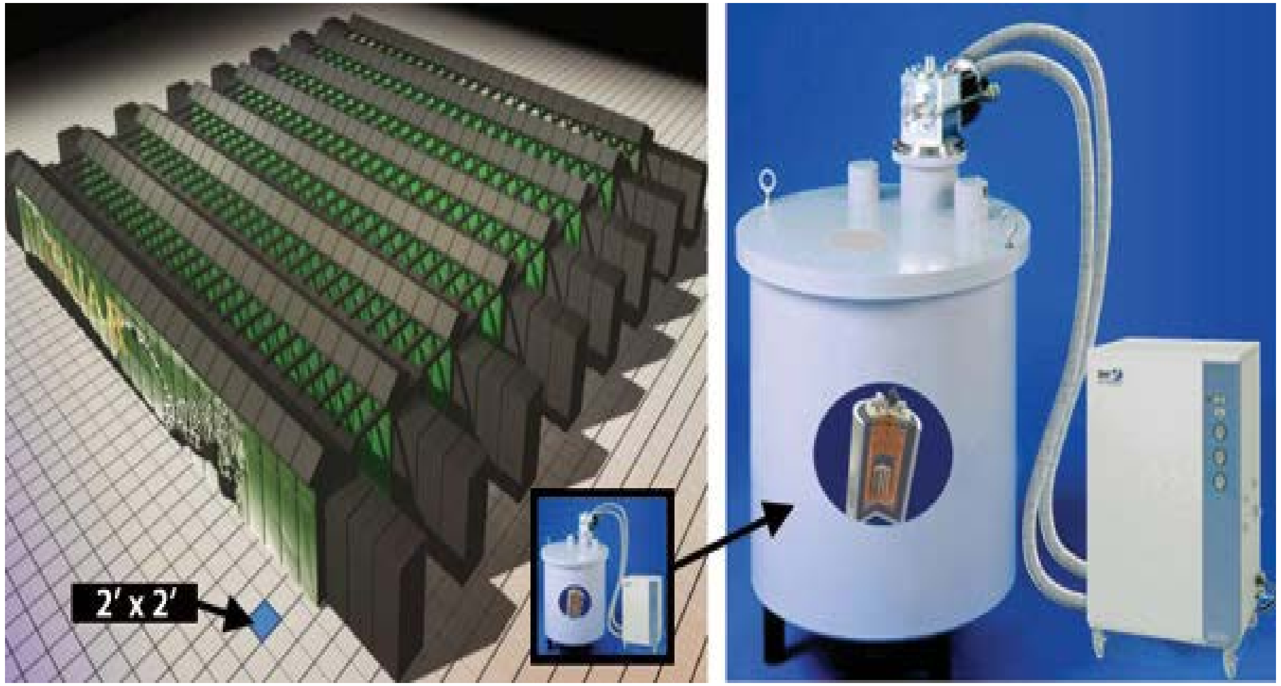

3D-1024 pixels STJ array



Supply destinations of CRAVITY devices

CRAVITY: Clean room for analog-digital superconductivity

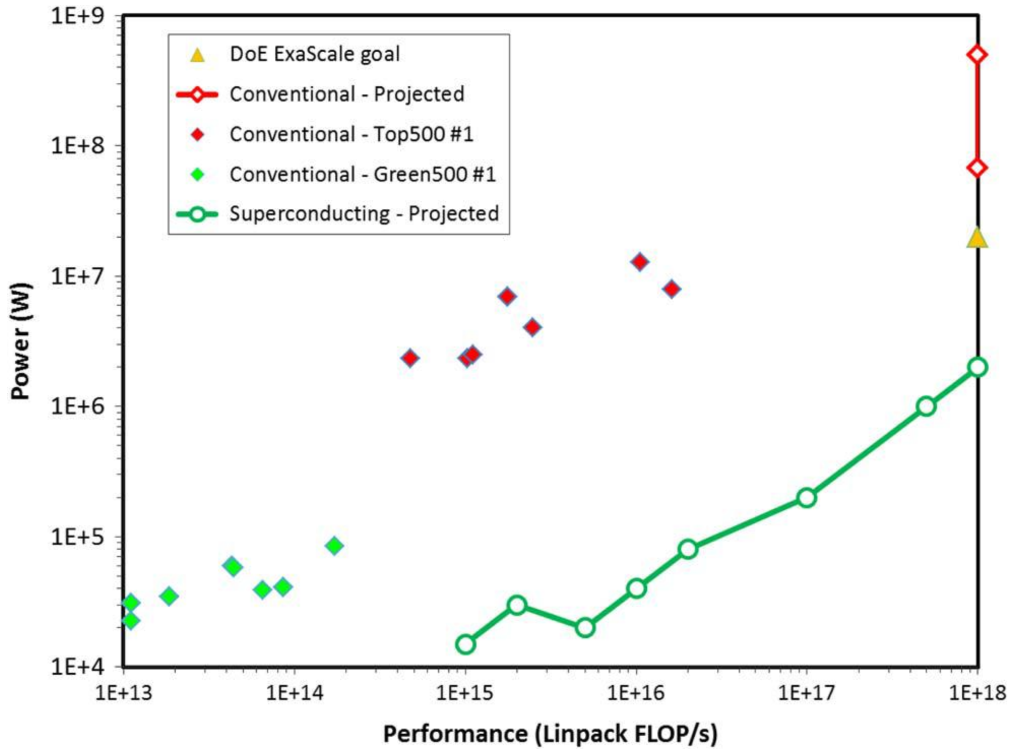
Supercomputer Semiconductor -> Superconductor C3-Project



The Jaguar XT5 supercomputer at Oak Ridge National Laboratory (on left) and the conceptual superconducting supercomputer (on right) both perform at 1.76 petaflops, but the Jaguar XT5 consumes over 7 MW; whereas, the superconducting one consumes 25 kW. (Jaguar XT5 image credit: Cray Inc.)

From Marc A. Manheimer in “The Next Wave, Vol. 20, No. 2 (2013)”

Power Consumption of Supercomputers => C3-Project



Replace RSFQ logic with energy-efficient logic like:

RQL (Northrop Grumman),

ERFSQ/eFSQ (Hypres)

Very low power alternative:

Adiabatic Quantum Flux Parametron AQFP

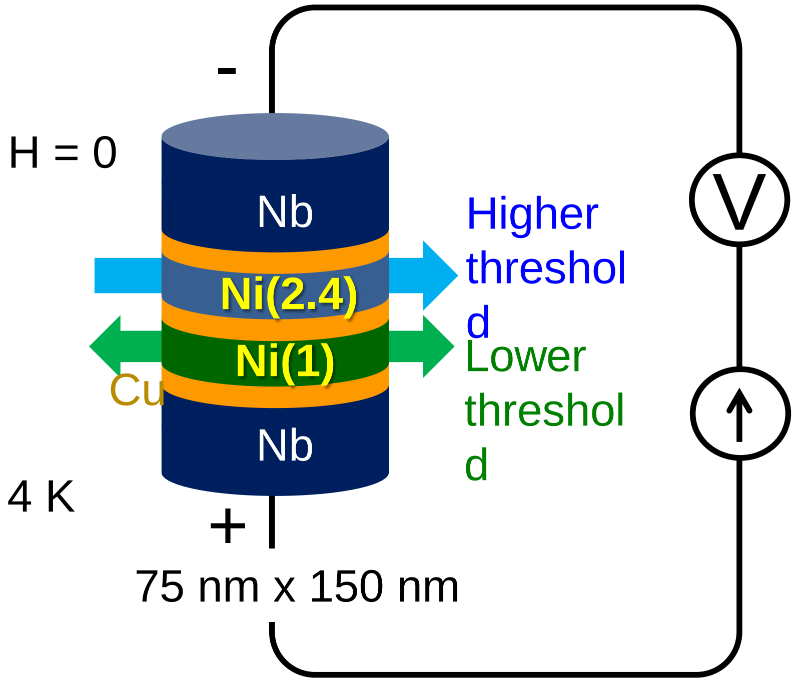
(e.g. Yokohama National University)

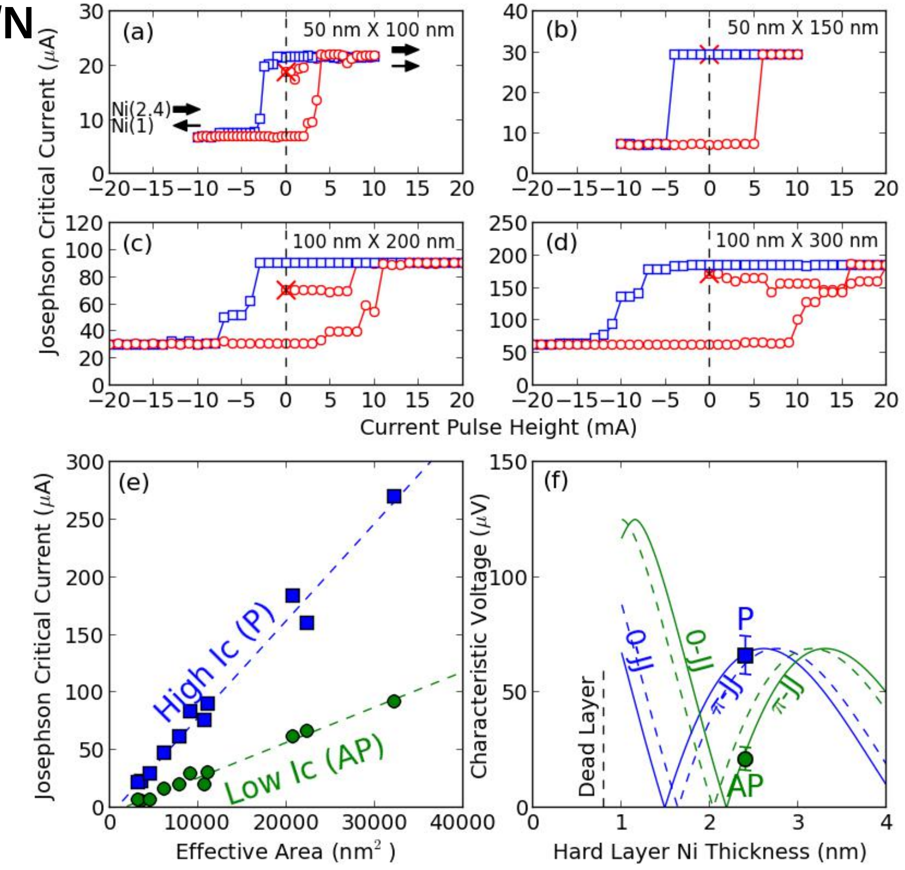
D. Scott Holmes, Andrew L. Ripple, and Marc A. Manheimer, IEEE Transactions On Applied Superconductivity, **23**, 1701610 (2013)

Most urgent problem: Superconducting Memory

Nanopillar Hybrid JJs

Current-induced switching (Ni/Cu/N





NIST: Baek et al. Nat Commun 2014

Thinner layer as FL:
Regular STT effect

Future

- Combination of Qubits with Superconductive Readout (like DWave Co.)
- Secure transmission over long distances
- Storage Elements (magnetic JJs or nano-loops)
- Scaling!!!
- Digital: Fast and Low Energy (Low Power SFQ and Reversible Computing)
- Neuromorphic circuits with superconductors

Future

HTc Superconductive Electronics

-> NO widespread applications with LTS!!

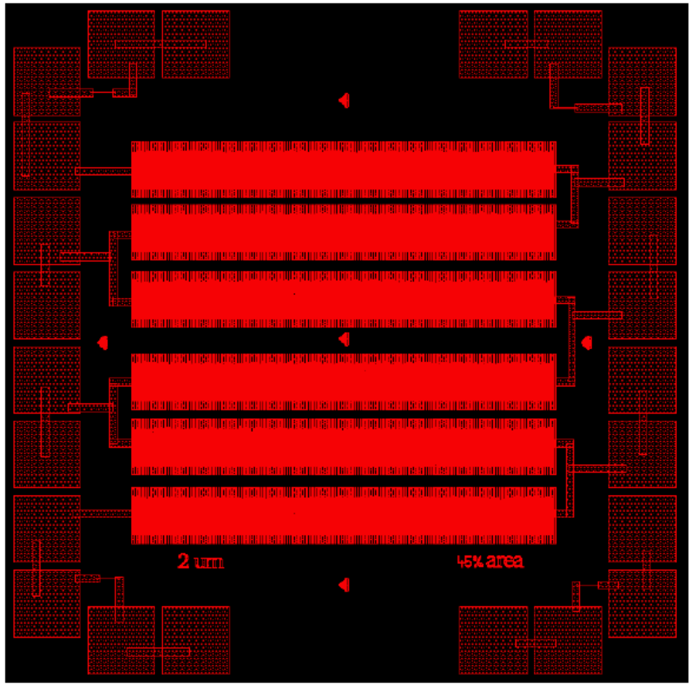
-> multilayer thin film techniques

-> reproducible junction technology

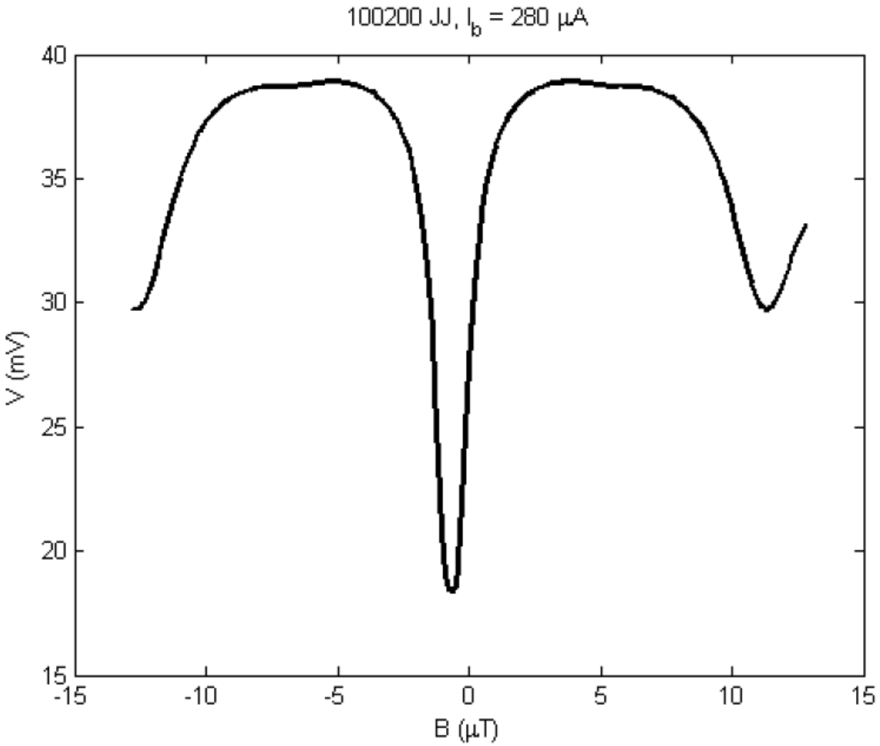
-> needs (big) investment in fabrication technology

Largest SQIF array with SEJs, *N*=100,200
Best sensitivity to date: V_B = 23,000 V/T

Array Fabrication:
J Du, J Y Lazar, S K H Lam, E Mitchell and C P Foley
SUST 27 (2014) 095005



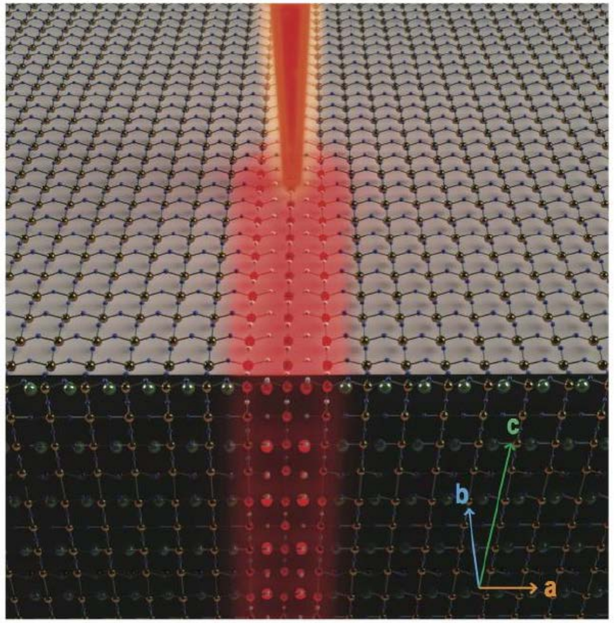
- 100200 junctions
- 45% spread area
- β_L ~0.42 when I_c = 20 μA
- R_N ~50 Ω



- I_b = 280 μA
- Voltage modulation ~20.5 mV
- Sensitivity ~**23,000 V/T**

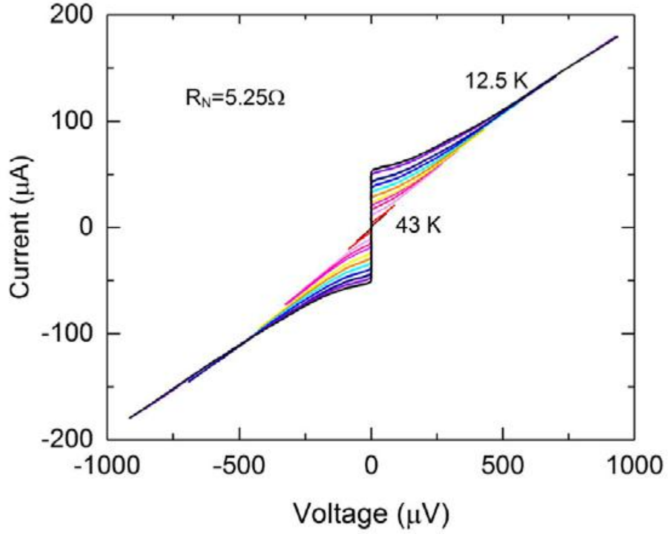
He ion-damage junctions

Maskless direct-write ion implantation



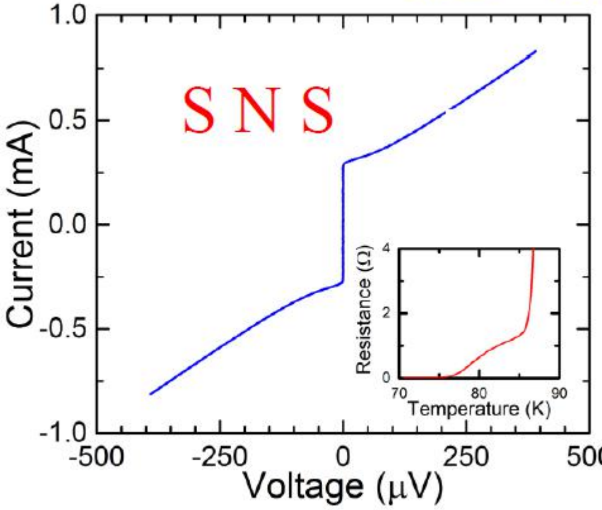
Implantation of a YBCO crystal

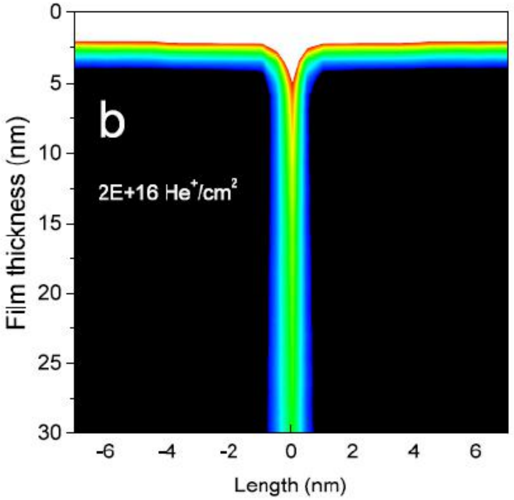
Carl Zeiss Orion Nanofab: He-ion 35 keV 0.5 nm



S. A. Cybart et al.,
Nature Nanotechnology **10**. p 598, 2015

$2x10^{16}$ ions/cm^2





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Future

➡ **We need to make the step from scientific to engineering operation.**

Future

Without technology advances and the step from scientific to engineering operation:

Superconductive Electronics will stagnate.

Future

With technology advances and the step from scientific to engineering operation:

Superconductive Electronics will flower!!

Happy 30th anniversary to the ISS!