



Large-scale Superconductor Electronics: Opportunities and Challenges

*D. Scott Holmes, IEEE IRDS, USC DISCoVER
2025-10-29 QUEST-SSV, Yokohama, Japan*



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Abstract: Technology roadmaps for superconductor electronics (SCE) and quantum computing are under development within the framework of the International Roadmap for Devices and Systems (IRDS). Application needs are drivers for IRDS roadmaps. Most important for the future of superconductor electronics are large-scale applications requiring more than one million switching devices per chip. Potential large-scale applications are evaluated in areas including digital signal processing, quantum computing, neuromorphic computing, and digital computing. Technology improvements required to meet the expected needs are assessed along with time scales for development.

Speaker bio: Dr. D. Scott Holmes chairs the Cryogenic Electronics and Quantum Information Processing (CEQIP) International Focus Team (IFT) for the International Roadmap for Devices and Systems (IRDS). He previously supported the Intelligence Advanced Research Projects Agency (IARPA), including the SuperTools program to develop electronic design automation (EDA) tools for superconductor circuits and the Cryogenic Computing Complexity (C3) program that developed technologies for energy-efficient superconductor computing. He served as a DARPA program manager in the Microsystems Technology Office (MTO). Earlier career experience includes large-scale superconductor systems development at what is now the Air Force Research Laboratory, sensor and measurement system development at Lake Shore Cryotronics, and a decade as a Learning Strategist with an international clientele. Areas of interest include superconductor electronics and novel computing technologies. Professionally, Holmes is a member of the IEEE Council on Superconductivity as a representative of the Electron Device Society. Holmes received a BSME from MIT and two master's degrees and a joint Ph.D. from the University of Wisconsin–Madison.

► Note: Post-presentation version





IRDS Technology Roadmaps:

Cryogenic Electronics and Quantum Information Processing (CEQIP)

2023 IRDS CEQIP Report + 2025 Update

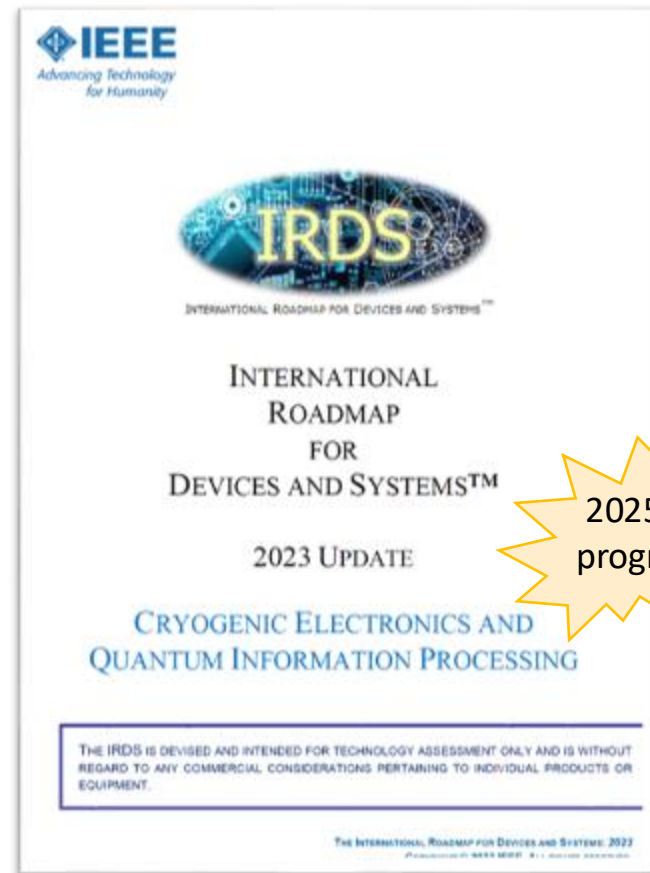




IRDS CEQIP Report

2023 Update and 2025 Update (2024 skipped)

- IRDS IFT Cross-team and Collaborative Alignments
- Coverage
 - Superconductor Electronics (SCE)
 - Roadmap (partial)
 - Cryogenic Semiconductor Electronics
 - Quantum Information Processing (QIP)
 - **2023**: First Roadmap for superconducting QC
 - 2026(?): Roadmap development for ion trap QC
- Summary slides by area:
 - Difficult Challenges: Near- and Long-term
 - Technology Assessment Updates
 - New Technology Requirements
 - Breakthroughs in Technology, Research
- Recommendations and Plans
- Appendix: Team Members



Superconductor Digital Logic Families

2025 Table CEQIP-4

Name	Power	SFQ	Devices per amp	Static Power	Devices	Transformers	Clocked Gates	Switch count
RSFQ : rapid single flux quantum	I dc –	1	1.9E+04	1.3E-07	JLR		■	2.5E+04
LR-RSFQ : inductor-resistor RSFQ	I dc –	1	5.7E+04	4.4E-09	JLR		■	3.6E+01
LV-RSFQ : low-voltage RSFQ	I dc –	1	5.7E+04	4.4E-09	JLR		■	4.9E+03
ERSFQ : energy-efficient RSFQ	I dc –	1	9.5E+03	0 *	JLR		■	6.8E+03
eSFQ : efficient SFQ	I dc –	1	1.9E+04	0	JLR		■	2.6E+03
Self-timed SFQ	I dc –	1	1.9E+04	1.3E-07 ±	JLR		□	6.0E+02
DSFQ-LV : dynamic SFQ, low volt.	I dc –	1	2.9E+04	1.7E-08 ±	JLR		□	2.3E+01
TSFQ : temporal SFQ	I dc –	1	5.7E+04	4.4E-08 ±	JLR		□	
xSFQ : alternating SFQ	I dc –	2	2.9E+04	8.8E-08 ±	JLR		□	
HFQ-LV : half flux quantum (0-0- π)	I dc –	0.5	4.8E+05	1.1E-09	JLP		■	1.6E+01
HFQ : half flux quantum (all-JJ: 0, π)	I dc –	0.5	8.5E+04	5.9E-09	JLP		■	
nTron : nanowire cryotron	I dc –	-	6.5E+03		LN		■	3.2E+01
hTron : heater-cryotron nanowire	I dc –	-	>1E+9		LNR		■	1.6E+01
FPL : fast phase logic	I dc – I ac ~	1 1	? >1E+9	? ?	JLP JLPT	□ ■	■ ■	
SSBF : sustainable ballistic fluxon	I dc – I ac ~	1 1	? >1E+9	? ?	JL JLT	□ ■	■ – □	
SFQ-AC : AC-powered SFQ	I ac ~	1	>1E+8		JLRT	P	■	8.1E+05
RQL : reciprocal quantum logic	I ac ~	2	>1E+8		JLRT	LP	□	7.3E+04
PML : phase mode logic	I ac ~	1	>1E+8		JLRT	LP	□	
PCL : pulse conserving logic	I ac ~	1	>1E+8		CJLRT	L	□	
AQFP : adiabatic quantum flux param.	I ac ~	-	>1E+8		JLRT	LP	■	2.1E+04
RQFP : reversible QFP	I ac ~	-	>1E+8		JLRT	LP	■	2.8E+01
QPSJ : quantum phase slip junctions	V dc –	-	>1E+9	0	CQ		■	2.0E+00

Other metrics?

- Area
- Logic depth
- JJ per gate
- Scalability

▶ Searching for a winning combination



Roadmap: Fab for Superconductor Electronics (SCE)

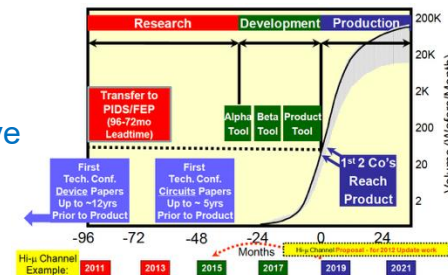
2025 update in progress

- 2025 Roadmaps
 - Interconnect (CEQIP-5)
 - Digital circuits (CEQIP-19)
 - Superconductor MCM (-20)
- Future
 - Update needed!
 - Move from first availability (IRDS standard) to second commercial producer?
 - Add potential solutions and timelines

Year	2024	2025	2026	2027	2028	2029	2030
Digital SCE Fabrication							
"Node Range" label (nm)	"150"	"150"	"150"	"150"	"90"	"90"	"90"
Substrate material, maximum size (mm)	Si, 200	Si, 200	Si, 200	Si, 200	Si, 300	Si, 300	Si, 300
Wiring							
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	10	10	10	10	12	12	12
Linewidth, minimum (nm)	150	150	150	150	90	90	90
I _c , minimum (μA)	100, 580	100, 580	100, 580	100, 580	50, 290	50, 290	50, 290
Junctions, Switching							
Junction materials	Al/AIO _x	Al/AIO _x	Al/AIO _x	Al/AIO _x	Al/AIO _x	Al/AIO _x	Al/AIO _x
Junction layers	2	2	2	2	2	2	2
Junction critical current densities, J _c (μA/μm ²)	100, 600	100, 600	100, 600	100, 600	100, 600	100, 600	100, 600
Minimum junction diameter (nm)	350	350	350	350	250	250	250
Minimum junction critical current, I _c (μA)	10, 58	10, 58	10, 58	10, 58	5, 29	5, 29	5, 29
Killer defect density per layer (1/cm ²)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
J _c wafer-to-wafer variation	3%	3%	3%	3%	3%	3%	3%
Maximum relative spread (σ/I _c) at minimum I _c	3%	3%	3%	3%	3%	3%	3%

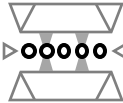
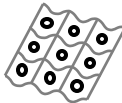
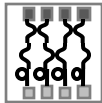


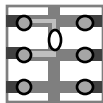

2025 Table CEQIP-19 (preliminary)

ITRS 2011 Executive Summary, Fig. 3





Quantum computing: Still a race with several contenders

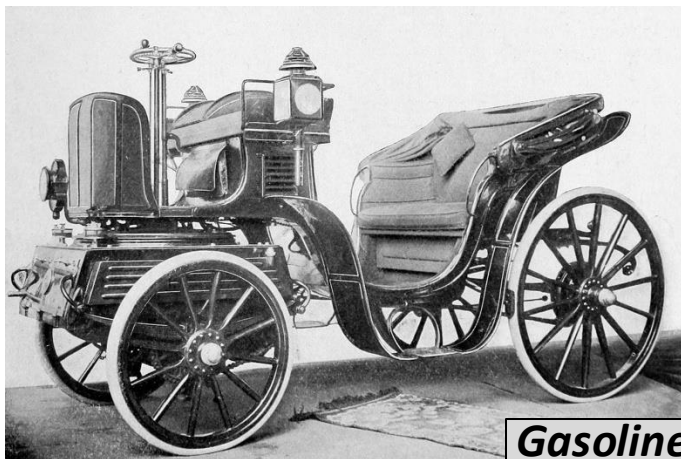
	Natural qubits			Synthetic qubits			
Qubit:	 Trapped ion	 Neutral atom	 Photonic	 Superconducting	 Quantum dot	 Topological	 N-V diamond
Basis	Electron spin of ionized atoms	Internal states of atoms trapped in an optical lattice	Optical photons in waveguides	Nonlinear oscillator circuits containing Josephson junctions	Impurity dopants in a semiconductor	Majorana particles in nanowires	Spin state of N atom + vacancy defect in diamond
$E_{transition}$ (= $hf, k_B T$)	1 – 700 THz 50 – 30,000 K	~ 4 MHz ~ 200 μ K	100 – 200 THz 4,800+ K	2 – 10 GHz 0.1 – 0.5 K	10 – 50 GHz 0.5 – 2.5 K	?	300 – 800 THz 15,000+ K
T_{system}	1 – 300 K	4 – 300 K	1 – 300 K	0.01 – 0.05 K	0.1 – 1 K	?	1 – 300 K
Pros	Long lifetime, low gate error	Many qubits, 2D, maybe 3D	Linear optical gates, photonic IC	Fast gates, adjustable, easy fabrication size	High density, CMOS compatible	Lower errors	Room temperature operation?
Cons	Slow gates, vacuum, many lasers	Hard to control individual qubits, noise, high errors	Superconducting single photon detectors	T noise, variability, large size, mK temperatures	T noise, low temperatures, high errors	Device? Magnetic field?	Variability, detector?

System temperatures vary by approach

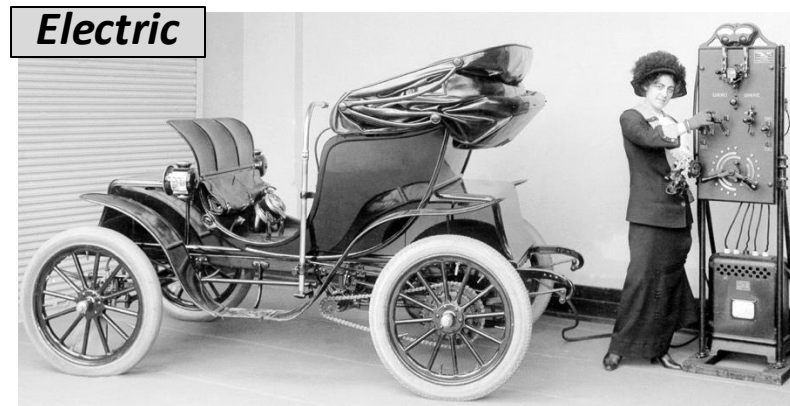


Searching for a winning combination (QC edition)

Automobile analogy, circa 1900



Gasoline



Electric



Steam

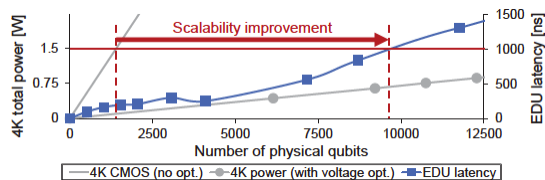
- ▶ The eventual winner was not obvious at the time.



Limits for superconducting qubit control (1)

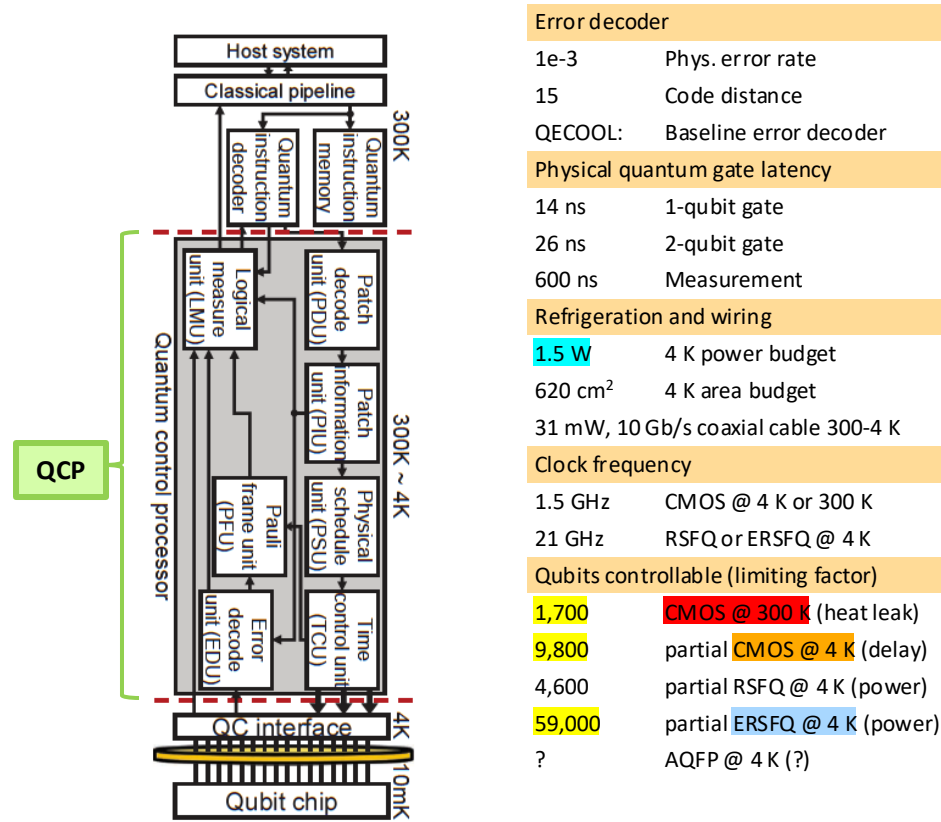
Where are the breakpoints?

- **XQsim**: quantum control processor (**QCP**) simulator (open-source, cross-technology)
- Scalability analysis
 - Maximum number of qubits subject to constraints (delay, power, area)
 - Did not include QC interface



CMOS @ 4 K scalability analysis [1, Fig. 17b]

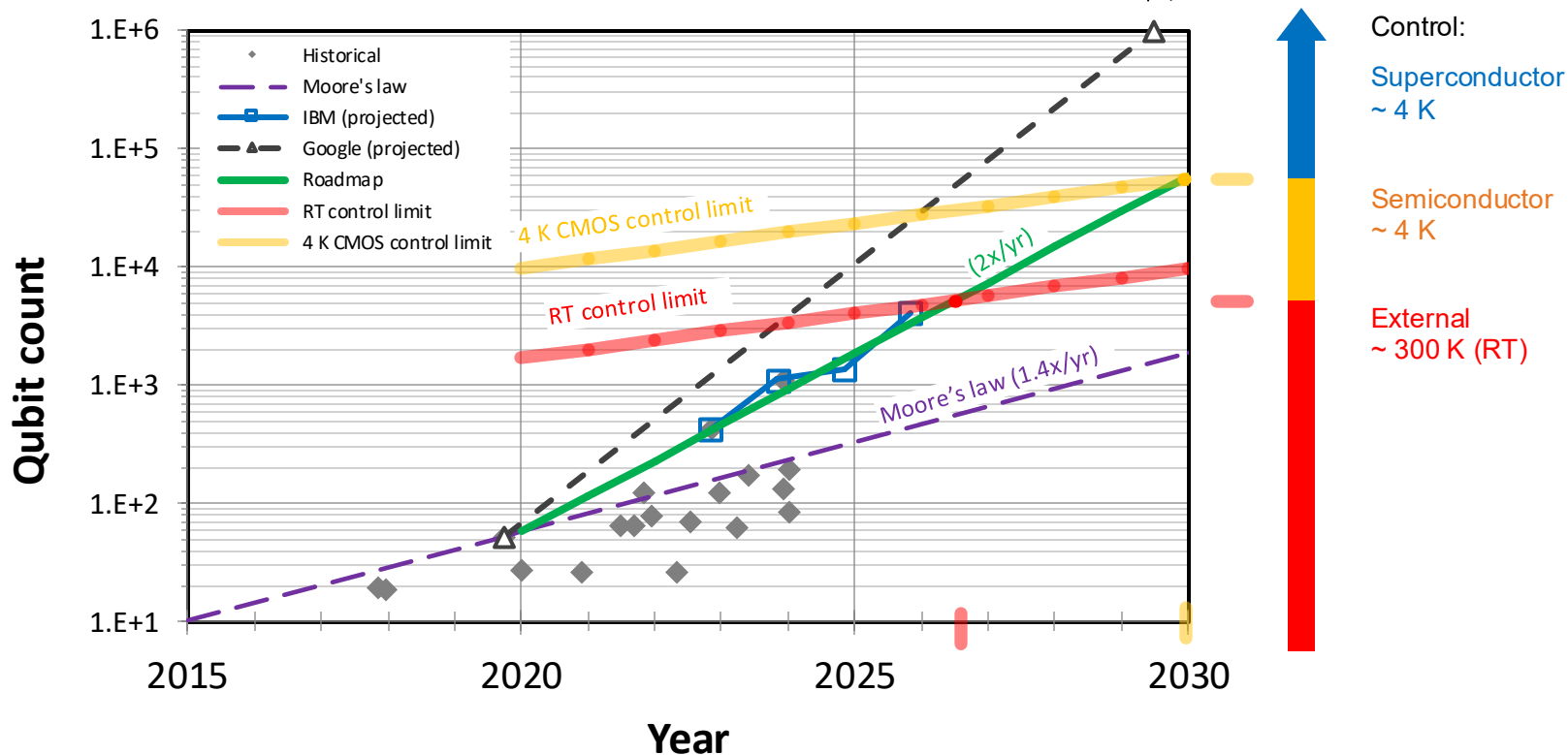
[1] Byun +, "XQsim: modeling cross-technology control processors for 10+K qubit quantum computers," 2022, doi: [10.1145/3470496.3527417](https://doi.org/10.1145/3470496.3527417).



FTQC system overview [1, Fig. 1]



Superconducting Qubit Trends



Historical: 2025 Figure CEQIP-8
 IBM: <https://research.ibm.com/blog/ibm-quantum-roadmap-2025>
 Google: <https://www.cnet.com/tech/computing/quantum-computer-makers-like-their-odds-for-big-progress-soon/>



Superconducting QC Roadmap

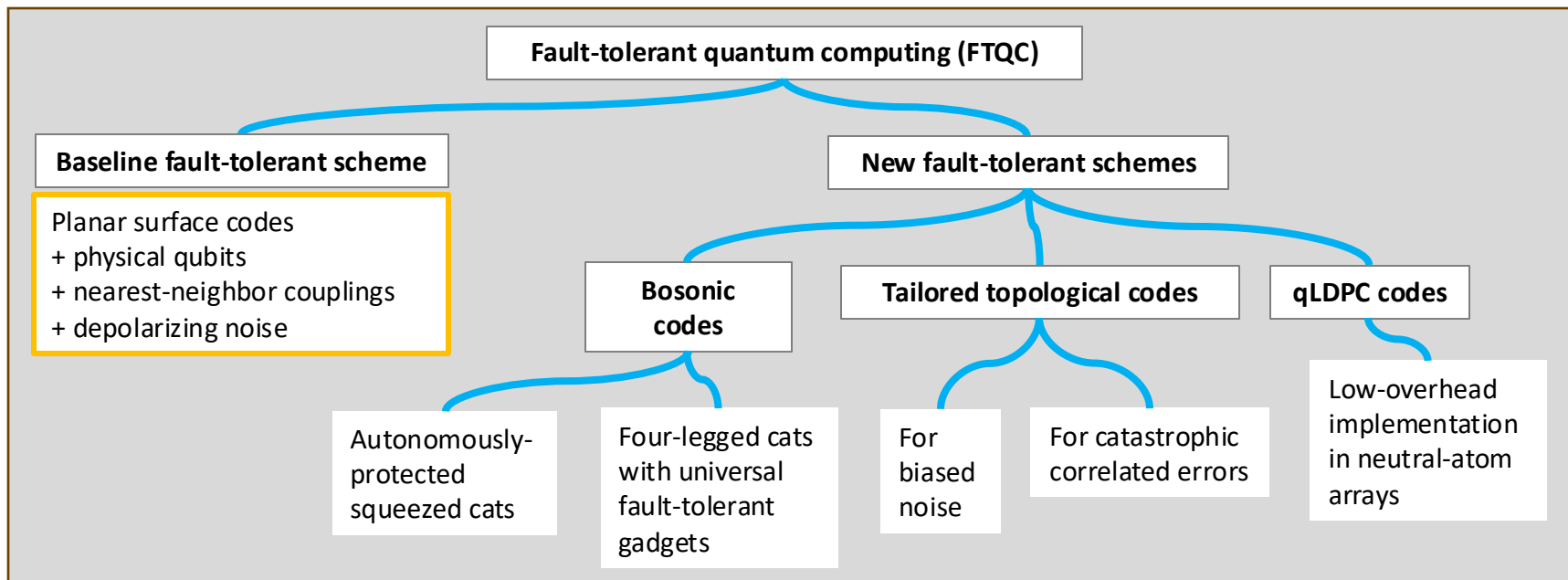
Metric	2022	2024	2026	2028	2030	2032
Qubit growth factor	2	2	2	2	2	2
Qubit count	2.32E+02	9.28E+02	3.71E+03	1.48E+04	5.94E+04	2.38E+05
Qubit type	Transmon	Transmon	Transmon	Transmon	Transmon	Transmon
Coherence time T2* [s]	1.00E-03	2.00E-03	4.00E-03	8.00E-03	1.60E-02	3.20E-02
2-qubit gate time t_2g [s]	2.83E-07	2.00E-07	1.41E-07	1.00E-07	7.07E-08	5.00E-08
Operations to error (T2*/t_2g)	3.54E+03	1.00E+04	2.83E+04	8.00E+04	2.26E+05	6.40E+05
Cycle time [s]	3.54E-06	2.50E-06	1.77E-06	1.25E-06	8.84E-07	6.25E-07
2-qubit gate error rate, median (p_2Q)	5.00E-03	2.50E-03	1.25E-03	6.25E-04	3.13E-04	1.56E-04
Gate depth (1/p_2Q)	2.00E+02	4.00E+02	8.00E+02	1.60E+03	3.20E+03	6.40E+03
Error correction code	Surface	Surface	Surface	Surface	Surface	Surface
Qubits per logical qubit	17	49	161	337	577	881
Logical qubit count (max.)	14	19	23	44	103	270
Logical qubit error rate p_log	2.31E-02	2.53E-03	1.52E-05	5.72E-09	1.34E-13	1.97E-19
Control type, temp. [K]	CMOS, 300	CMOS, 300	CMOS, 300	CMOS, 4	CMOS, 4	SCE, 4
SCE control complexity [JJ]	4.72E+05	1.89E+06	7.55E+06	3.02E+07	1.21E+08	4.83E+08



FTQC: Alternatives to the Surface Code

There is more than one way to achieve fault tolerance!

FTQC approaches [1, Fig. 1.1]



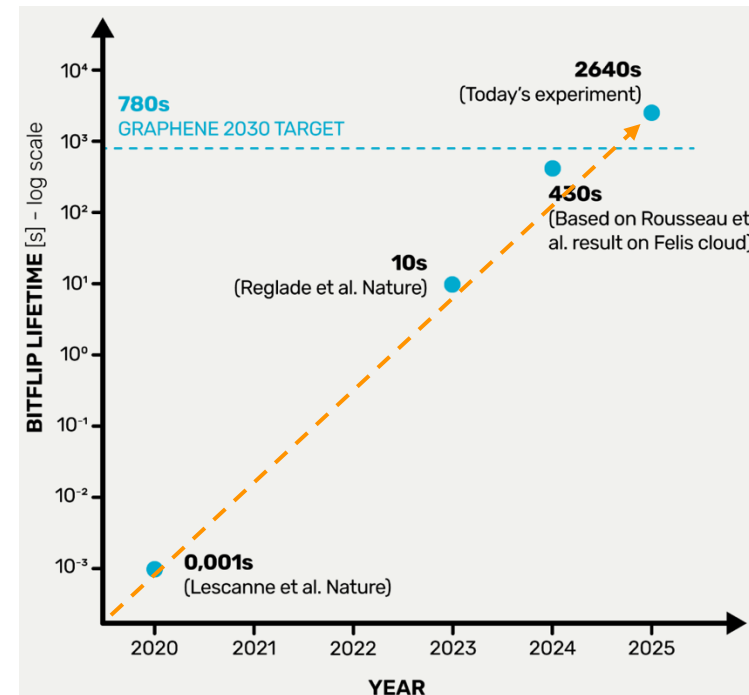
[1] Q. Xu, "Towards Practical Fault-Tolerant Quantum Computing," Ph.D. dissertation, The University of Chicago, Chicago, IL, USA, 2024. doi: [10.6082/uchicago.12363](https://doi.org/10.6082/uchicago.12363).



Superconducting cat qubits are promising

Reducing one error type is significant

- **Bit-flip** lifetime (44 minutes) is much longer than time between cosmic ray impacts
- **Phase-flip** lifetime (420 ns) is short
- One dominant error type
 - enables use of more efficient quantum error correction (QEC) codes,
 - which can greatly reduce the number of physical qubits per logical qubit



S. Jezouin, Alice & Bob, 2025-09-25,

<https://alice-bob.com/blog/just-out-of-the-lab-a-cat-qubit-that-jumps-every-hour/>



SCE Digital Accelerators

Application area 1



Digital accelerators (ASICs)

Favorable for early applications

- Characteristics:
 - Computation intensive
 - Integer arithmetic, few bits
 - Feed-forward data flow (no or few feedback loops)
 - Memory-light: minimal RAM usage (acceptable: moderate sequential access memory)

Application	Ref.	Circuit family	~ JJ count, min.
Sensor readout			1E+2
Array readout (8×8)			1E+4
DSP: digital signal processing			
• FFT (8 b, 64 pt)	1	RSFQ	1E+5
• FIR (256 taps, 16 b)	2	U-SFQ	2E+5
Bitcoin mining	3	RQL	3E+6
QC support (2.4E+5 qubits)	4	ERSFQ	5E+8
Homomorphic encryption	5	RSFQ	1E+9

1. Ono+, 2017, doi: [10.1109/TASC.2017.2667398](https://doi.org/10.1109/TASC.2017.2667398)
2. Gonzalez-Guerrero+, 2022, doi: [10.1145/3503222.3507765](https://doi.org/10.1145/3503222.3507765)
3. Tannu+, 2019, doi: [10.1145/3310273.3321561](https://doi.org/10.1145/3310273.3321561)
4. Byun +, 2022, doi: [10.1145/3470496.3527417](https://doi.org/10.1145/3470496.3527417)
5. Razmkhah+, 2025, doi: [10.48550/arXiv:2508.21265](https://doi.org/10.48550/arXiv:2508.21265)

Large-Scale Digital Computing (LSDC)

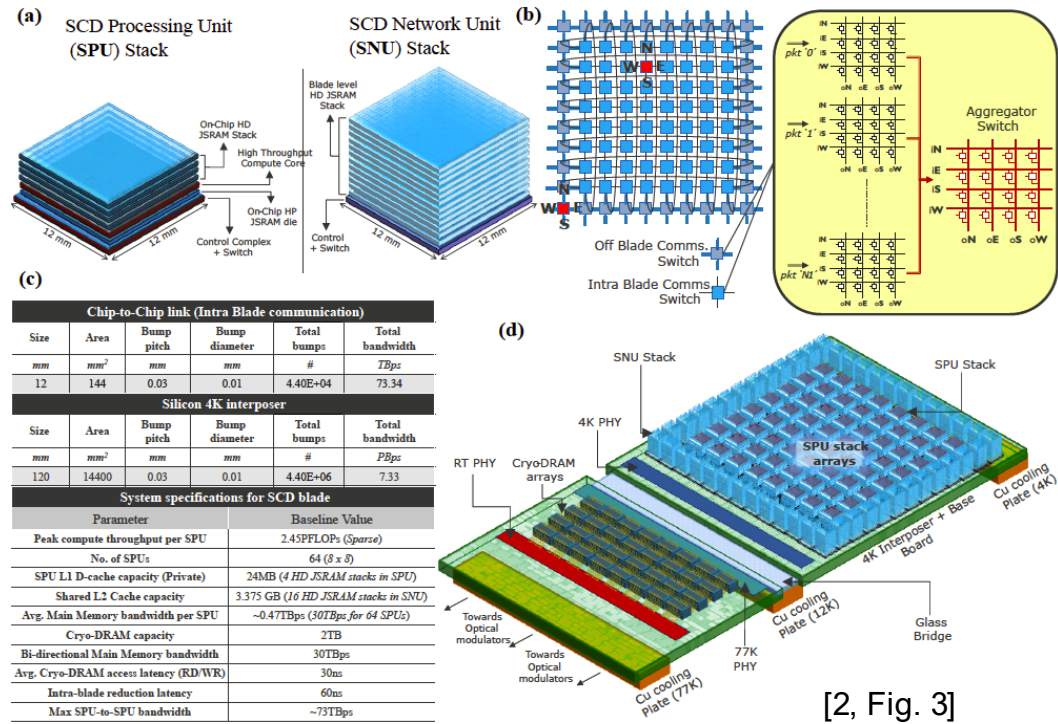
Application area 3



Vision for digital superconductor computing

“Data Center in a Shoebox” (IMEC)

- SPU: Superconductor Processing Unit
 - 4 HD JSRAM chips, 24 MiB total, 4(144 mm²), ~4(5E+8 JJ)
 - 1 HP JSRAM chip, ? MiB total, 1(144 mm²)
 - 1 compute core, 1(144 mm²), ~5E+7 JJ
 - 1 control + switch, 1(144 mm²), ~5E+6 JJ
 - 64 SPUs, ~ 2E+9 JJ/SPU
- SNU: Superconductor Network Unit
 - 16 HD JSRAM chips, 3.4 GiB total, 16(144 mm²), ~16(5E+8 JJ)
 - 1 control + switch, 1(144 mm²), ~5E+6 JJ
 - 48 SNUs, ~8E+9 JJ/SNU
- Totals
 - Chips: 64(6) + 48(17) = 1200
 - Area: 1200(144 mm²) = 172,300 mm²
 - JJs: 64(2E+9) + 48(8E+9) = ~5E+11
 - New technologies: 5+ (fab, logic, memory, power, TSV, ?)



[1] A. Herr, Q. Herr, 2024, doi: [10.1109/MSPEC.2024.10551792](https://doi.org/10.1109/MSPEC.2024.10551792)
Public: <https://spectrum.ieee.org/superconducting-computer>

[2] J. Kundu et al., “A system level performance evaluation for superconducting digital systems,” 2025. doi: [10.23919/DATE64628.2025.10992879](https://doi.org/10.23919/DATE64628.2025.10992879)

Brain-inspired Computing (BIC)

Application area 4



Neuromorphic Circuits using Superconductor Electronics

A more natural fit?

- Natural spiking behavior of Josephson junctions
- Pulses travel on striplines without the RC time constants that typically hinder spike-based computing
- Possibly tolerant to variations in component parameter values

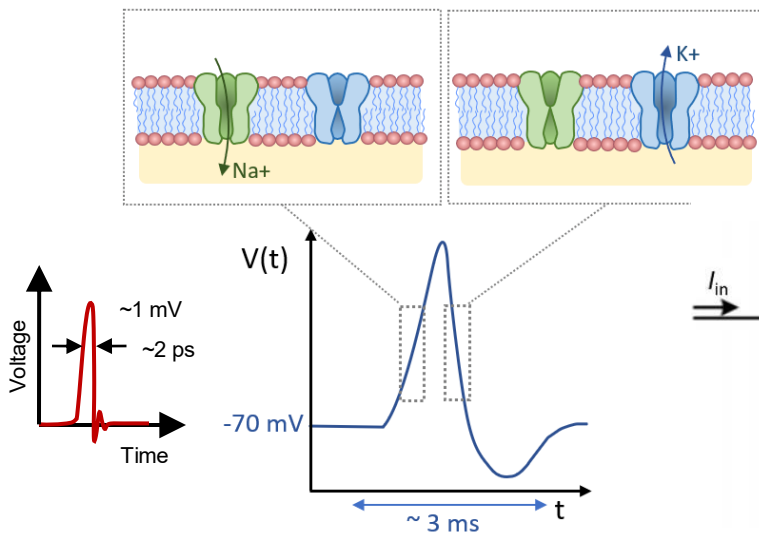


Fig. 3a. Spiking in biological neurons [1]

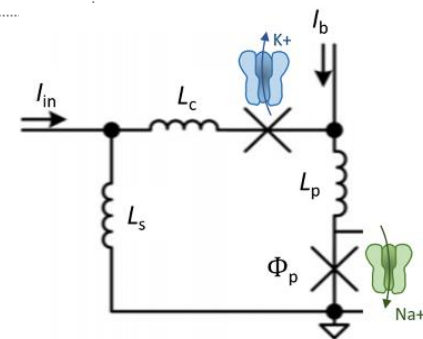


Fig. 4a. JJ neuron circuit [1]

[1] Schneider+ “**Supermind**,” *SuST*, 2022, doi: [10.1088/1361-6668/ac4cd2](https://doi.org/10.1088/1361-6668/ac4cd2)

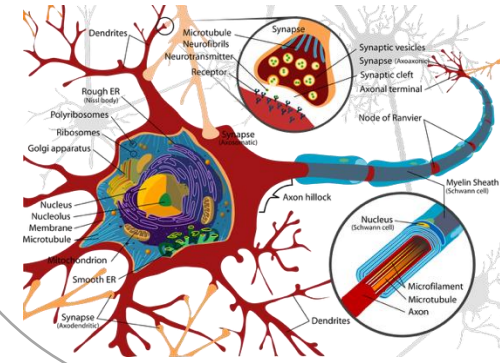
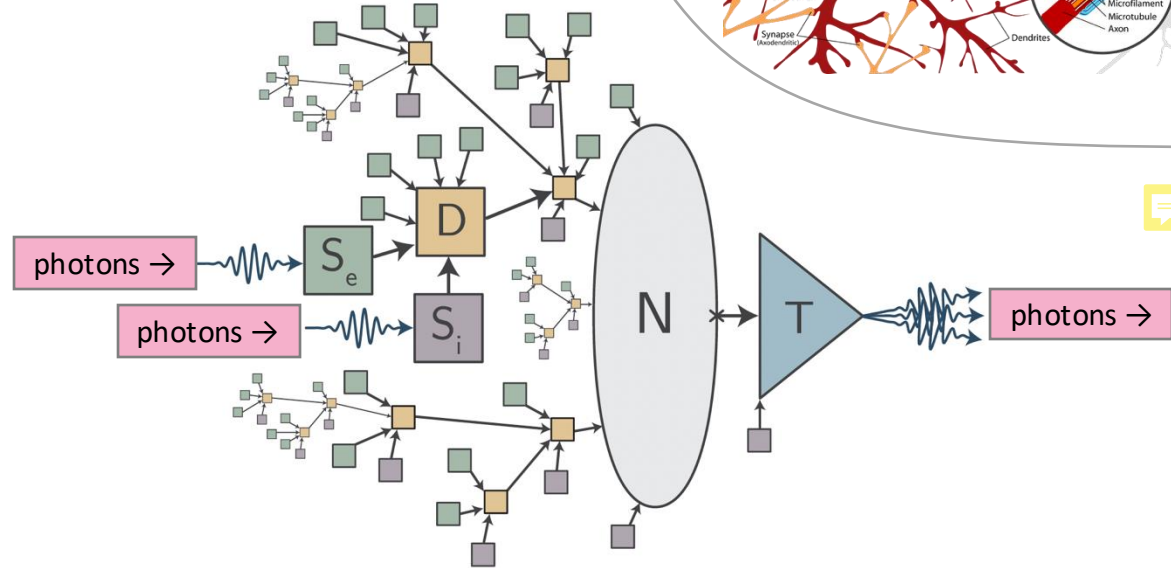


Brains and neurons are complex

Example: Optoelectronic implementation

• Components

- S_e : synapse, excitory
- S_i : synapse, inhibitory
- D : dendrite
- N : nucleus or soma
- T : transmitter (EO)
- \rightarrow : axon (waveguide)

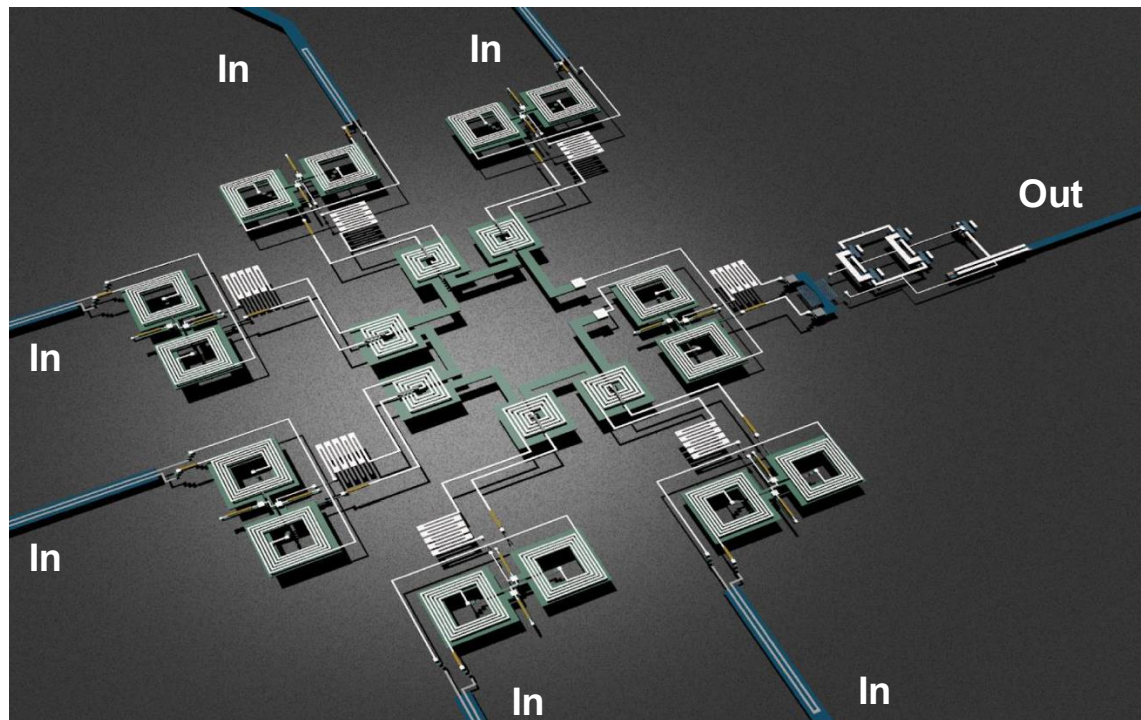




Superconducting optoelectronic networks (SOENs)

Example from Great Sky AI

- Neurons: SCE
- Interconnects: photonic
- Picture:
 - Simple neuron with 6 synaptic inputs and a photonic output
 - 8 JJs per synapse
 - 3 JJs per dendrite
 - 2 JJs per soma
 - + transformers, SSPDs, ...
 - = ~100 J/neuron?
- Goal:
 - 1000+ synapses per neuron



discoverexpedition.usc.edu/outreach/#seminarseries > Shainline

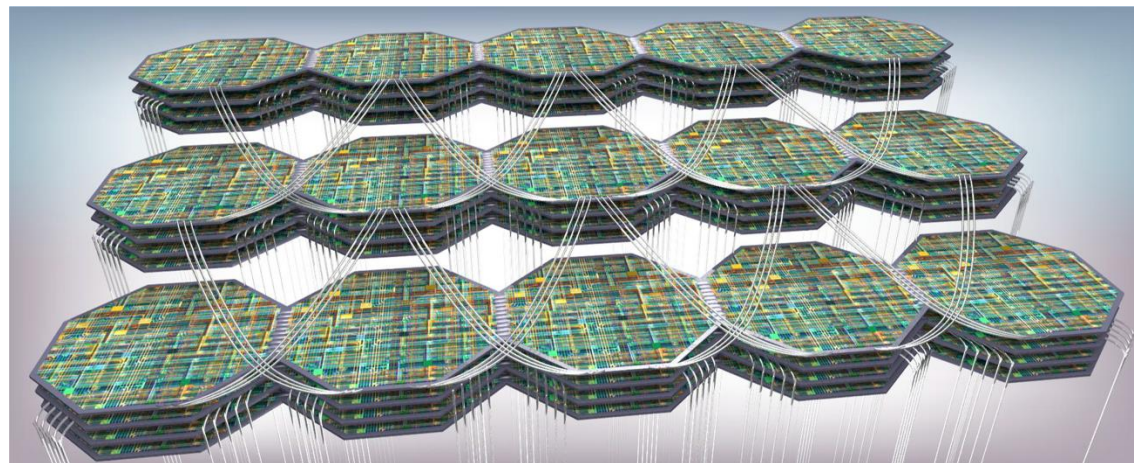
Shainline, "Optoelectronic intelligence," *APL*, 2021, doi: [10.1063/5.0040567](https://doi.org/10.1063/5.0040567)



Superconducting optoelectronic networks (SOENs)

Jeff Shainline, Great Sky AI

- 300 mm wafer
 - 1E+6 neurons
 - 1E+9 synapses
 - 1E+10 (+) = ~ 1E+11 JJs
 - 65× human brain SynOp/s
- System (1000 wafers)
 - 1E+9 neurons
 - 1E+12 synapses
 - 1E+13 (+) = ~ 1E+14 JJs
 - 1E+12 parameter model
 - ~ 1 m³



discoverexpedition.usc.edu/outreach/#seminarseries > Shainline

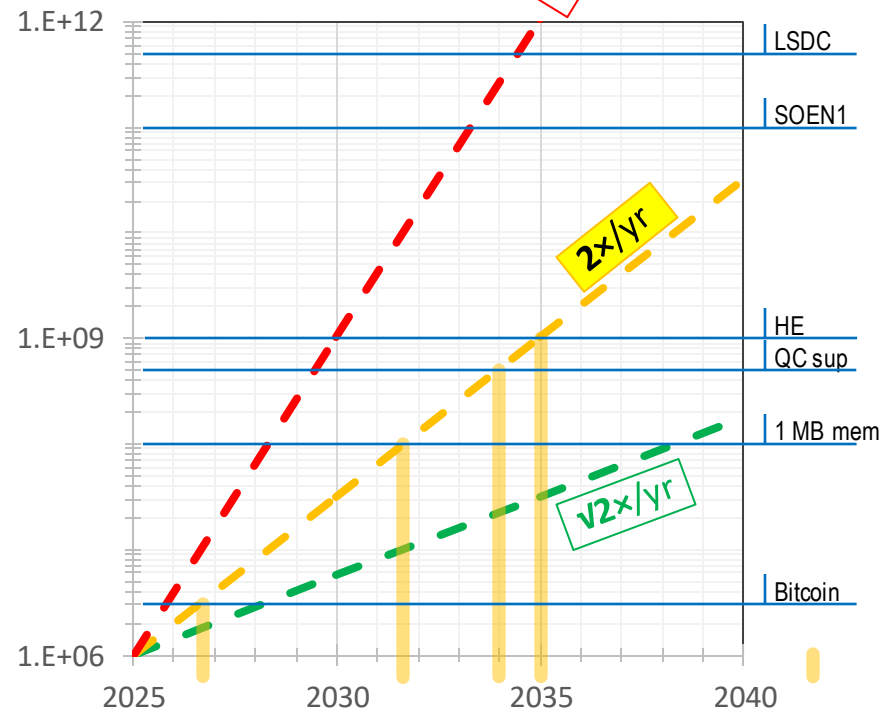
Roadmap and Conclusions

Application needs and timeline

Drivers for technology roadmaps

Application	Circuit family	~ JJ count, min.
Sensor readout		1E+2
Array readout (8x8)		1E+4
DSP: digital signal processing		
• FFT (8 b, 64 pt)	RSFQ	1E+5
• FIR (256 taps, 16 b)	U-SFQ	2E+5
Bitcoin mining	RQL	3E+6
QC support (2.4E+5 qubits)	ERSFQ	5E+8
Homomorphic encryption	RSFQ	1E+9
Large-scale digital computing		
• Memory chip (1 MB)	PCL	1E+8
• Data center in a shoebox	PCL	5E+11
Brain-inspired computing (BIC)		
• SOEN, 300 mm	SFQ	1E+11
• SOEN, full system	SFQ	1E+14

JJ count



► How fast can we ramp fab?



Conclusions

Large-scale Superconductor Electronics: Opportunities and Challenges

- **Opportunities**

- Stepping-stone applications are available
- Markets exist

- **Challenges**

- **Logic:** Searching for a winning logic family
- **Memory:** better solutions are needed!
- **Design tools** for architecture exploration, SNNs, temporal logic
- **Fabrication:** How fast can we ramp up?
- **Testing:** turnaround time, capacity

- **Roadmaps**

- Provide metrics, goals, and timelines to guide R&D and to evaluate alternatives

Appendix

For more information

- International Roadmap for Devices and Systems (IRDS)
 - <https://irds.ieee.org/>
- Cryogenic Electronics and Quantum Information Processing (CEQIP)
 - <https://irds.ieee.org/editions/2023/20-roadmap-2023-edition/129-irds™-2023-cryogenic-electronics-and-quantum-information-processing>
 - <https://doi.org/10.60627/042b-j892>
 - Chair: D. Scott Holmes, d.scott.holmes@ieee.org
- D. S. Holmes, “Superconductor electronic device technology roadmapping within the IRDS,” *IEEE Electron Devices Society Newsletter*, pp. 6–11, Apr. 2022.
https://eds.ieee.org/images/files/newsletters/Newsletter_Apr22.pdf

2025 CEQIP Members

2024-2025

Changes

15: Americas

10: Europe + Africa

5: Asia

=====

30 total

Name	Area	Organization	Region
Asenov, Asen	Cryo-Semi	University of Glasgow, UK	Europe
Byun, Ilkwon	Cryo-Semi, QIP-QC	Kyushu University, Korea	Asia
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK	Europe
DeBenedictis, Erik	QIP-QC	Zettaflops, USA	Americas
Delfanazari, Kaveh	QIP-QC	University of Glasgow, UK	Europe
Fagaly, Bob	SCE-App	Tristan Technologies (retired), USA	Americas
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland	Europe
Febvre, Pascal	SCE-Fab	Université Savoie Mont Blanc, France	Europe
Filippov, Timur	SCE-Log	HYPRES, USA	Americas
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa	Africa
Frank, Mike	SCE-Log, -Rmap	Sandia National Laboratories, USA	Americas
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