

100 GHz bandwidth measurements of single flux quantum pulses using a Josephson Sampler

Presenter: Pete Hopkins
Superconductive Electronics Group
National Institute of Standards and Technology

Team members: Charlie Burroughs, David Olaya, John Biesecker, Manuel Castellanos-Beltran, and Sam Benz

Outline



Goals

- **SFQ Digital: diagnostic, failure analysis, and model verification**
- **Voltage Metrology: AC voltage standard/RF reference sources**

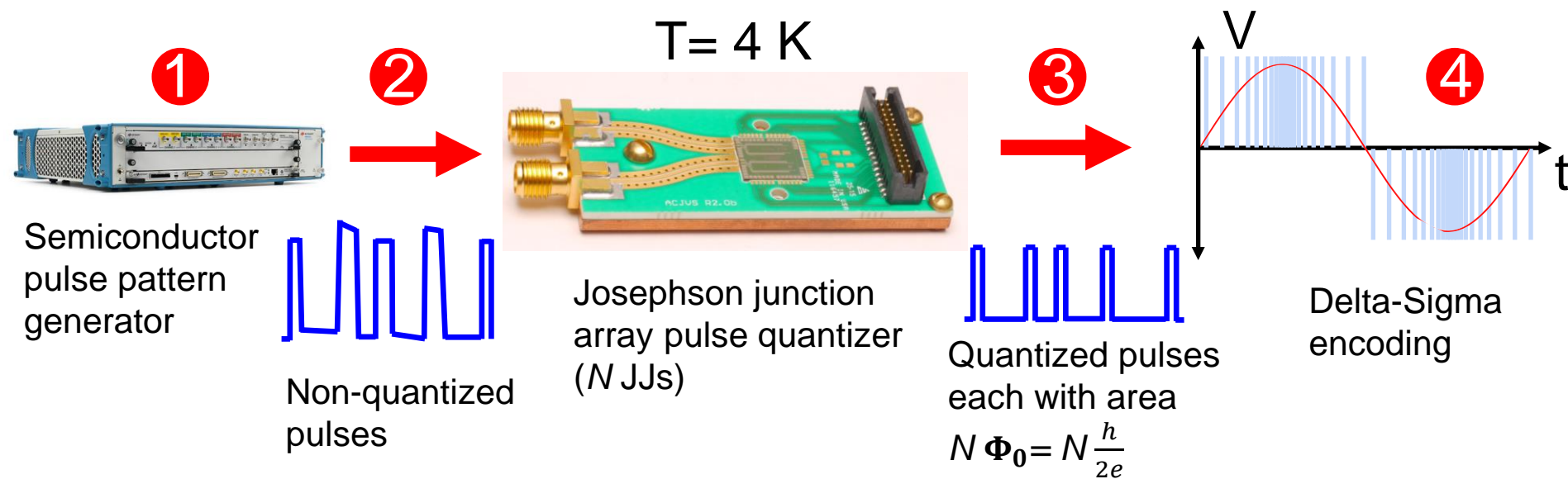
Outline

- Previous work
- Theory of operation
- Fabrication and test setup
- Sampled waveforms of SFQ pulses

Quantum-Based RF (GHz) Sources



Primary AC voltage standard for the world
Josephson arbitrary waveform synthesizer (JAWS)

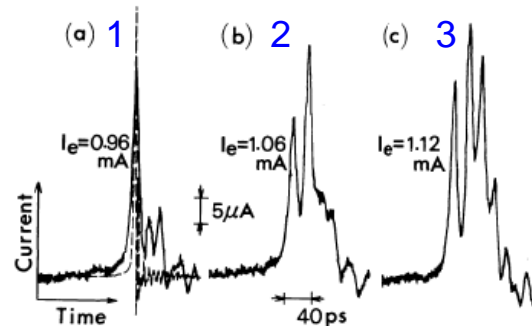
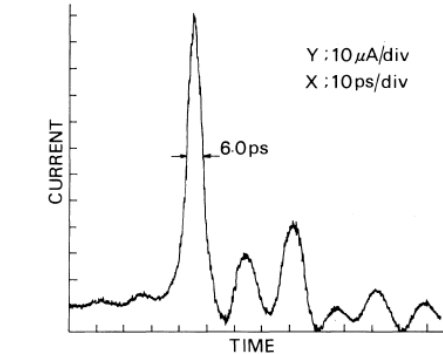


Previous demonstrations of Josephson Samplers **NIST**

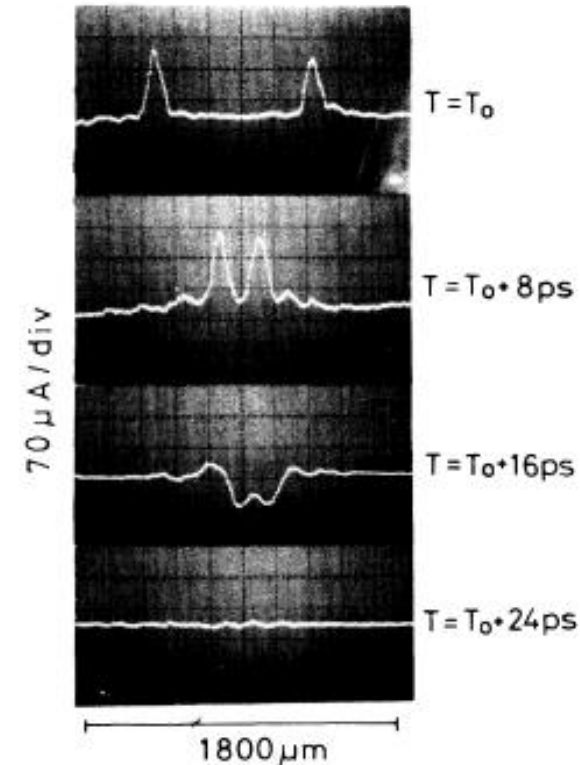
HYPRESS MODEL PSP-1000 PICOSECOND SIGNAL PROCESSOR (#4122)



Sakai et al., Japan JAP (1983)
Electrotechnical Laboratory

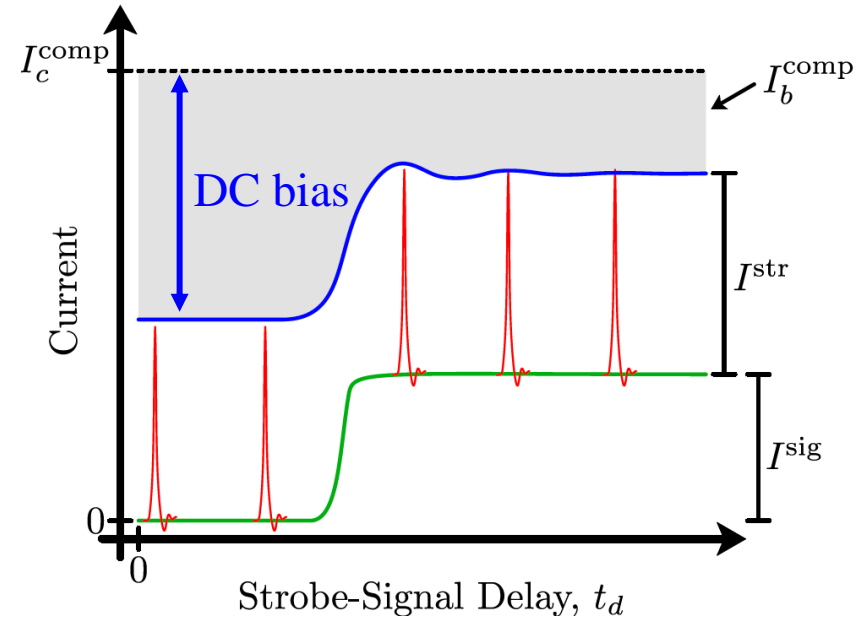
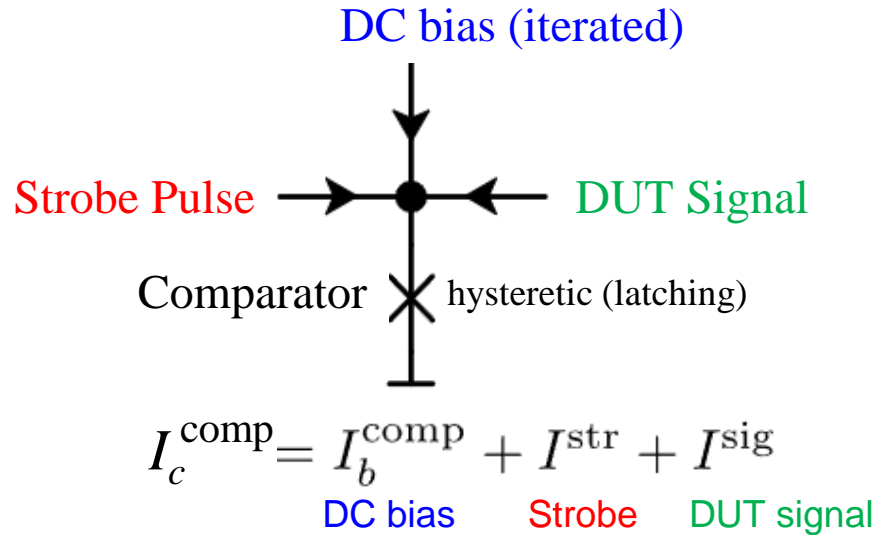


Fujimaki et al., PRL (1987)
Tohoku University

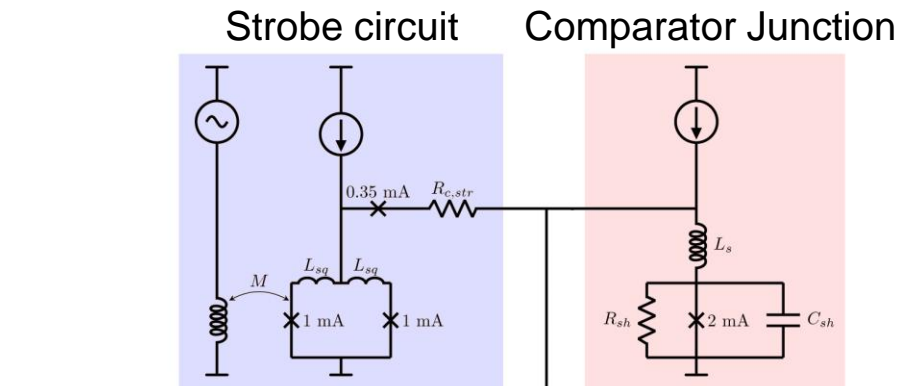


Picosecond waveform sampling using fast JJs

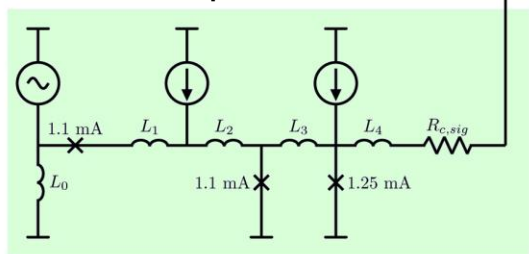
Operation



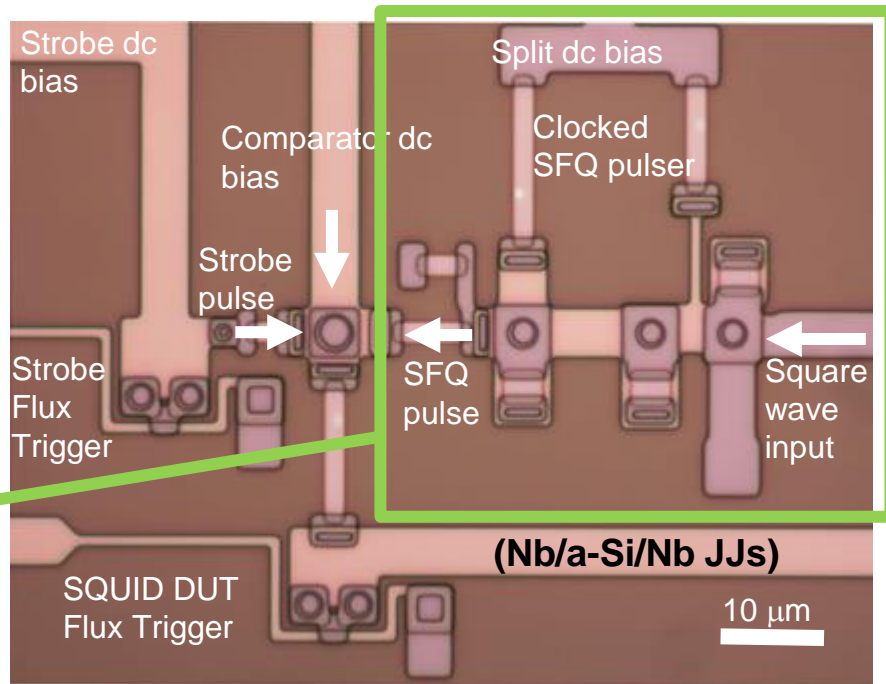
Sampling an SFQ pulse waveform



Clocked SFQ pulser device under test (DUT)



Charlie Burroughs

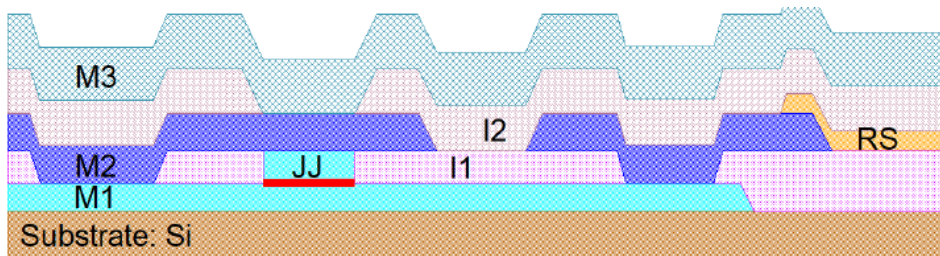


Sampler integrated on-chip measures SFQ pulses from Device Under Test (DUT)

Fabrication at NIST



3 metal layer fab with Nb/a-Si/Nb JJs



- 3" intrinsic silicon wafers
- 3 Nb layers including skyplane
- SiO_x dielectric
- Nb/a-Si/Nb JJs, $J_c = 0.2 \text{ mA}/\mu\text{m}^2$
- PdAu resistors, $2 \Omega/\text{sq}$.
- on-chip 100Ω series resistors on DC lines

NIST's Boulder Microfabrication Facility



1700 m² ISO Class 100 Cleanroom

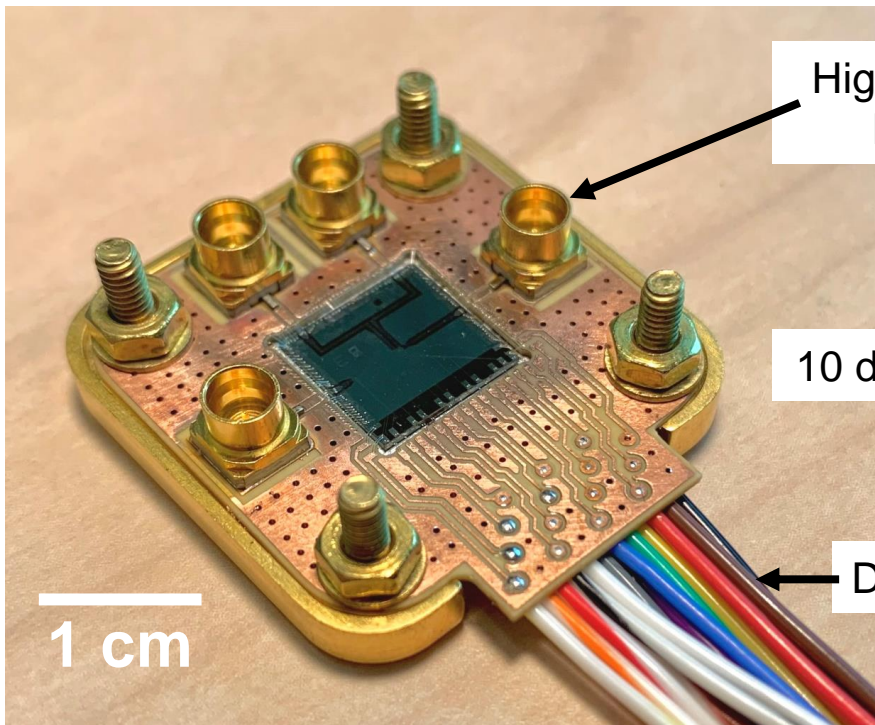


Olaya

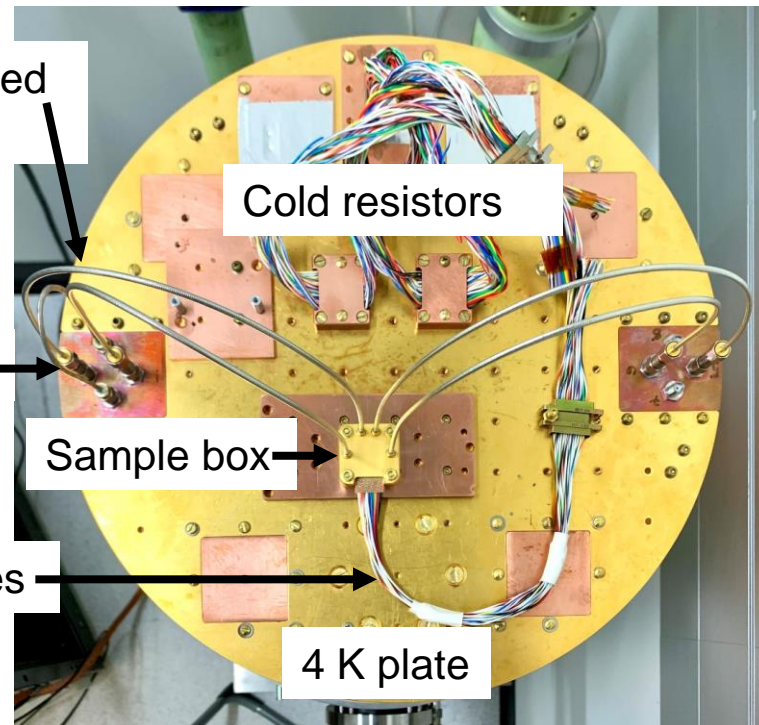


Biesecker

Packaging and mounting

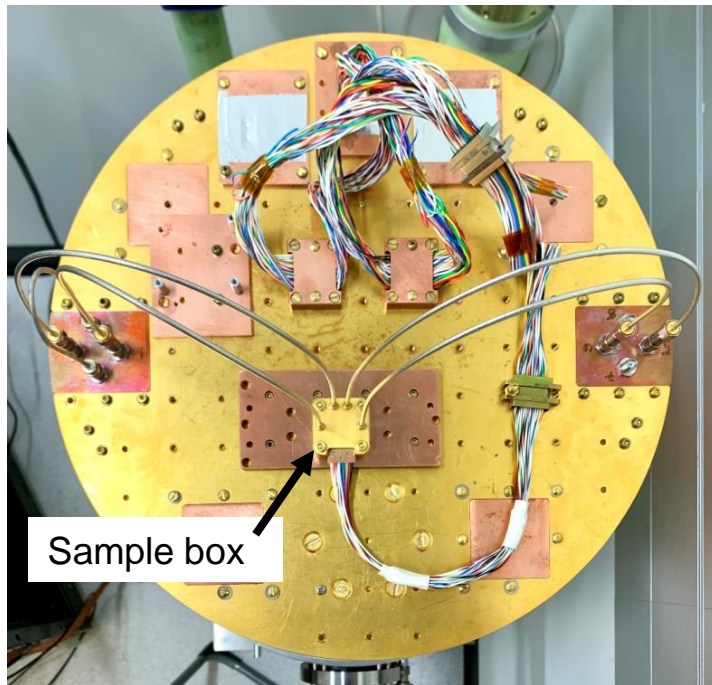


Packaged JJ Sampler Chip

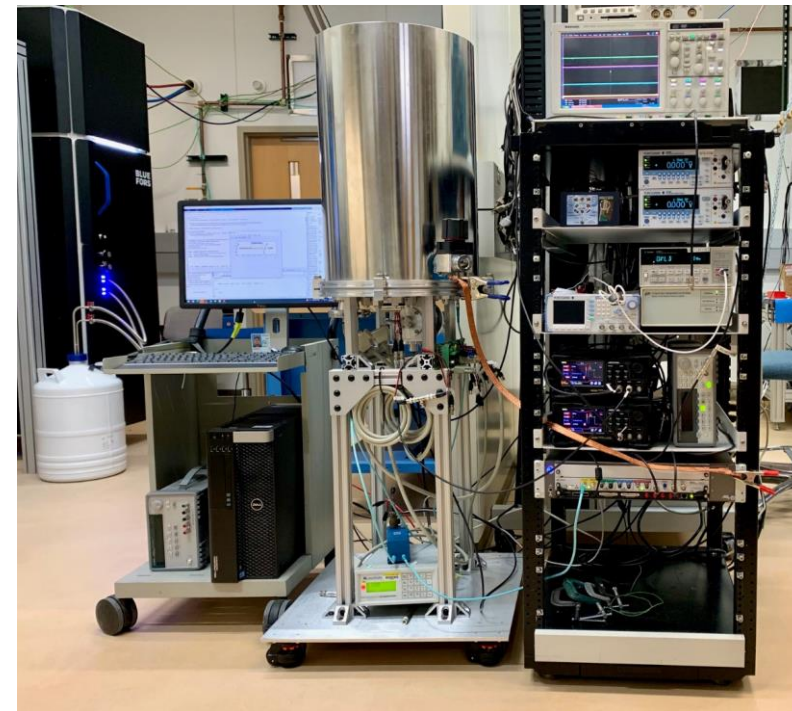


Cryostat configuration

Operational JJ Sampler System



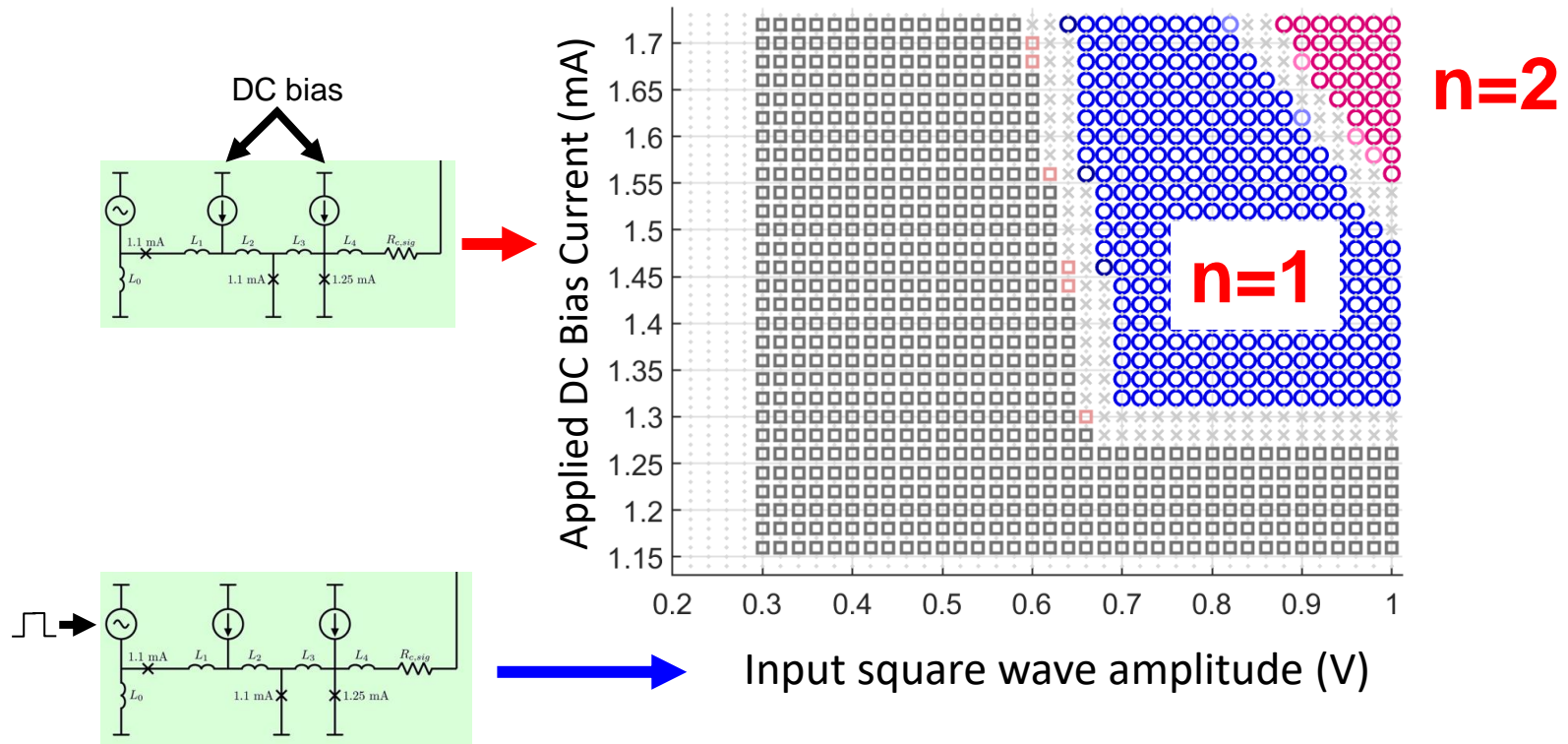
GM-cooled 4 K Cryostat



**Josephson Sampler System
(Cryostat and Electronics)**

Clocked SFQ Pulser – Quantum Locking Range

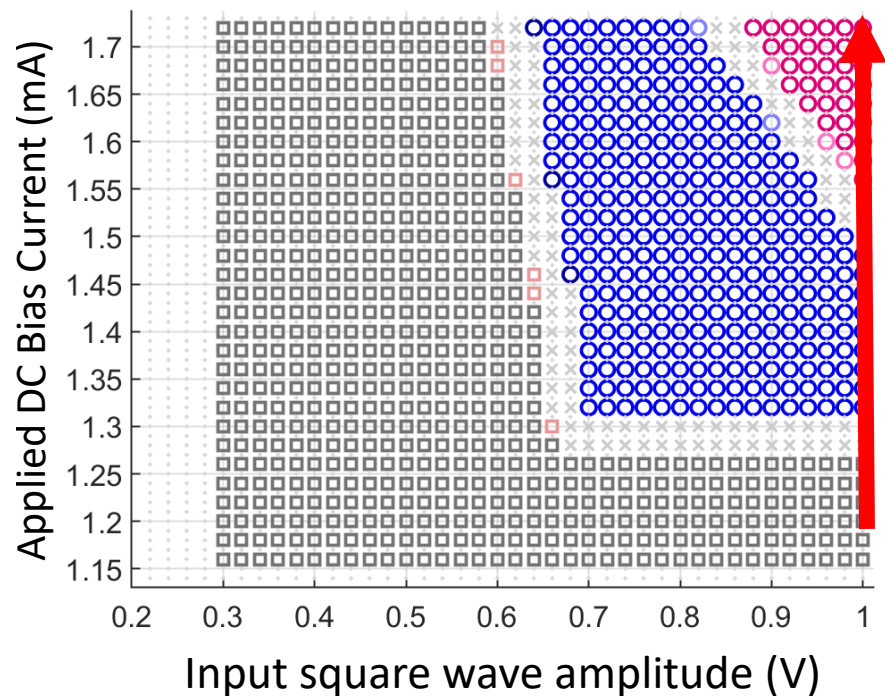
Output DC Voltage of SFQ Pulser at 8 GHz



Clocked SFQ Pulser – Quantum Locking Range

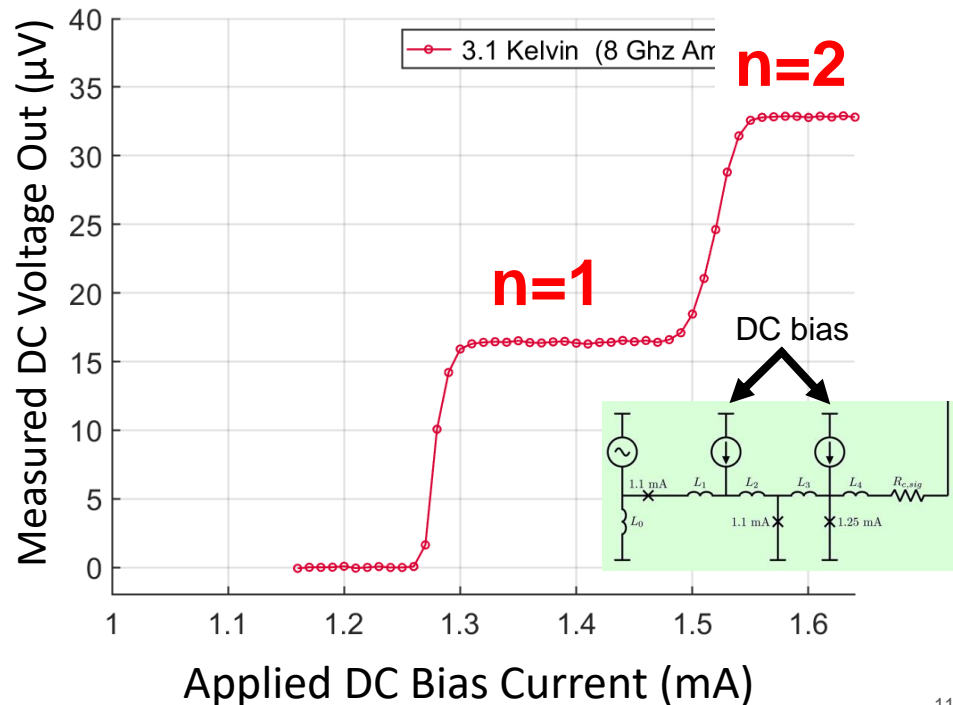
Quantum Locking Range (3.1 Kelvin)

Measured QLR of DC-SFQ Pulser



Extracted “Traditional” Plot

Measured Output of DC-SFQ Pulser

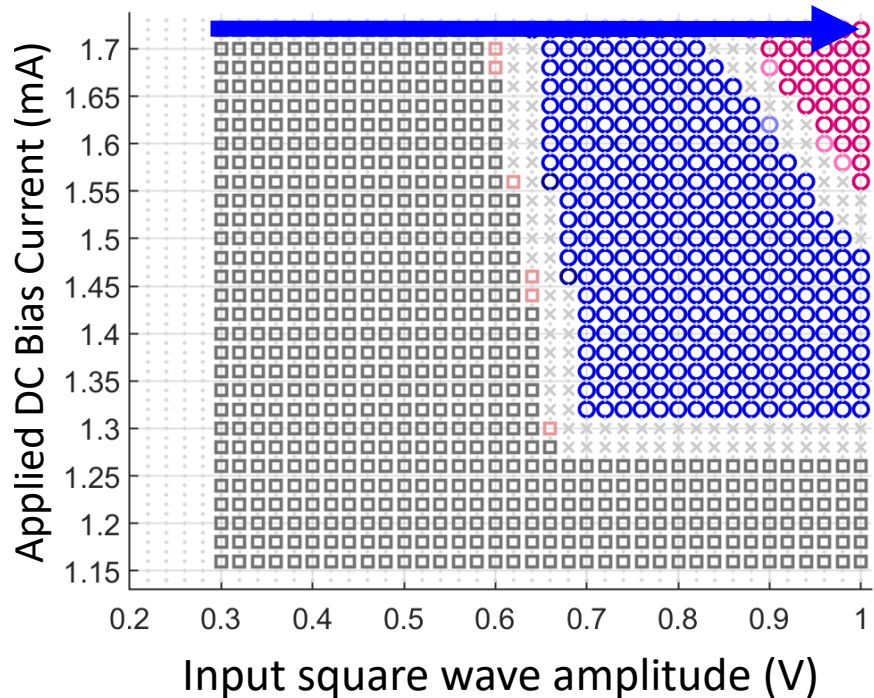


Clocked SFQ Pulser - QLR Measurements



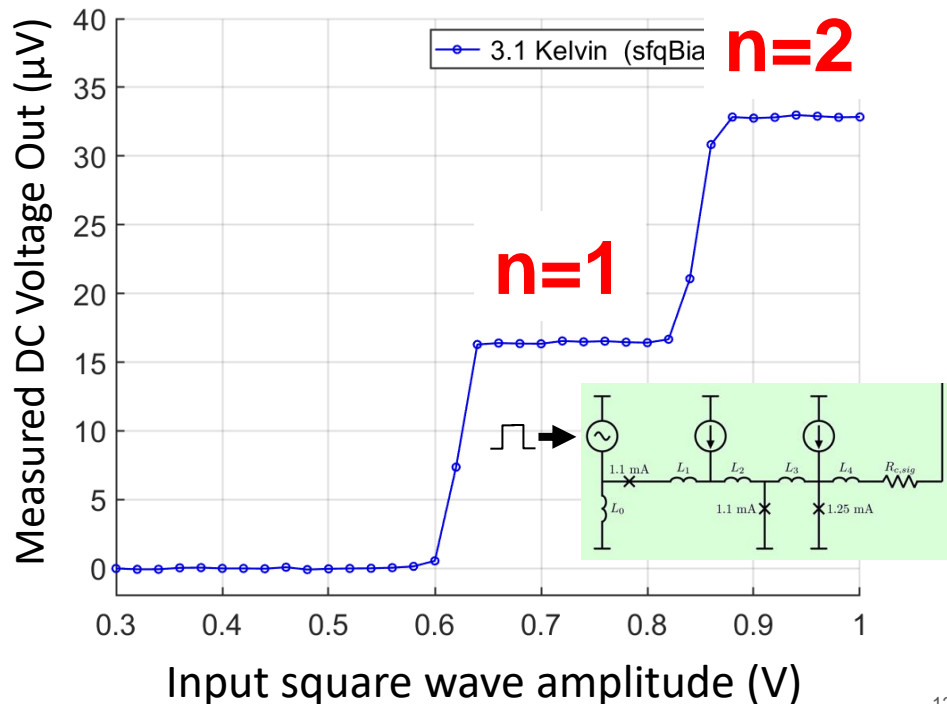
Quantum Locking Range (3.1 K)

Measured QLR of DC-SFQ Pulser



Extracted “Traditional” Plot

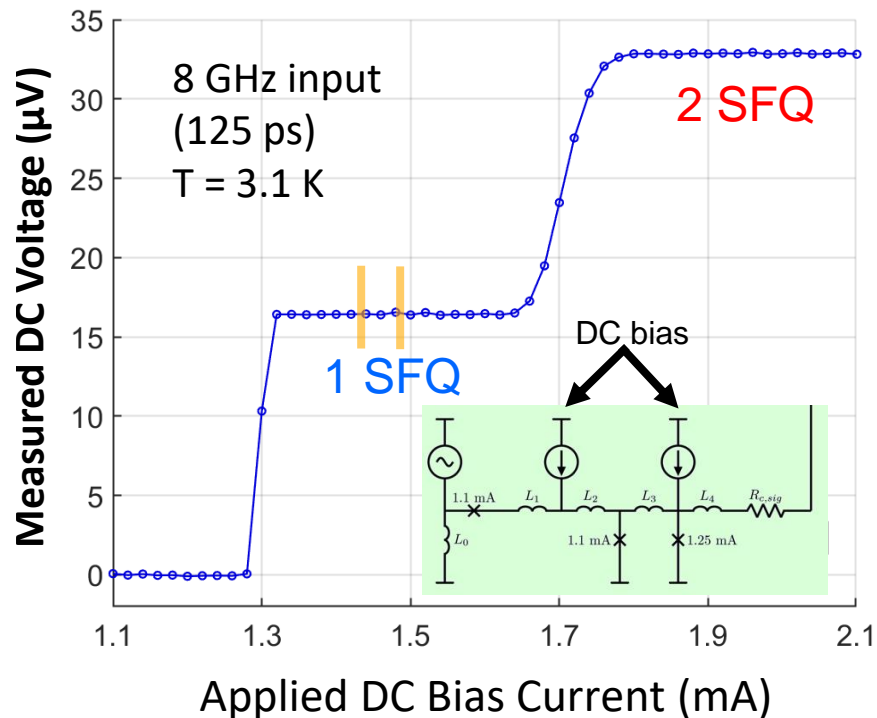
Measured Output of DC-SFQ Pulser



Clocked DC-SFQ Pulser Testing

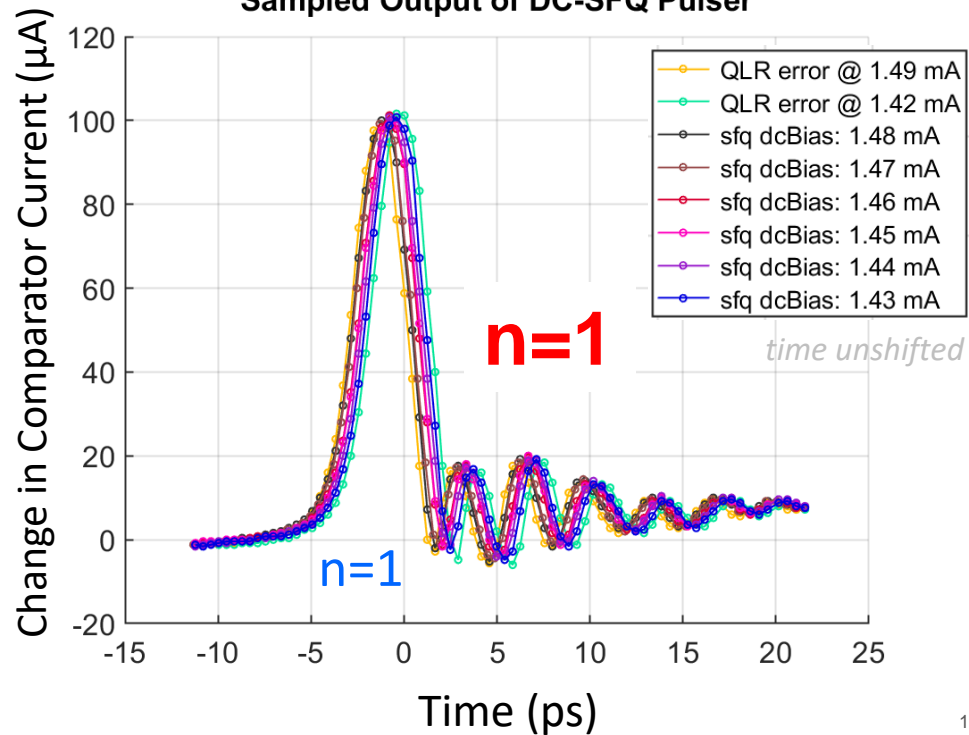
Quantum Locking Range verification

Measured Output of DC-SFQ Pulser



JJ Sampler Image SFQ pulses

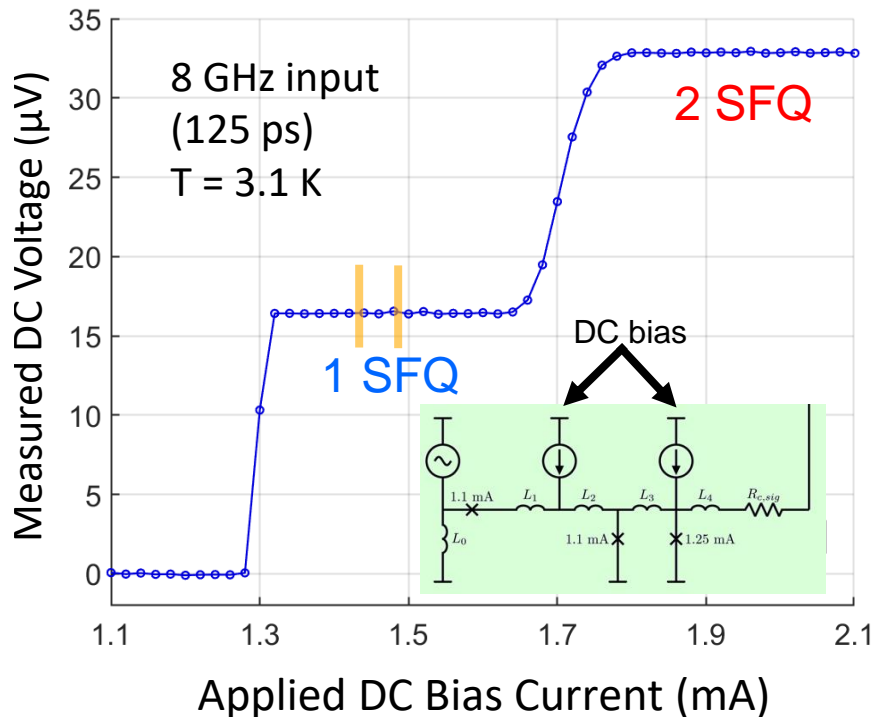
Sampled Output of DC-SFQ Pulser



Clocked DC-SFQ Pulser Testing

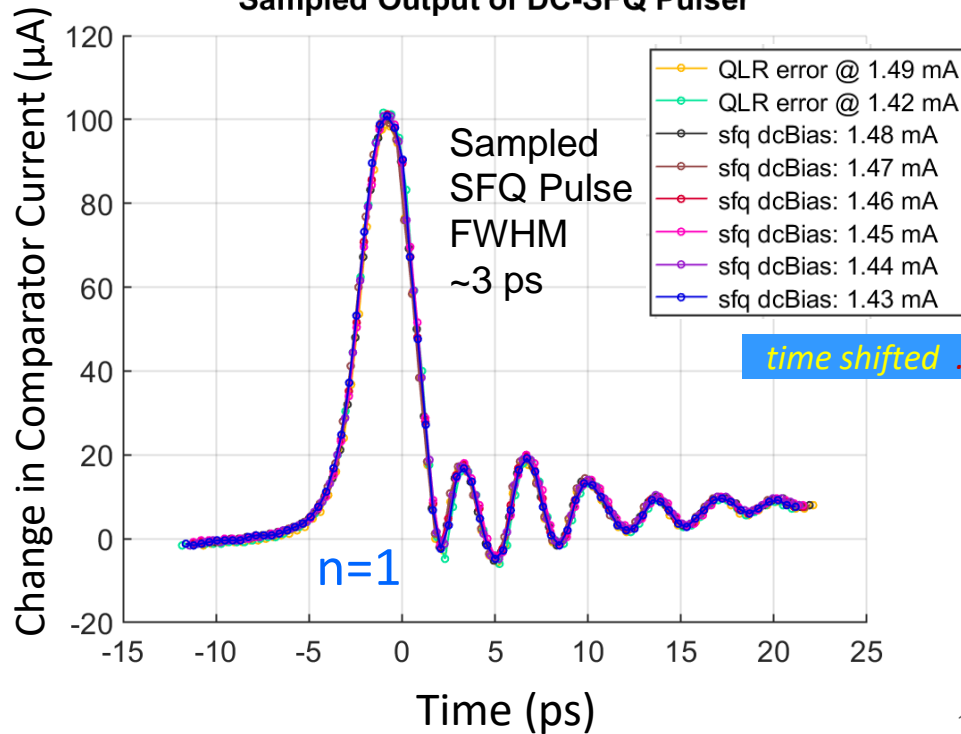
Quantum Locking Range verification

Measured Output of DC-SFQ Pulser



JJ Sampler Image SFQ pulses

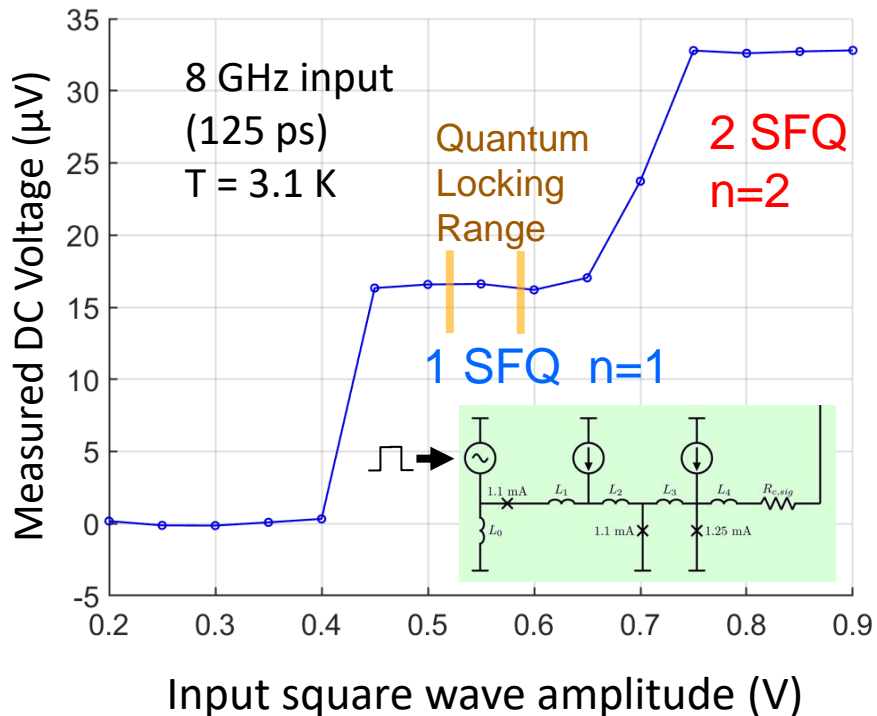
Sampled Output of DC-SFQ Pulser



Clocked DC-SFQ Pulser Testing

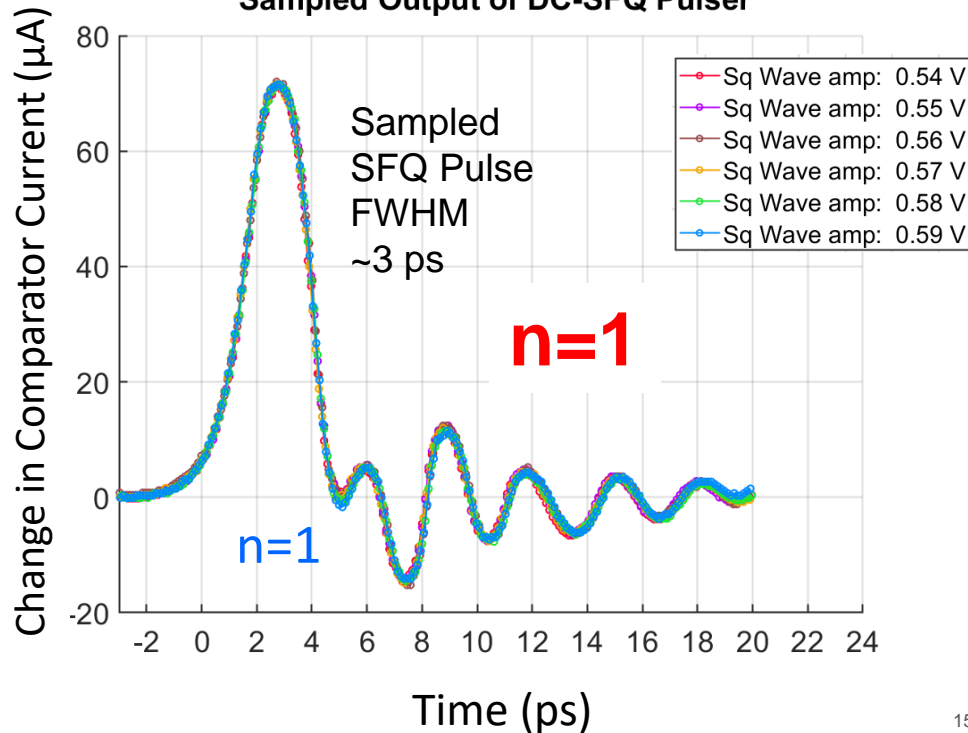
Quantum Locking Range verification

Measured Output of DC-SFQ Pulser



JJ Sampler Image SFQ pulses

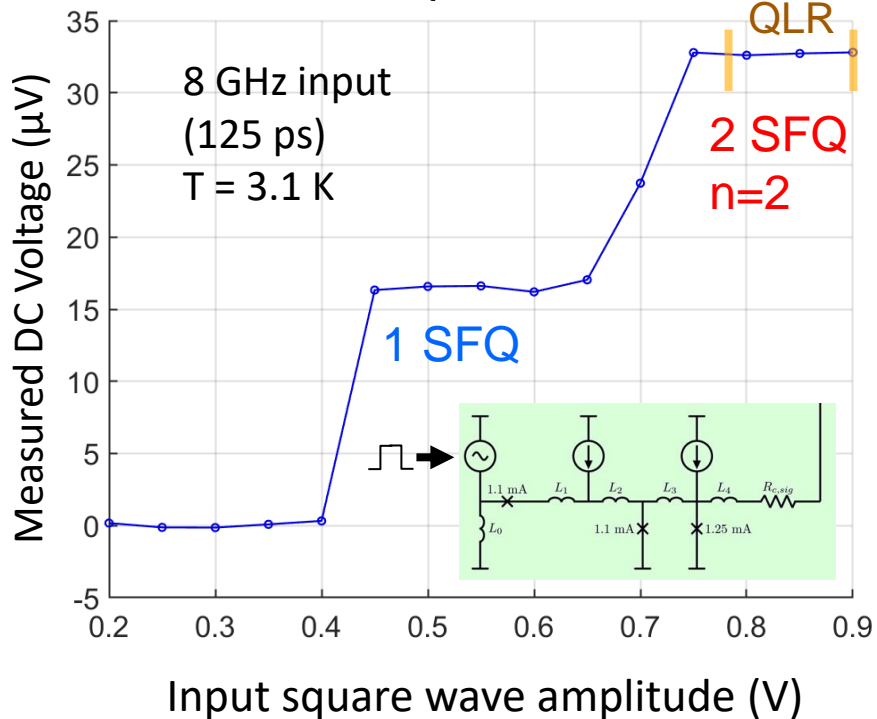
Sampled Output of DC-SFQ Pulser



Clocked DC-SFQ Pulser Testing

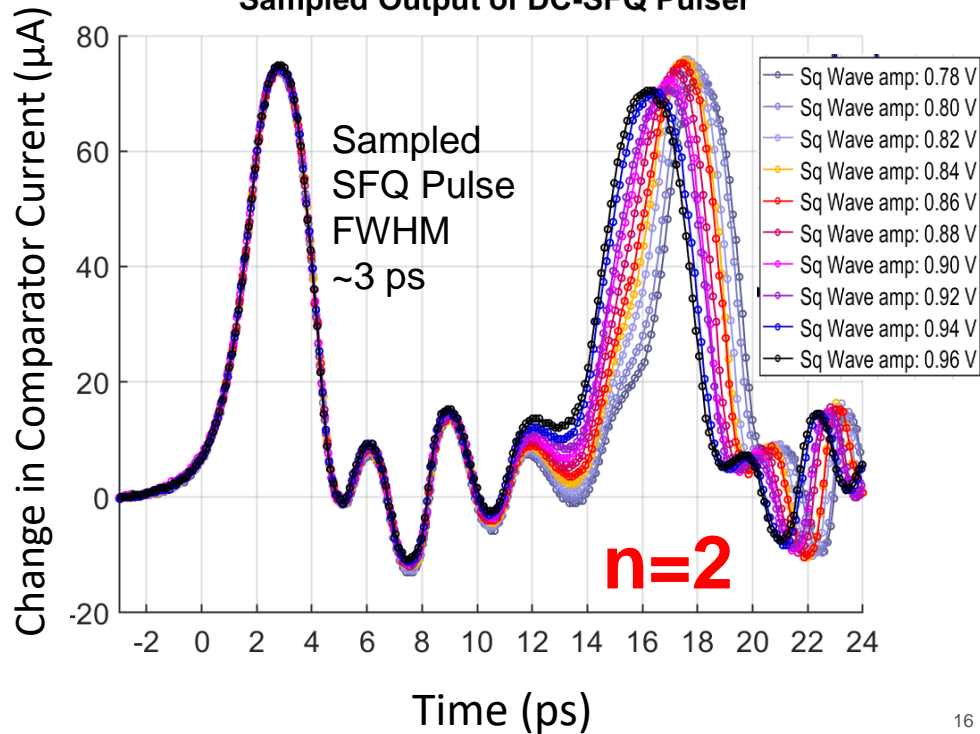
Quantum Locking Range verification

Measured Output of DC-SFQ Pulser



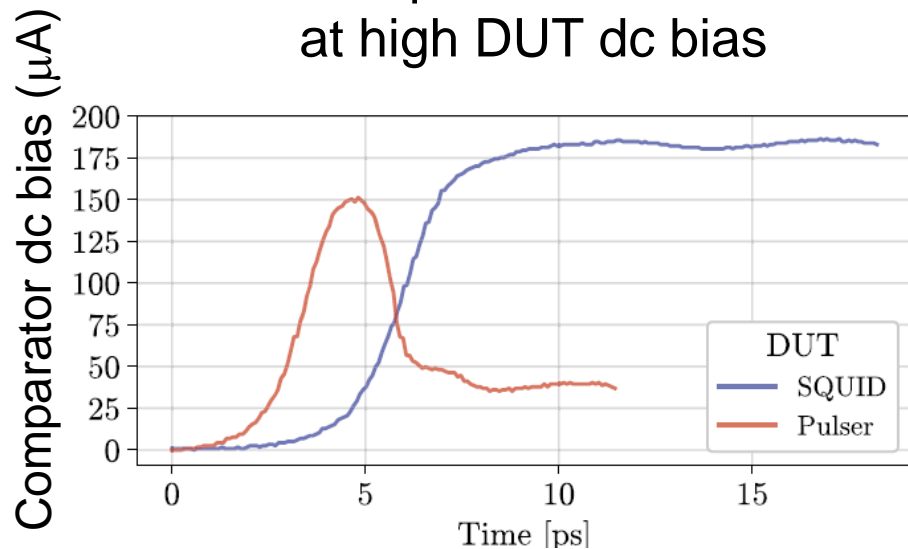
JJ Sampler Image SFQ pulses

Sampled Output of DC-SFQ Pulser

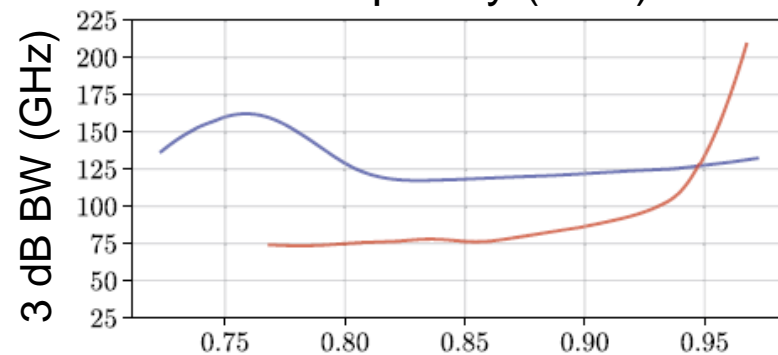
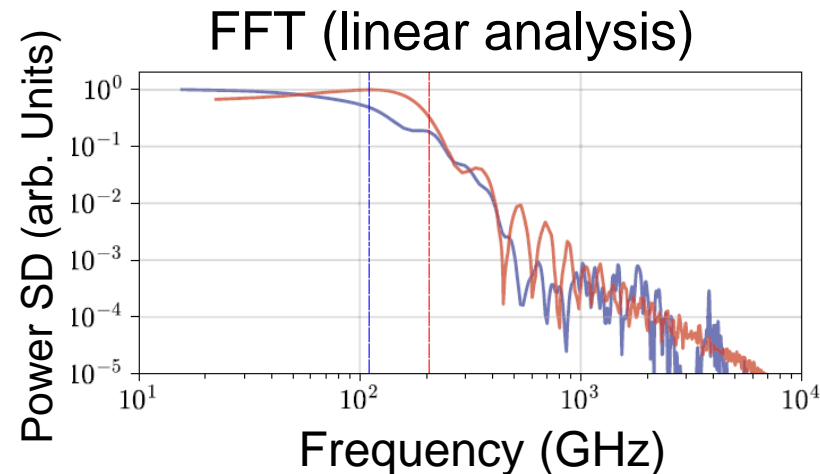


Sampler bandwidth

Sampled waveforms
at high DUT dc bias



- convolved waveform
- 175 GHz BW is lower bound



Normalized dc bias

JJ Sampler – Challenges and Next Steps



Challenges

1. DUT waveform distortion/convolution: characterizing and minimizing
2. Detecting subtle pulse-shape differences
3. Speedup of data acquisition

Next Steps

1. Demonstrating applications to SFQ digital logic and AC voltage circuits
 - e.g. does trapped flux alter SFQ pulse shape and timing?
 - Detecting pulse-shape and delay differences in quantum locking range