27-29 October 2025

Progress towards high-density superconductor digital logic

Leonard M. Johnson

Quantum-Enabled Computation Group

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

This material is based upon work supported by the Under Secretary of War for Research and Engineering under Air Force Contract No. FA8702-15-D-0001 or FA8702-25-D-B002. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Under Secretary of War for Research and Engineering.

MIT Lincoln Laboratory
Quantum-Enabled Computation Group

MIT Lincoln Laboratory

Federally-funded research & development center located in Lexington, Massachusetts

~4500 employees

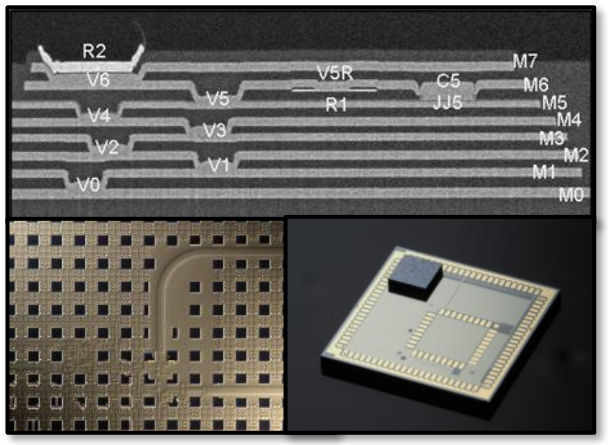
Quantum-Enabled Computation Group

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Quantum-Enabled Computation Group

Mission: Develop advanced hardware, systems, and algorithms that leverage quantized signals for transformative computational advantage

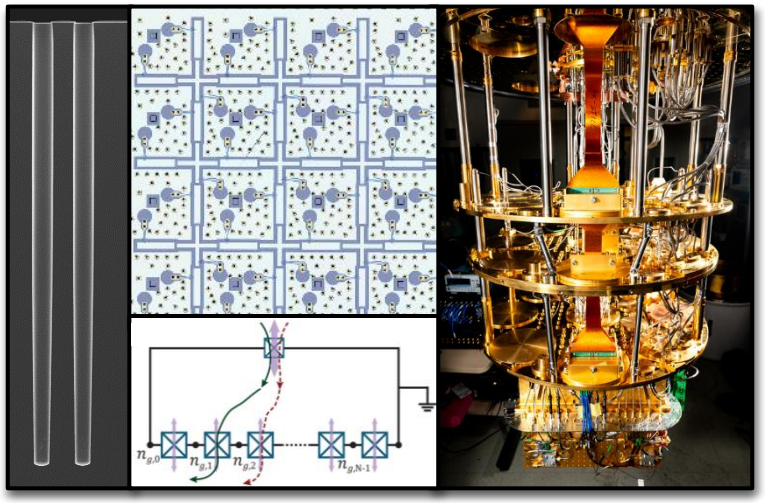
Superconductor Electronics (SCE)



- Demonstrating and validating efficient SCE supercomputing and processing concepts
- Enhancing SCE foundry capabilities to access new paradigms for cryogenic computing
- Enabling new sensing, detection, control, and digitization capabilities with SCE electronics

Demonstrate transformative capabilities in SCE platforms and applications

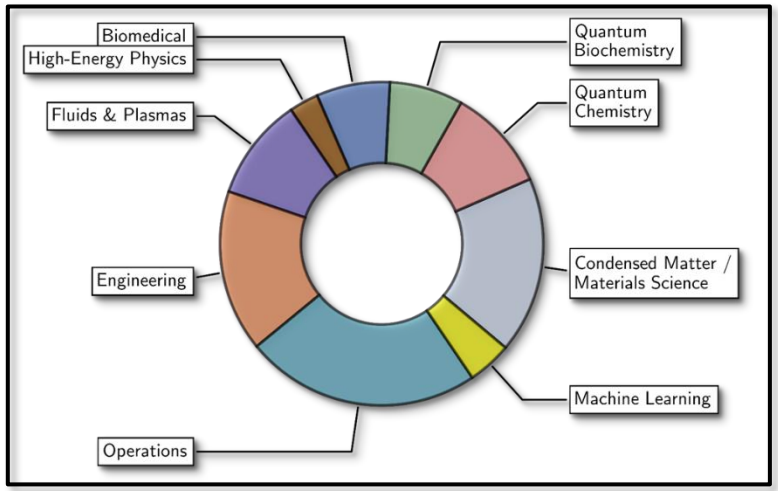
Superconducting Qubits (SCQ)



- Advancing fundamental science of SCQ devices
- Pathfinding for advanced integration & routing Building verification and validation protocols for quantum logic
- Accelerating fundamental research via SQUILL Foundry

Chart the path to useful quantum computation with superconducting devices

Quantum Information Science (QIS)



- Quantifying quantum utility for government and commercial sector
- Mapping applications to algorithms and processors
- Investigating tradeoffs in physical qubit architecture

Quantify and expand the use case for quantum computation

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

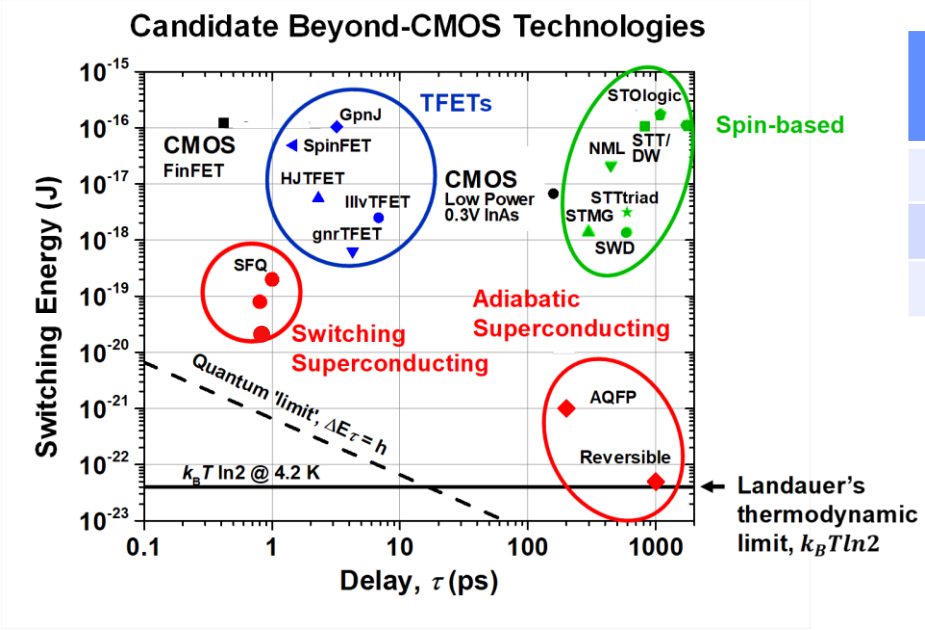
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Outline

- **Overview of MIT Lincoln Laboratory SCE integrated circuit foundry**
- **SCE digital logic applications and motivation for advanced process nodes**
  - **In context of continuing advances in digital CMOS technology**
- **Advanced process node development (SFQ7ee)**
  - **Emphasis on increasing SCE circuit density**
    - **Compact kinetic inductors**
    - **Self-shunted Josephson junctions**
- **Flux-trapping diagnostics and mitigation**

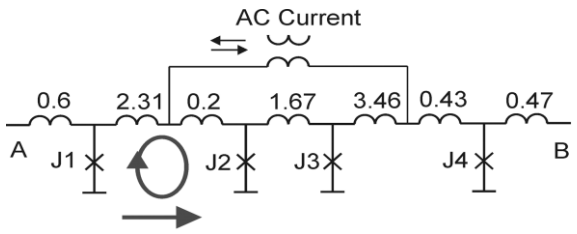
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Superconducting Electronics (SCE) for Low-Energy Digital Computation

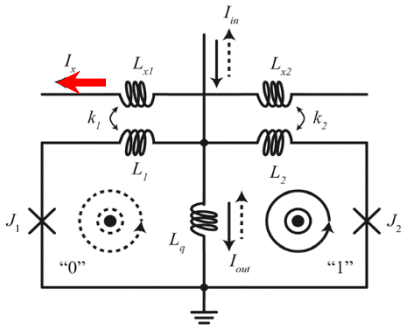


Logic Element	5-nm CMOS FinFET	SCE AQFP	Energy Ratio CMOS / SCE	
			w/o cooling	w/cooling
4-bit Adder	8*10^-15 J	8*10^-20 J	~10^5	~10^2
4-bit Multiplier	4*10^-14 J	4*10^-19 J	~10^5	~10^2
Data Transfer	10^-13 J/b	10^-19 J/b	~10^6	~10^3

SFQ



AQFP



- <u>Lowest energy</u> per digital bit operation
  - Adiabatic Quantum Flux Parametron (AQFP): ~10^-21 J
- <u>Highest clock rate</u> in digital circuits
  - Single Flux Quantum (SFQ): >100 GHz
- <u>Nearly lossless data transmission</u>: 10^-19 J/bit
- Operates in closed-cycle cryocooler at 4K

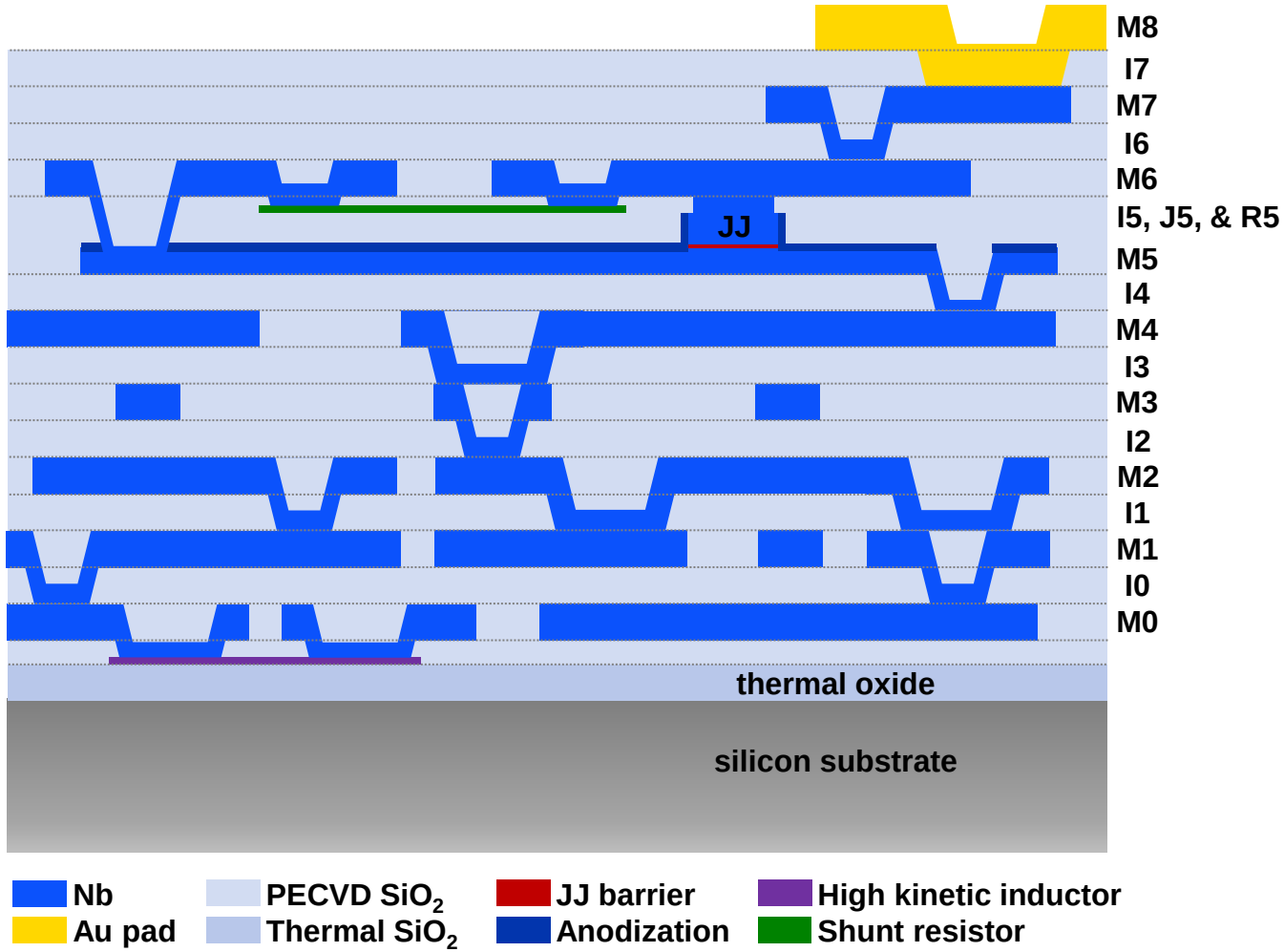
Superconductor electronics (SCE) is the lowest energy of all beyond-CMOS technologies for digital computation

See also: Chen et al, Nature Scientific Reports (2019)

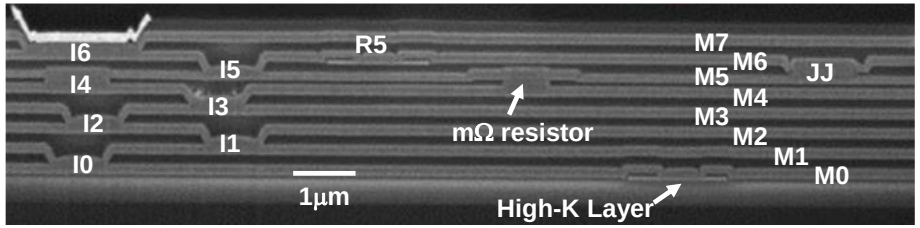
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

MIT-LL SFQ5ee Research Foundry Process Node

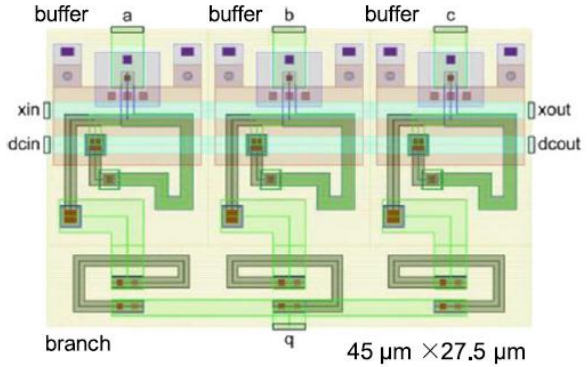
MIT LL SFQ5ee cross section



- 8 Nb layers, fully planarized
- 700 nm Josephson junctions (min)
- J_C : standard 100 μA/μm²
  - optional 2, 4, 200 & 600 μA/μm²
- Wiring: 250-nm minimum feature size
- Mo_2N high kinetic inductance layer



Example SFQ5ee layout: AQFP MAJ3 gate [1]

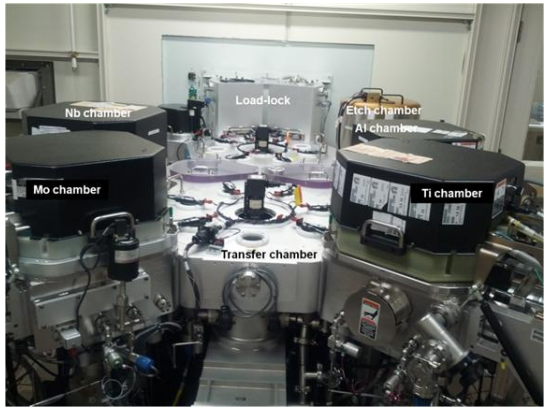


[1] He, Ayala, Takeuchi, Sahu et al., *Supercond. Sci. Technol.* 33(035020) (2020)

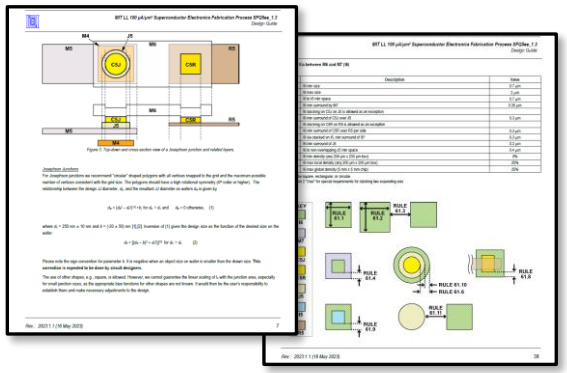
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

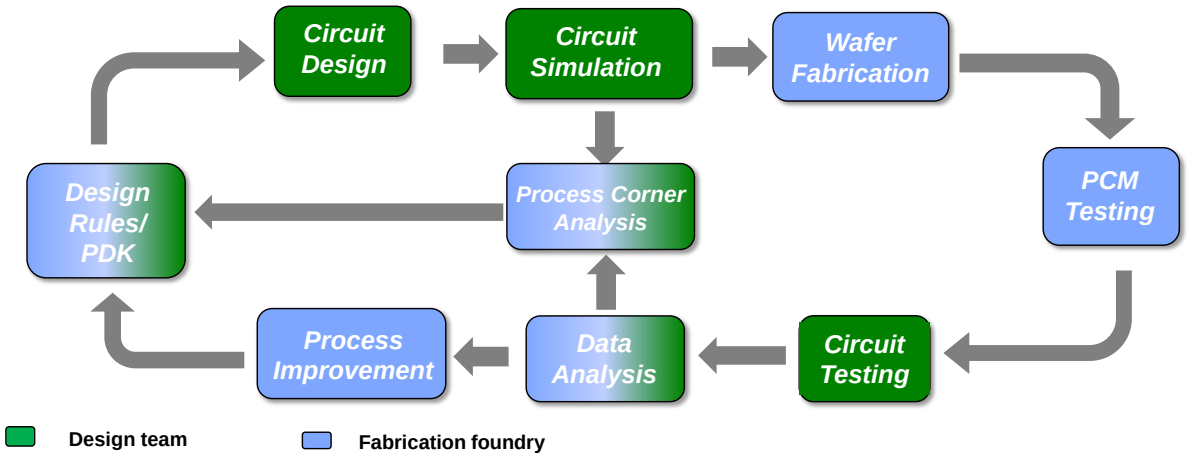
MIT LL Foundry for Superconductor Electronics (SCE)

MIT-LL Microelectronics Laboratory (Class 10, 200-mm wafers)



MIT LL SFQ5ee Design and Modeling Guide





Fabrication capability for advancing the state-of-the-art of SCE integrated circuits

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

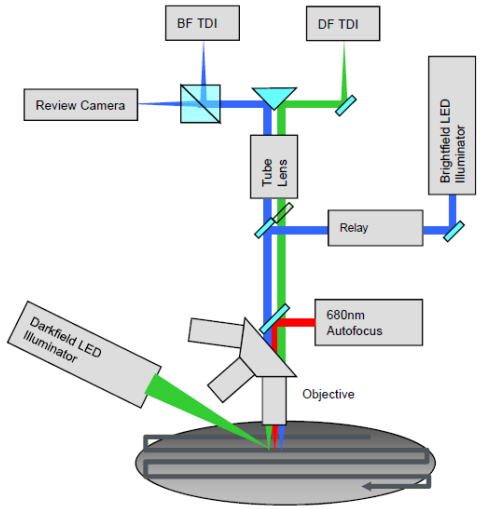
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

In-Line Defect Inspection

KLA-Tencor Defect Inspection Tool

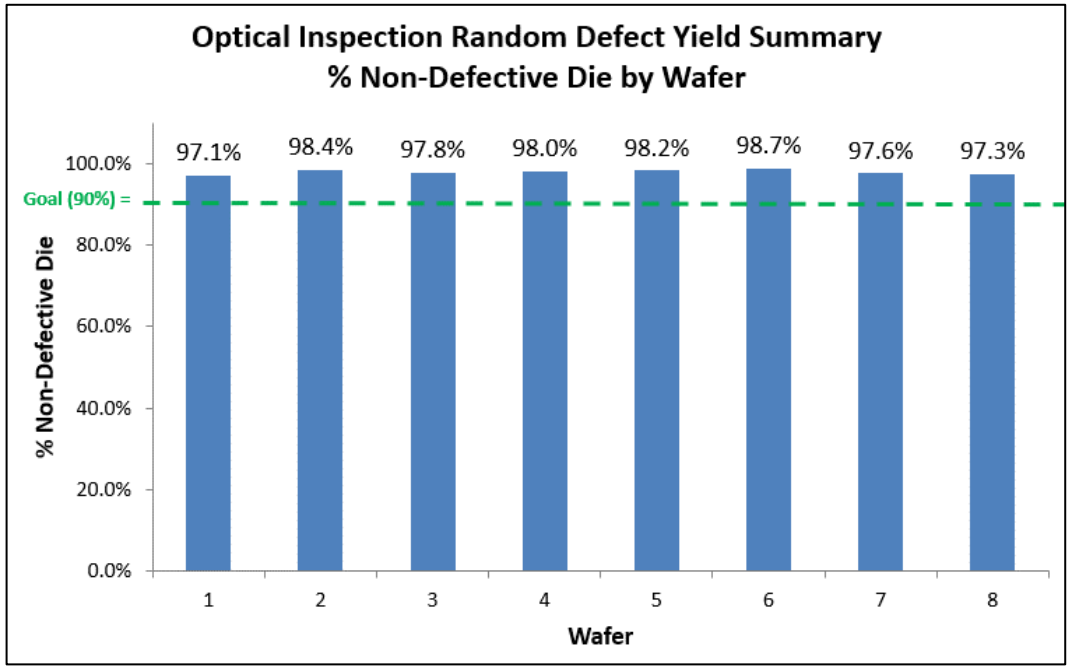
50 wafers/h throughput

- **Bright field: Litho and etch defects**
- **Dark field: Particles & polish defects**



~ 100 nm smallest defect detection (Dark Field)

SFQ5A4 MPW Run (2021)



- **SFQ5ee defect-free chip yield typically exceeds 90% for all wafers (as observed on active circuit area)**
- **Interconnect layer defect density (wafer average per layer) ~ 0.03 defects/cm^2**
- **SFQ5ee wafer average killer defect density ~ 0.3 defects/cm^2**

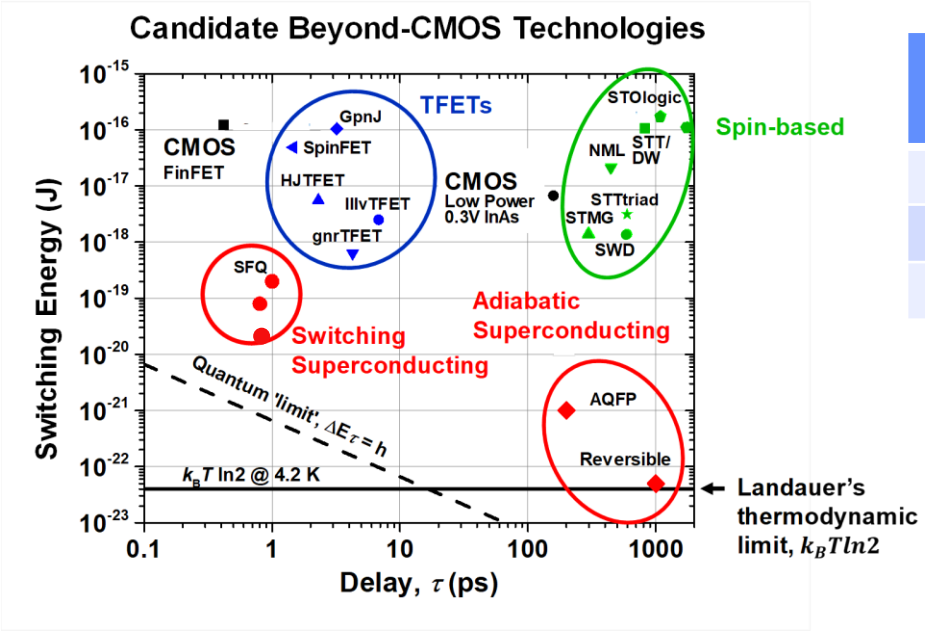
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Partners & Sponsors Utilizing MIT-LL SCE Fab Research Foundry

More than 700 publications reference the MIT-LL SFQ5ee fabrication process node

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

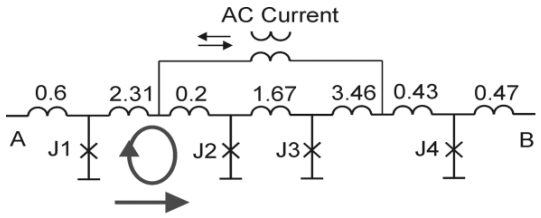
Superconducting Electronics (SCE) for Low-Energy Digital Computation



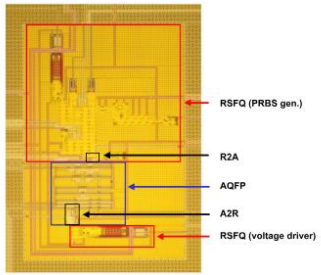
Logic Element	5-nm CMOS FinFET	SCE AQFP	Energy Ratio CMOS / SCE	
			w/o cooling	w/cooling
4-bit Adder	8*10^-15 J	8*10^-20 J	~10^5	~10^2
4-bit Multiplier	4*10^-14 J	4*10^-19 J	~10^5	~10^2
Data Transfer	10^-13 J/b	10^-19 J/b	~10^6	~10^3

- <u>Lowest energy</u> per digital bit operation
  - Adiabatic Quantum Flux Parametron (AQFP): ~10^-21 J
- <u>Highest clock rate</u> in digital circuits
  - Single Flux Quantum (SFQ): >100 GHz
- <u>Nearly lossless data transmission</u>: 10^-19 J/bit
- Operates in closed-cycle cryocooler at 4K

Example Schematic

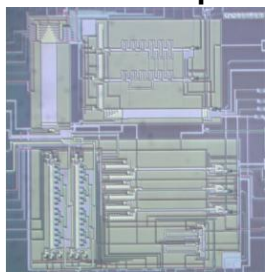


SFQ5ee AOFP/SFO interface



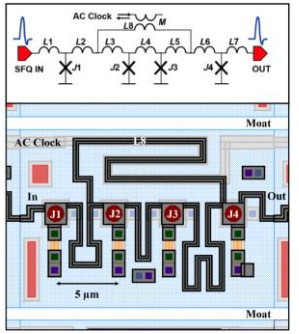
YNU & Hypres, Inc

SFQ data transmission test chip



Hypres, Inc

MIT-LL Shift Register ~1M JJs

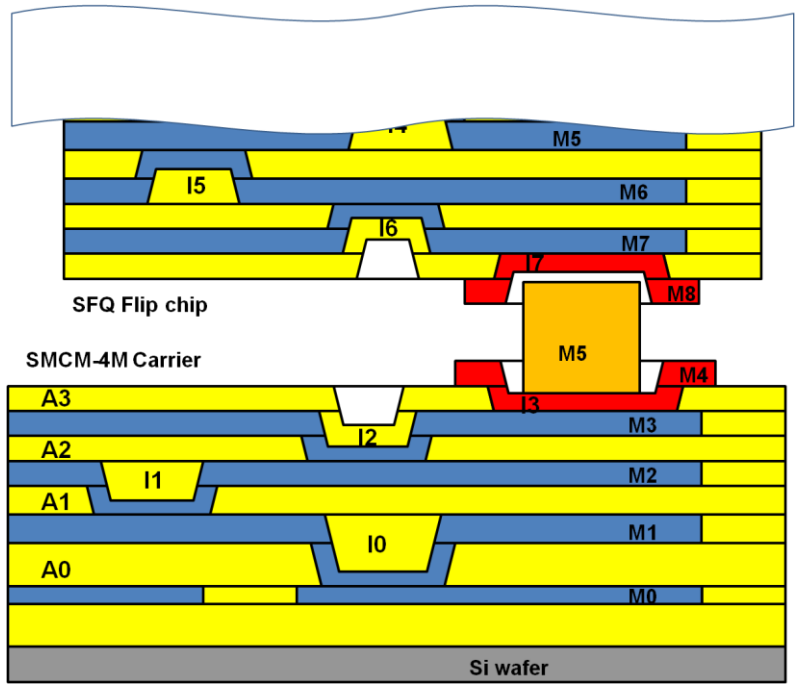


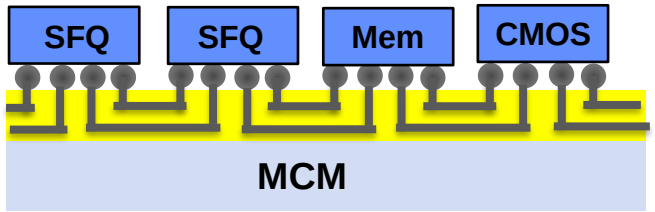
Superconductor electronics (SCE) is the lowest energy of all beyond-CMOS technologies for digital computation

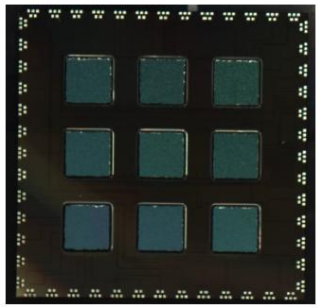
See also: Chen et al, Nature Scientific Reports (2019)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

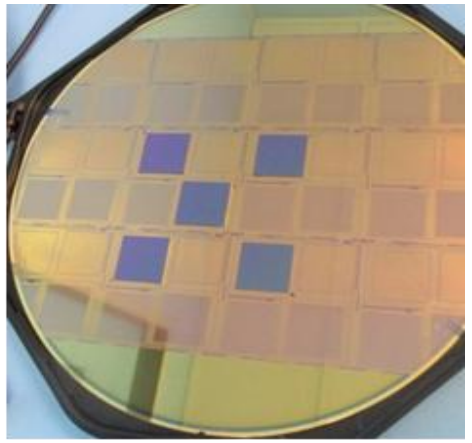
Flip-Chip Superconducting MCM Packaging







9-chip (Northrop Grumman RQL) on S-MCM assembly IARPA C3 Program



Wafer-scale S-MCM witn 800-nm minimum linewidth (utilizing stitching)

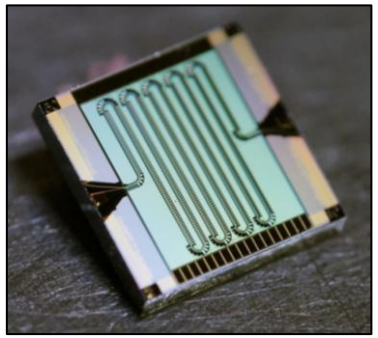
- **Flip-chip attachment of SFQ (and other) chips to S-MCM carriers**
- **Provides controlled-impedance transmission lines between chips**
- **Indium bumps: down to 5 μm pitch**
- **32 mm x 32 mm MCM size (up to 5 cm by 5 cm possible)**

See also: Das et al, Nature Scientific Reports (2023)

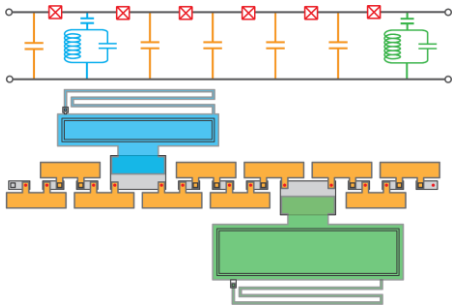
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Traveling-Wave Parametric Amplifiers (TWPAs) for Superconducting Qubit Diagnostics

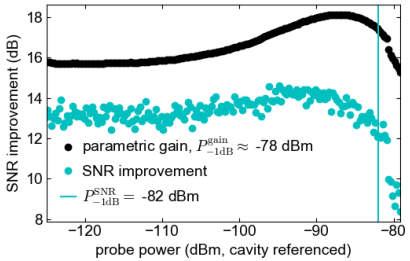
Research and Development for TWPAs



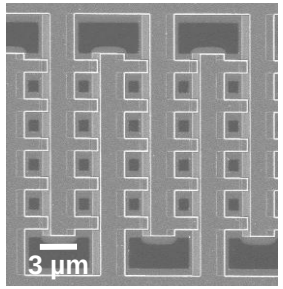
"OG" MIT LL JTWPA [1]



Dual-pumped JTWPA for broadband two-mode squeezing [2]



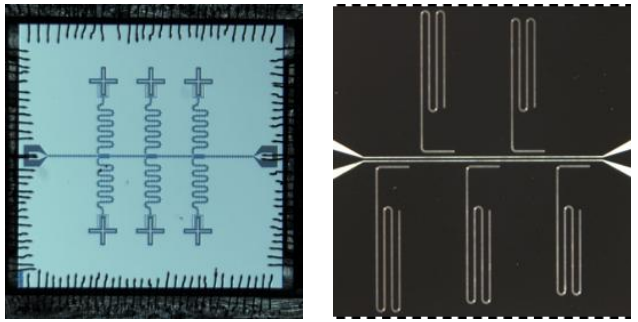
High-Dynamic Range JTWPAs



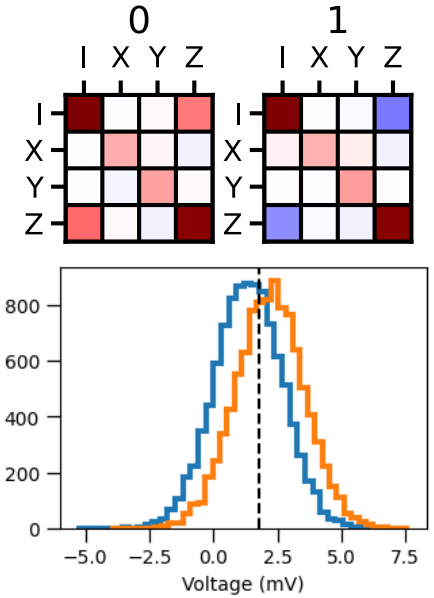
Low-Loss Parallel-Plate Capacitors

Floquet-Mode JTWPA [3]

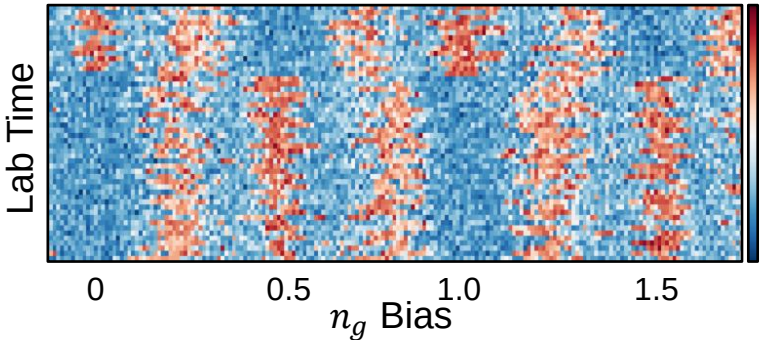
TWPAs for Research and Development



Candle qubits/witness resonators: >1,000 characterized per year



QCVV protocols for mid-circuit measurements



Single-shot measurement-based discrimination between charge offset drift and parity jumps

[1] Macklin, O'Brien, Hover, Schwartz, et al., *Science* 350(6258) (2015)
[2] Qiu et al., *arXiv:2201.11261* (2022)
[3] Wang*, Peng*, et al., *arXiv:2503.11812* (2025)

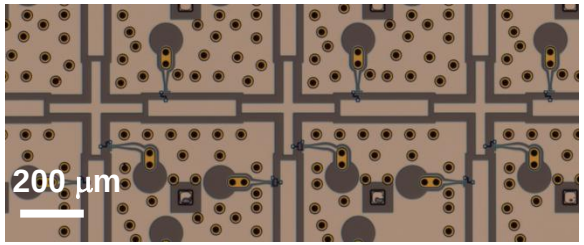
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

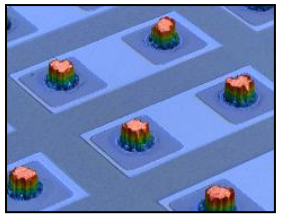
Heterogeneous Multi-Tier Qubit Integration Platform

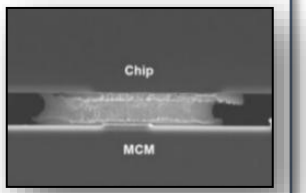
Incorporates Nb Routing based on SFQ5ee node

Superconducting Qubits

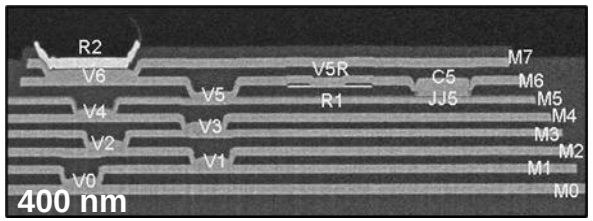


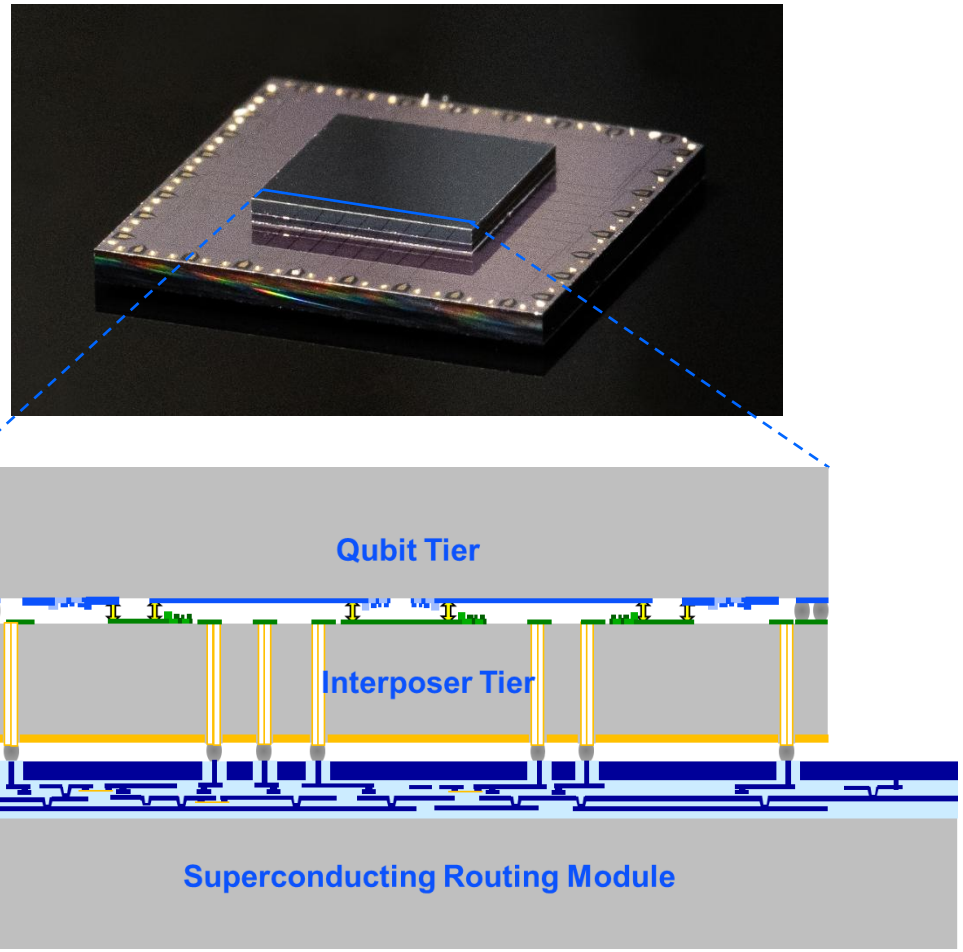
Indium Bump Interconnects



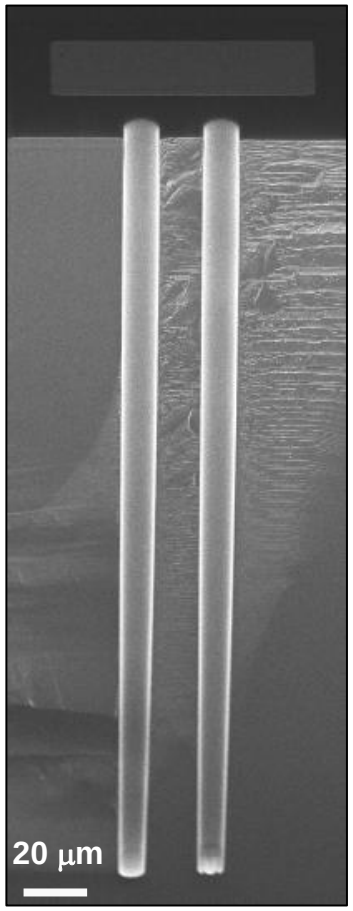


Multilayer Niobium Routing





Through-Silicon Vias



Multi-tier stacks aim to enable high connectivity while maintaining qubit coherence

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Superconducting mm-Wave Filters in SFQ5ee
U Waterloo

Millimeter-Wave Ultra Wideband Multilayer Superconducting Filter

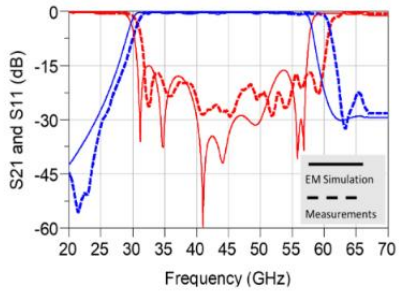


Fig. 12. Simulation and measurement results.

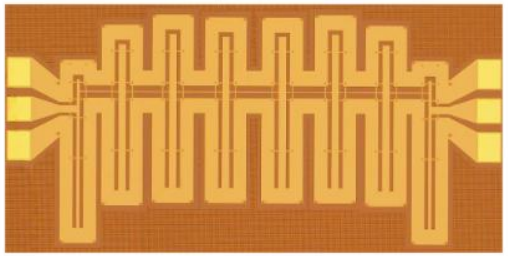


Fig. 2. Photo of the fabricated multilayer superconductor filter.

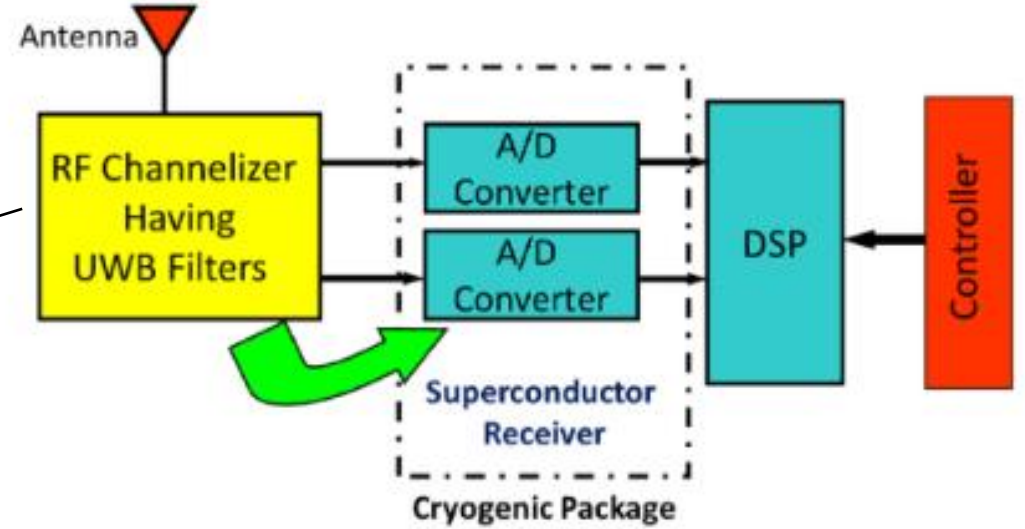


Fig. 1. Schematic block diagram of superconductor digital receiver.

Coplanar Waveguide (CPW) 8-pole design (0.9 x 2.2 mm^2)
Fabricated at MIT-LL in the SFQ5ee process (no JJ's)

Mansour, *IEEE Microwave Magazine* (June 2025)

Jia and Mansour, *IEEE Trans. Appl. Superconductivity* 29 (2019)

UNIVERSITY OF WATERLOO

Office of Naval Research ONR Science & Technology

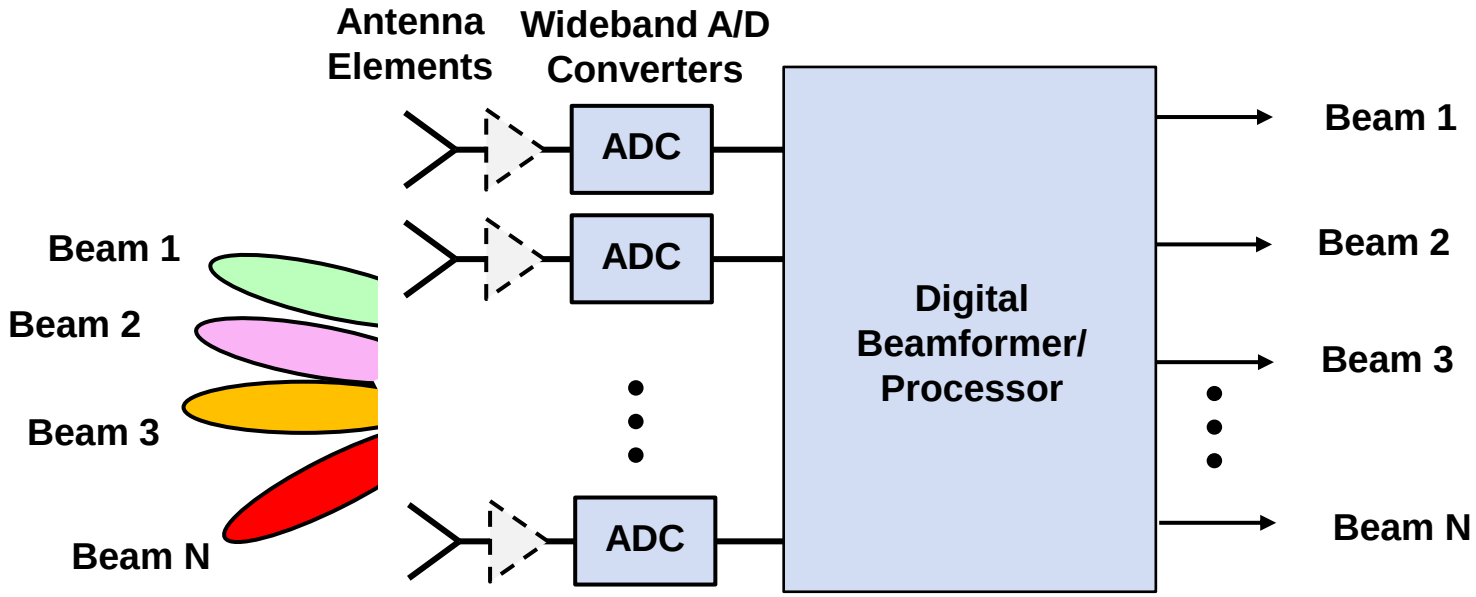
SCE fabrication processes (SFQ5ee) enable integration of passive microwave/mm-wave elements with active circuits

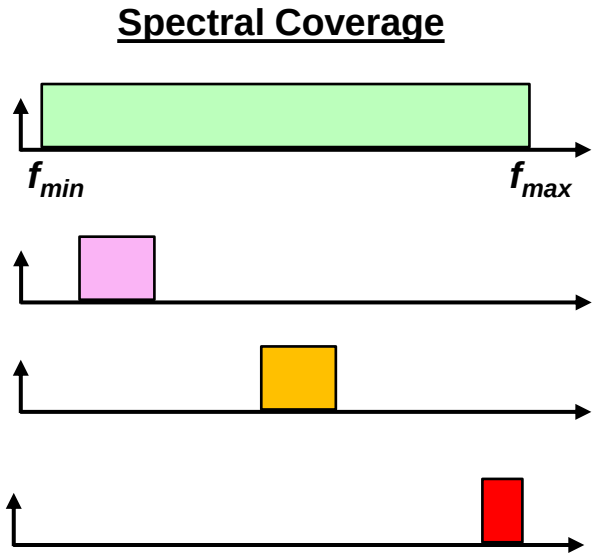
Outline

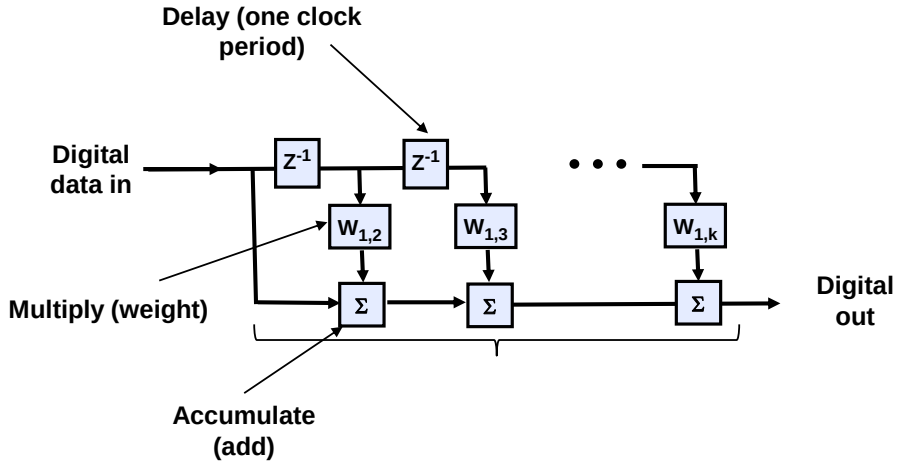
- Overview of MIT Lincoln Laboratory SCE integrated circuit foundry
- SCE digital logic applications and motivation for advanced process nodes
  - In context of continuing advances in digital CMOS technology
- Advanced process node development (SFQ7ee)
  - Emphasis on increasing SCE circuit density
    - Compact kinetic inductors
    - Self-shunted Josephson junctions
- Flux-trapping diagnostics and mitigation

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Multi-Beam Multi-Function Digital Array Sensor/Receiver for Wideband RF/mm-wave Systems







- Digital arrays offer highly agile independent beams
- Digital processing dominated by multiply/accumulate operations (FIR filtering)
  - Often with modest memory requirements
- Increasing energy efficiency of digital process enables wideband & high-beam-count systems
- Need for low-power (including cooling) digital processors with >10's petaFLOPS performance

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Ongoing Advances in Si CMOS Digital Logic

SPECIAL SECTION TRANSISTORS

REVIEW

Toward attojoule switching energy in logic transistors

Suman Datta[1,2]*, Wriddhi Chakraborty[2], Marko Radosavljevic[3]

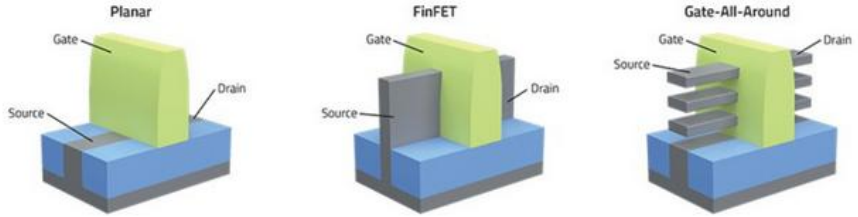
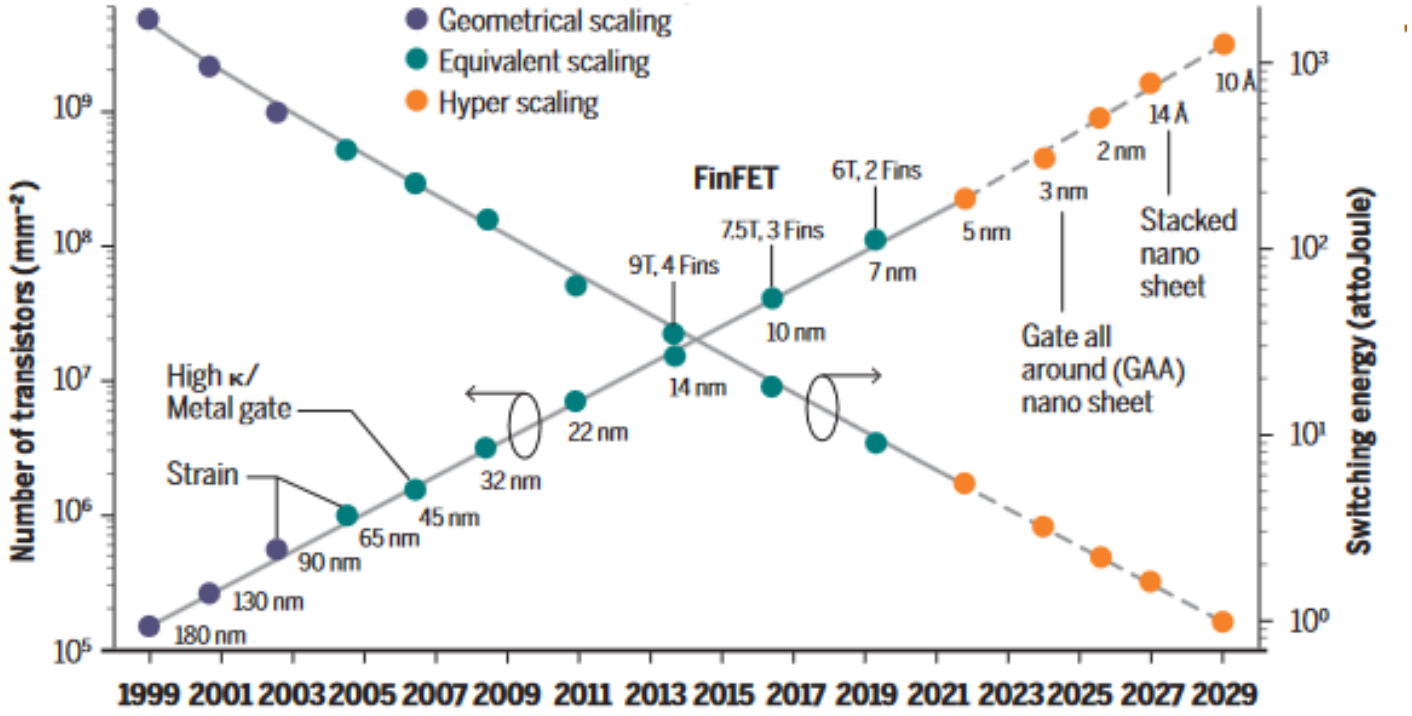


Fig. 1: Planar transistors vs. finFETs vs. gate-all-around Source: Lam Research

TSMC's 2nm N2 process node enters production this year, A16 and N2P arriving next year

News By Anton Shilov published April 24, 2025 tom's HARDWARE

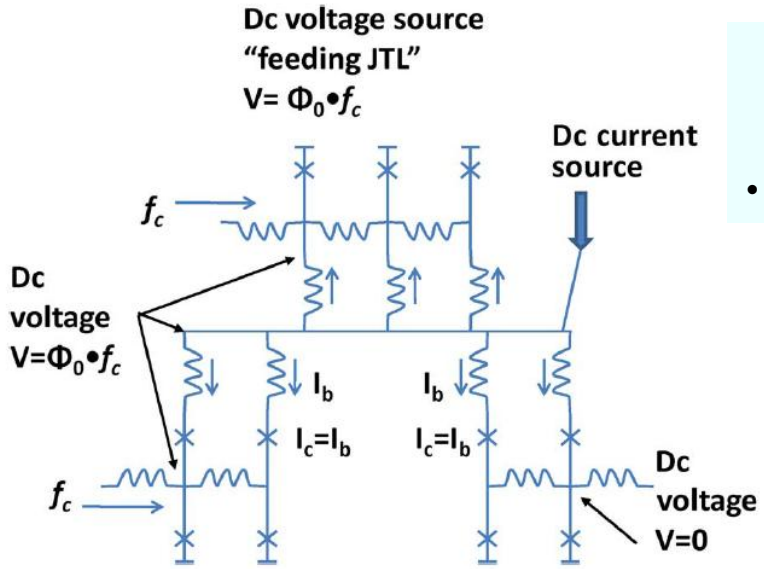
Datta *et al.*, *Science* **378**, 733–740 (2022) 18 November 2022



While logic transistor switching energy continues to decline, energy per OP in logic circuits and processors will likely be dominated by other factors (interconnects, etc.)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

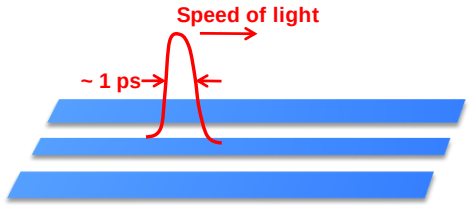
SFQ Logic Families



Energy-Efficient RSFQ (ERSFQ)

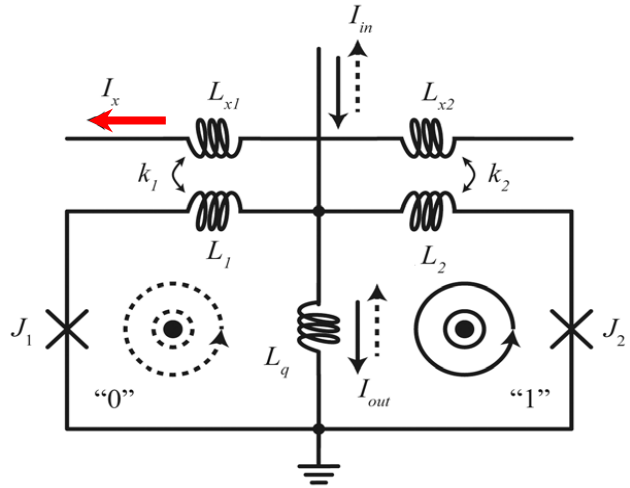
- Eliminates resistor-based bias network

Lossless SFQ data transmission



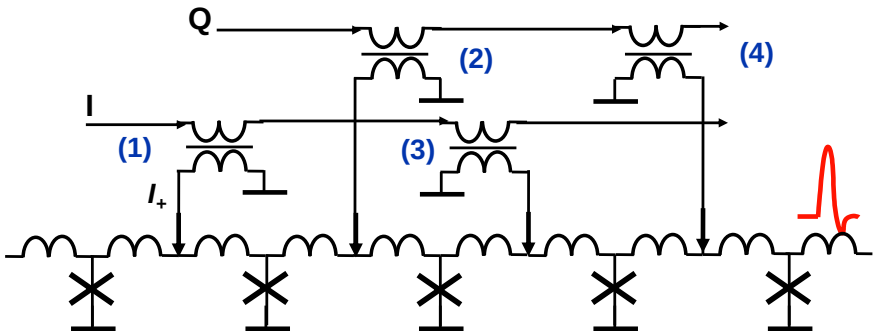
Adiabatic Quantum Flux Parametron (AQFP)

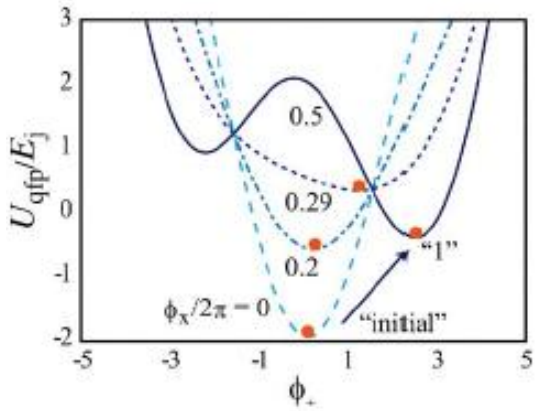
- JJs do not 'switch'



Reciprocal Quantum Logic (RQL)

- Developed by Northrop Grumman
- Based on AC biasing





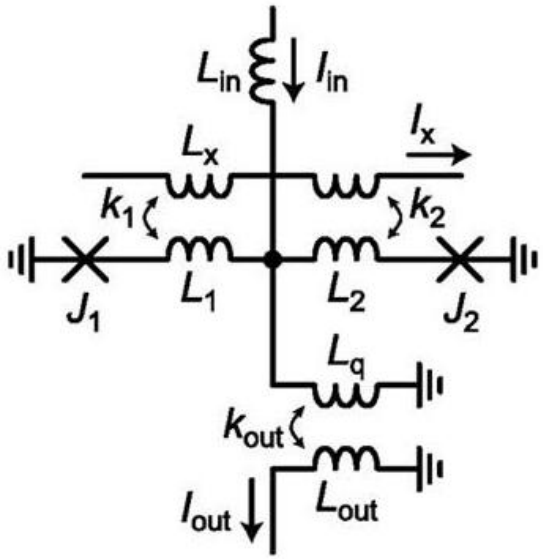
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

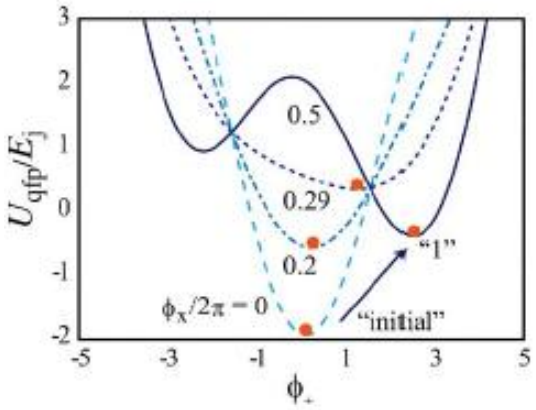
AQFP Energy Dissipation

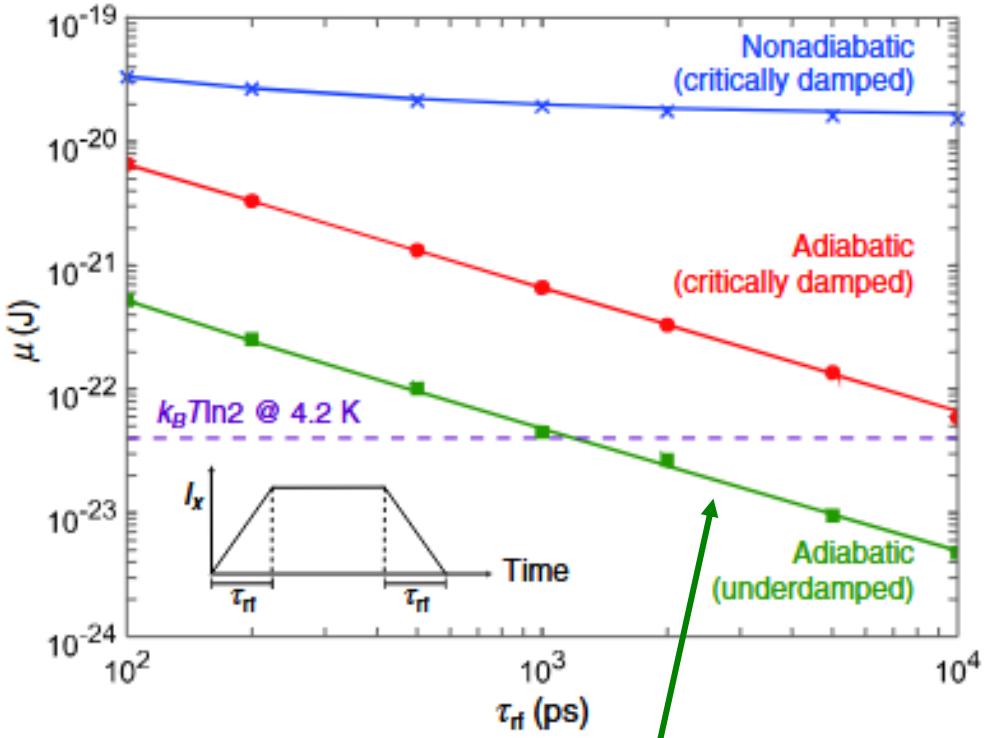
PHYSICAL REVIEW APPLIED 4, 034007 (2015)

Thermodynamic Study of Energy Dissipation in Adiabatic Superconductor Logic

Naoki Takeuchi,[1,*] Yuki Yamanashi,[1,2] and Nobuyuki Yoshikawa[1,2]
[1]*Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*
[2]*Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*
(Received 17 June 2015; revised manuscript received 28 June 2015; published 24 September 2015)







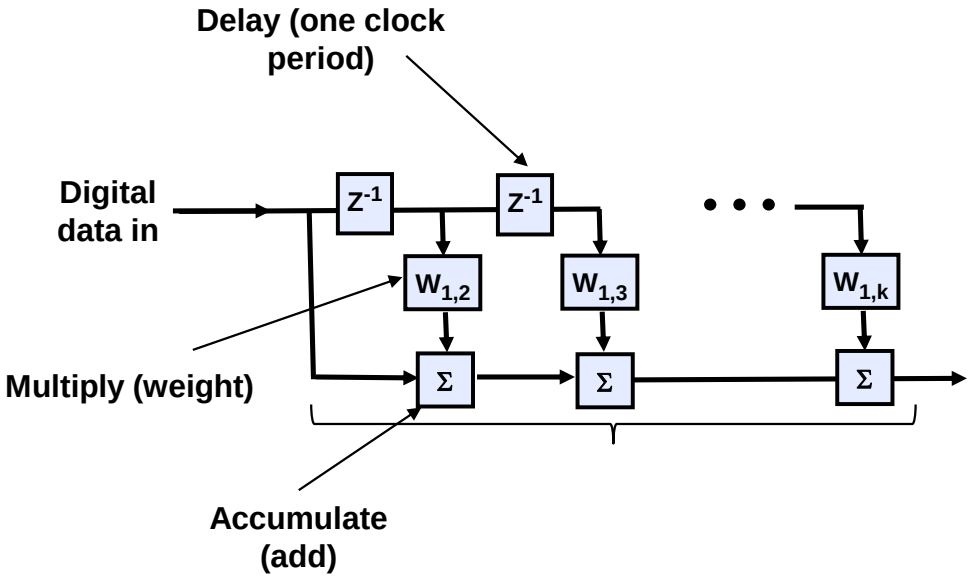
$$\beta_L = \frac{2\pi I_{CJ} L_2}{\Phi_0} = 0.2 \qquad \beta_q = \frac{2\pi I_{CJ} L_q}{\Phi_0} = 1.6$$

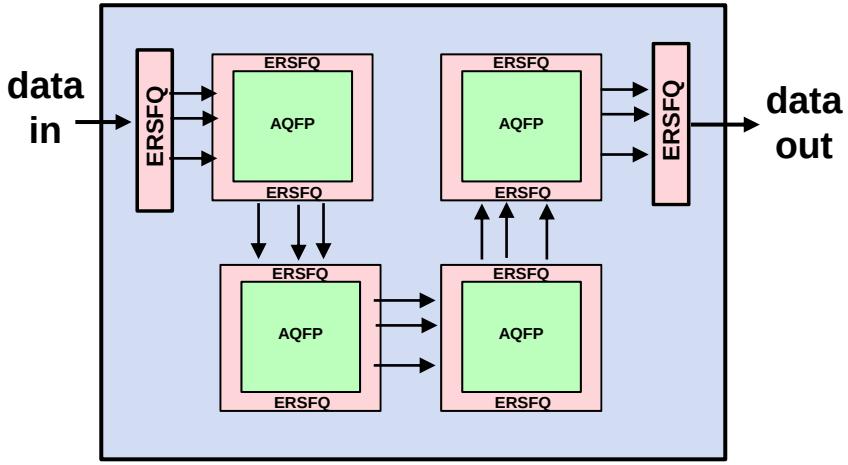
$I_{CJ} = 50\ \mu A$ **No external shunt resistor**

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

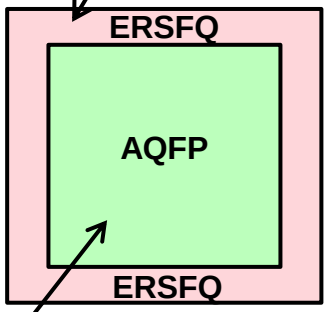
Dataflow FIR Filter

Hybrid ERSFQ/AQFP Superconducting Electronics

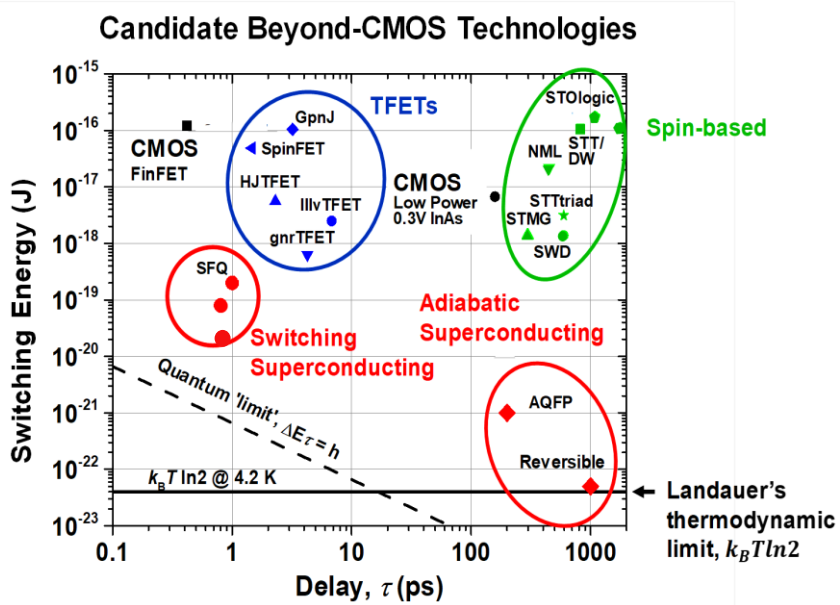


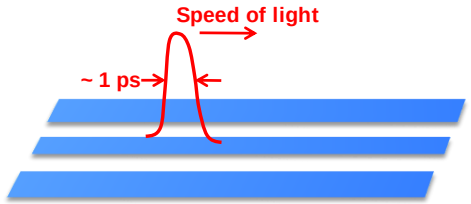


ERSFQ circuitry (as needed) for high-speed low-energy data transmission and interfaces



AQFP circuitry for low-energy digital computation





SFQ pulse ballistic data transport on superconducting transmission line

[1] Hironaka, Meher, Ayala et al., *IEEE Trans.Appl. Supercond.* 33 (1301905) (2023)
[2] Ayala et al, *2023 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (2023)*

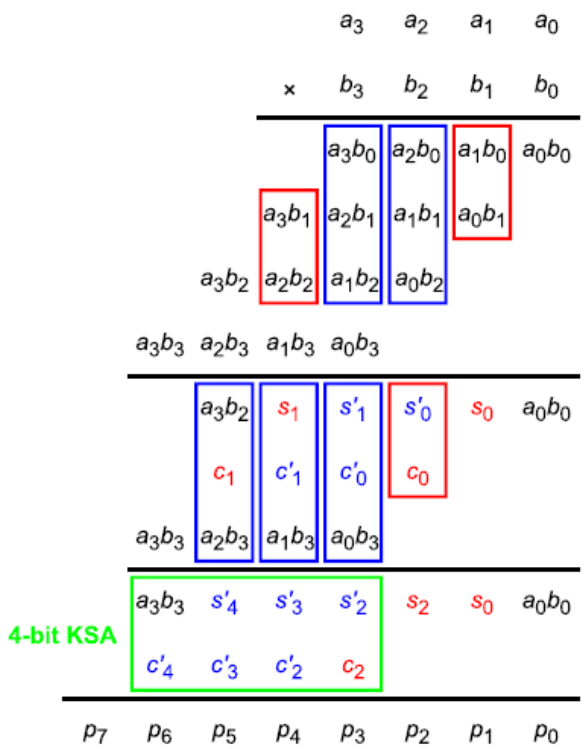
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Demonstrated AQFP Multiplier (2025)

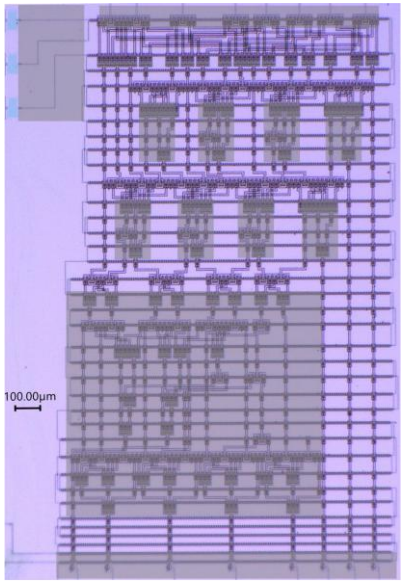
Yokohama National University (YNU)

- **Design & demonstration of Array and Wallace-Tree multipliers**
  - **AIST 10 kA/cm^2 high-speed standard fabrication process**

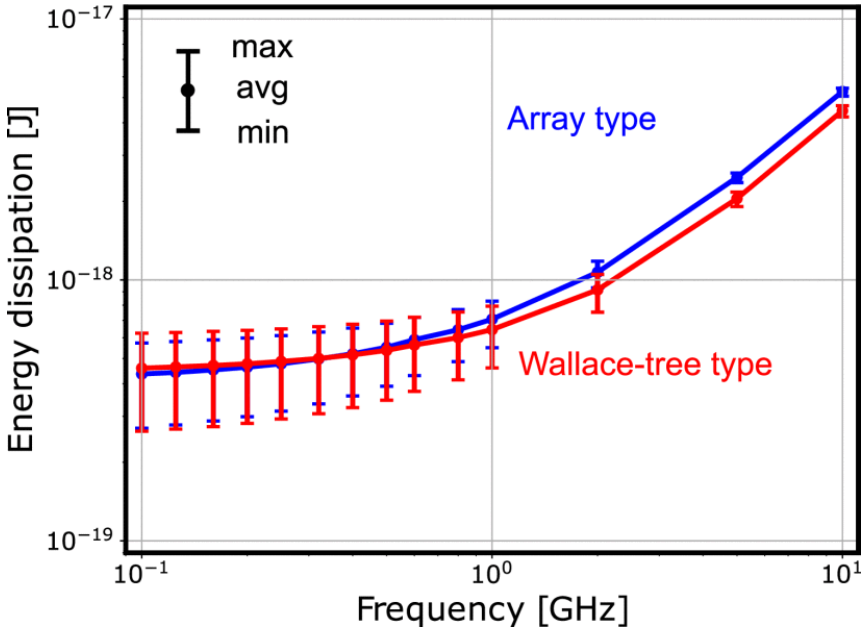
Wallace-tree multiplication



Wallace-tree multiplier chip



1624 JJs
1.6 x 2.5 mm



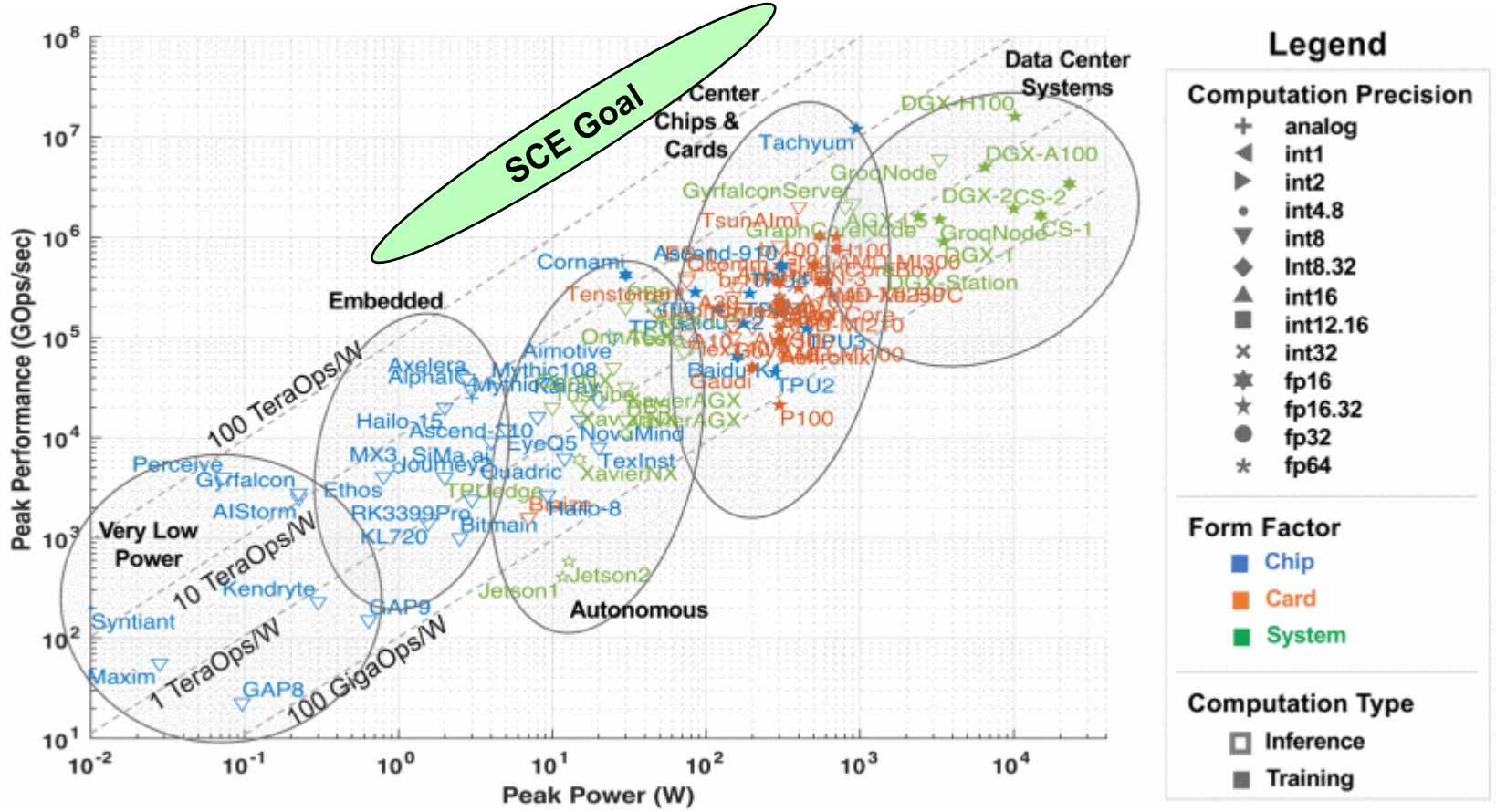
Multiplier energy ~6x10^-19 J @ 1 GHz

[1] Hoshika,Takagi, Ayala et al., *IEEE Trans. Appl. Supercond.*. 35(1) (2025)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

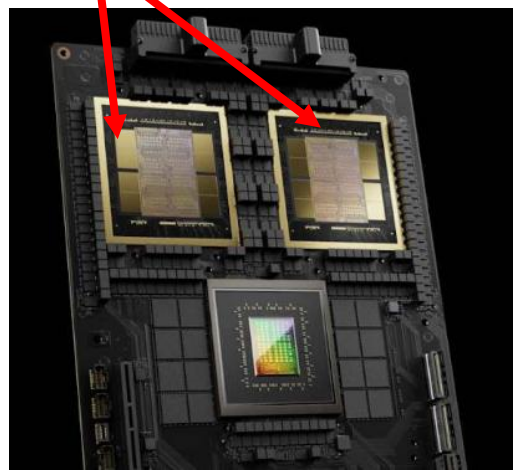
Lincoln AI Computing Survey (LAICS)

Reuther et al, MIT Lincoln Laboratory
Presented at 2023 IEEE High Performance Extreme Computing Conference (HPEC)



NVIDIA GB200 Superchip (2024)

Two Blackwell GPUs
208B Transistors



20 petaFLOPS @ 2700 W
~ 10^-13 J/FLOP
10 TOPS/W

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

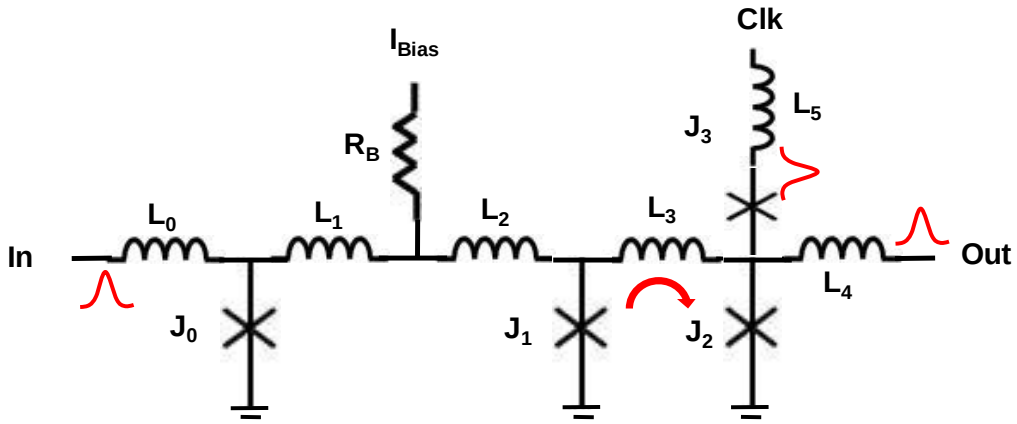
Outline

- Overview of MIT Lincoln Laboratory SCE integrated circuit foundry
- SCE digital logic applications and motivation for advanced process nodes
  - In context of continuing advances in digital CMOS technology
- Advanced process node development (SFQ7ee)
  - Emphasis on increasing SCE circuit density
    - Compact kinetic inductors
    - Self-shunted Josephson junctions
- Flux-trapping diagnostics and mitigation

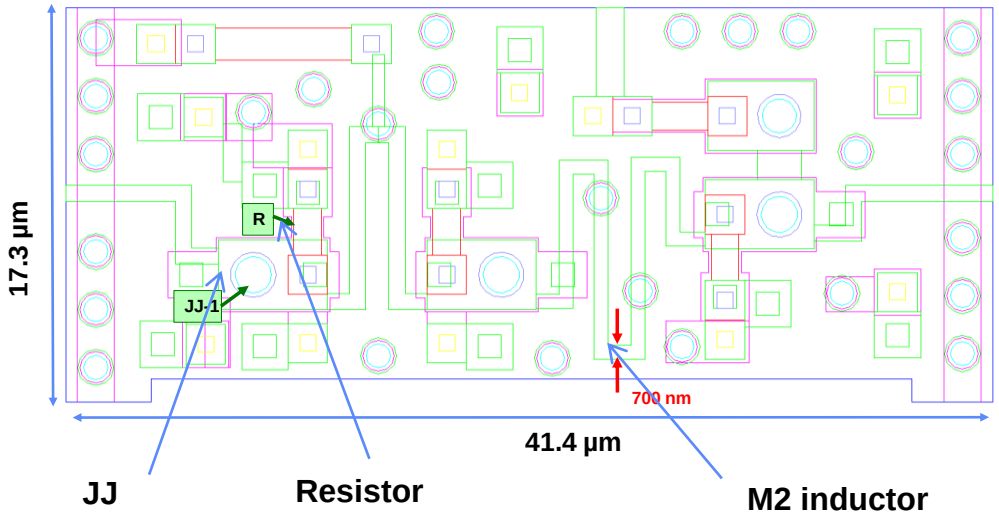
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

SFQ D flip-flop (DFF)

Example layout for 4-layer process (circa 2013)



SFQ storage loop



$$Flux\ quantum\ \Phi_0 = h/2e \approx 2\ mV\ ps$$

$$E \approx I_C \Phi_0 \sim 10^{-19}\ J$$

- Reducing I_C lowers switching energy, but min I_C limited by thermal error rate
- Min I_C typically 10's µA

$$LI_C \sim \Phi_0$$

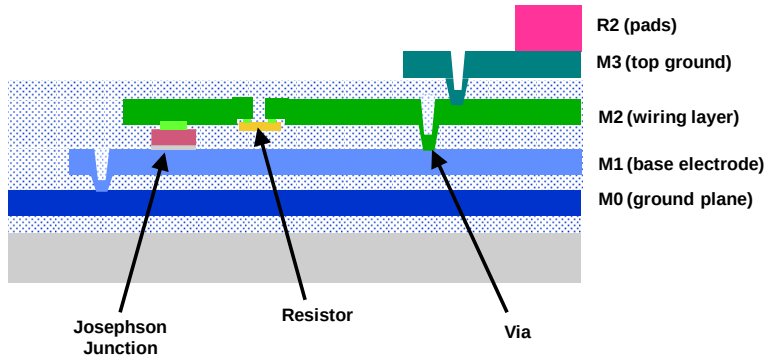
- Lower I_C calls for larger L's
- Implications for circuit density
- Geometric inductance per unit length varies inversely with linewidth

I_C's ~ 100 µA

L's ~ 5 pH

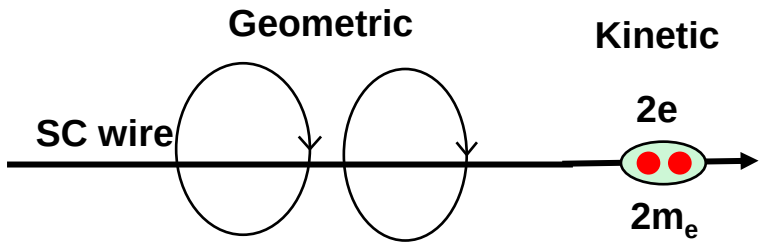
Legacy fab process

For min 700 nm linewidth:
L ~ 0.2 pH/µm (geometric)
~1M JJs/cm²

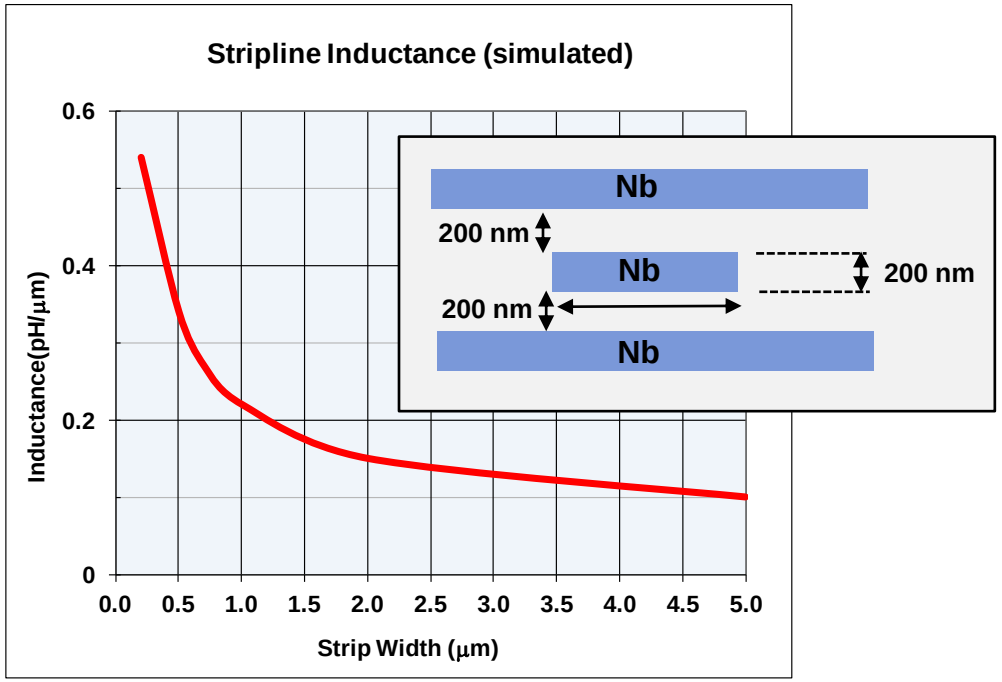


IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Inductance in Superconducting Wires

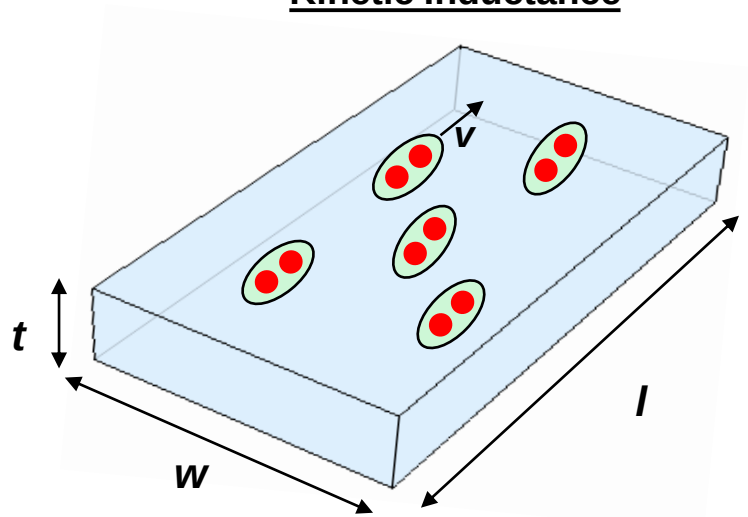


Geometric Inductance



Geometric inductance increases with decreasing linewidth.

Kinetic Inductance



- **Superconducting current: 2*e*, 2m_e, velocity *v*, Cooper pair density n_s; Penetration depth: λ**

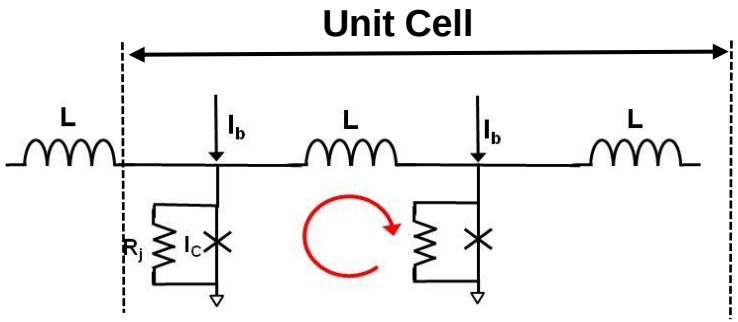
$$\frac{L_K}{l} = \left(\frac{m_e}{2n_s e^2}\right)\left(\frac{1}{tW}\right) = \frac{\mu_o \lambda^2}{tW}$$ **~ 4 pH/μm for NbN**

Kinetic inductance varies quadratically with λ, and inversely with cross-section area.

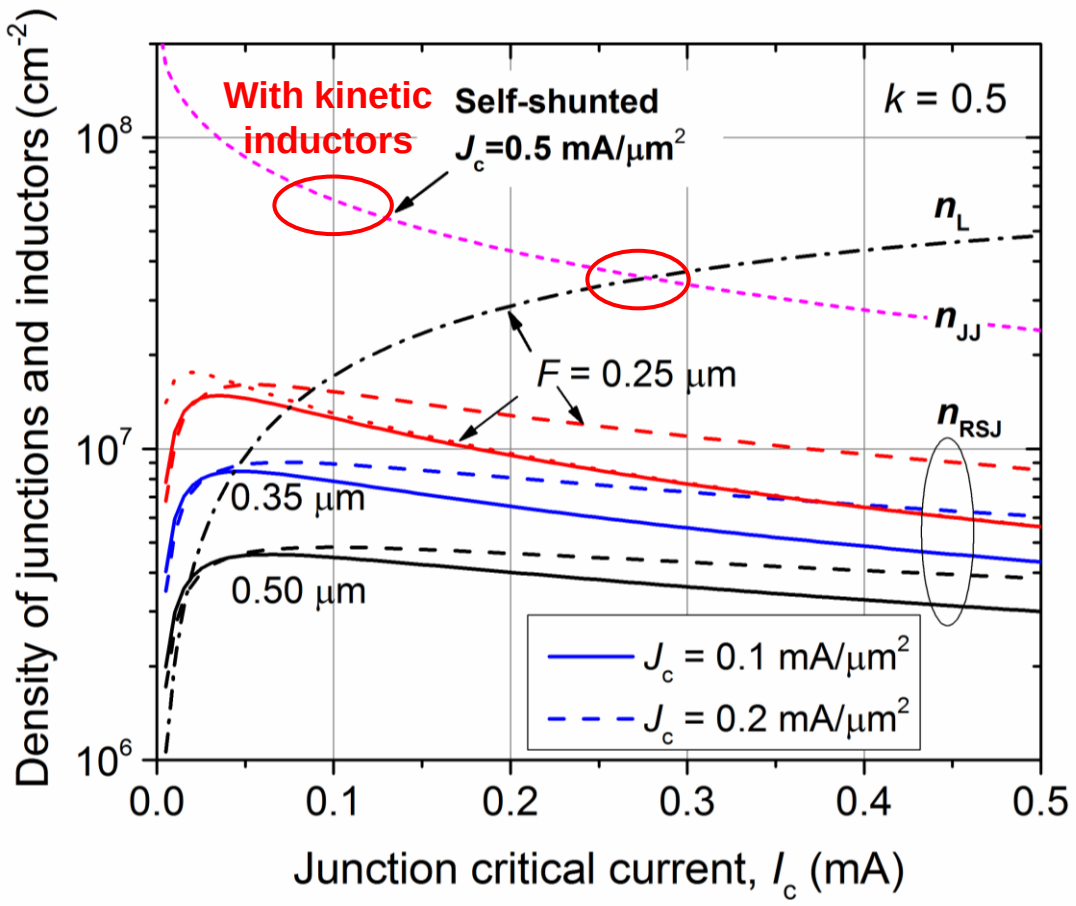
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

SFQ Circuit Density Drivers: Junctions and Inductors Pathway Towards ~ 10^8 JJs/cm^2

- SCE scaling needs to include both Josephson junctions (JJs) and inductors
  - About 1:1 ratio required
  - LI_c~ Const.
- Maximum circuit density when inductor density matches JJ density, $n_L \sim n_{JJ}$
- Reducing minimum feature size F results in more compact geometric inductors
  - Suitable for externally shunted JJs
- Replace geometric inducotrs with kinetic inductors with Lsq ~ 4pH/sq further increases density
  - Combine with self-shunted JJs



Component Requirements for Higher Density SCE Circuits



LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

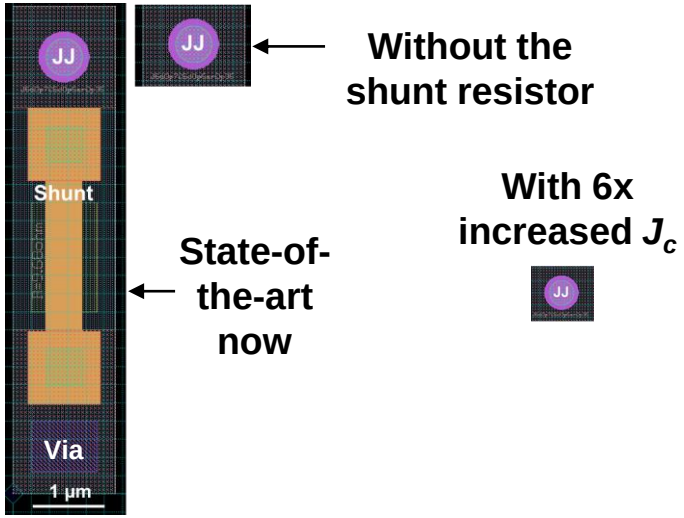
SFQ7ee Process Development Goals

- **Develop advanced materials and fabrication technology for a 10x increase in the integration scale of superconductor integrated circuits**

Three Major Development Areas

Reduce Area of Active Devices - Josephson Junctions (JJs)

- Develop self-shunted JJs with high critical current density (high-J_c) to
  - eliminate resistive shunts
  - reduce the JJ area



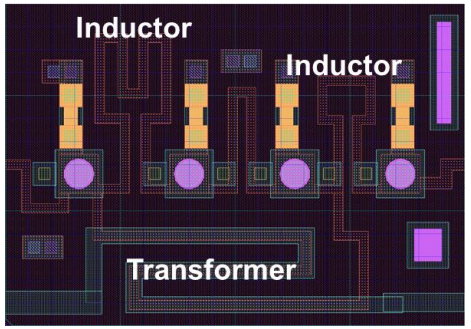
Without the shunt resistor

State-of-the-art now

With 6x increased J_c

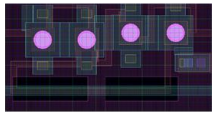
Decrease Area of Circuit Inductors

- Develop kinetic inductors using superconducting NbN and NbTiN thin films instead of Nb geometrical inductors



Shift register cell with Nb inductors: 20 μm x 14 μm

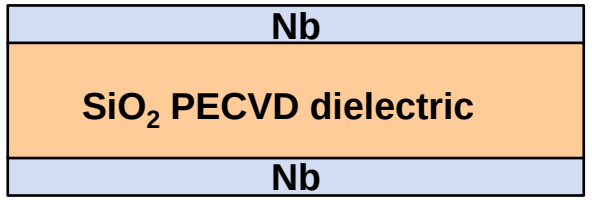
Cell with NbN inductors



9 μm x 5 μm

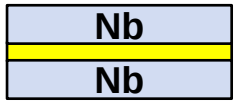
Decrease Linewidth of Data, Clock, and AC Power Transmission Lines

- Develop high-κ, low-loss interlayer dielectric instead of conventional SiO_2



High-κ dielectric Ta_2O_5

50 nm Ta_2O_5 →



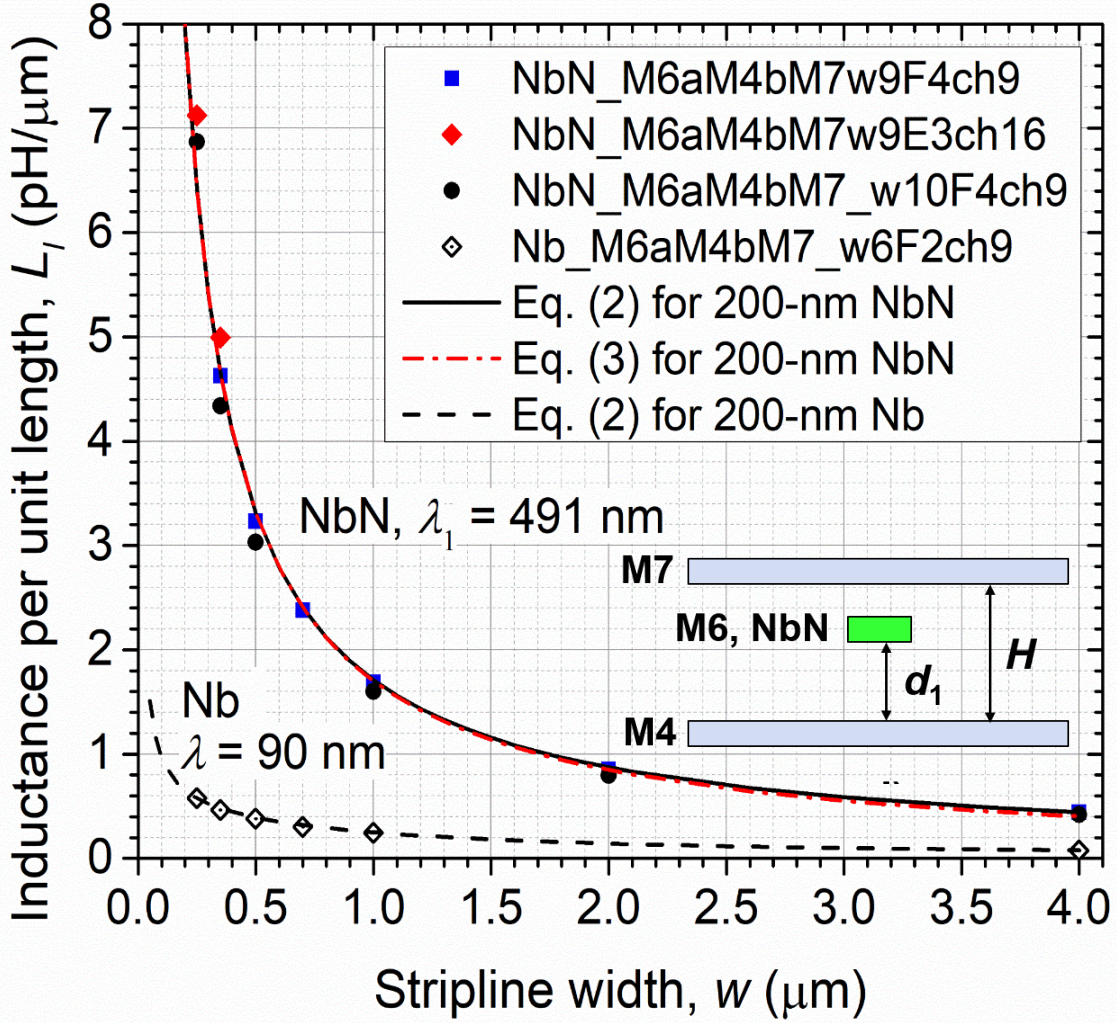
7x – 10x stripline width reduction

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Inductance of NbN (and Nb) Striplines with Nb Ground Planes

$$L_l = \underbrace{\frac{\mu\mu_0}{4\pi}\ln\left(1+\frac{\sin^2\frac{\pi\left(d_1+\frac{t_1}{2}+\lambda\right)}{H+2\lambda}}{\sinh^2\frac{0.2235\pi(w+t)}{2(H+2\lambda)}}\right)}_{\text{Geometric Inductance: dominates for Nb } \lambda \sim 90\text{ nm}} + \underbrace{\frac{\mu_0\lambda_1^2}{t_1 w}}_{\text{Kinetic Inductance: dominates for NbN } \lambda \sim 490\text{ nm}}, \qquad (3)$$



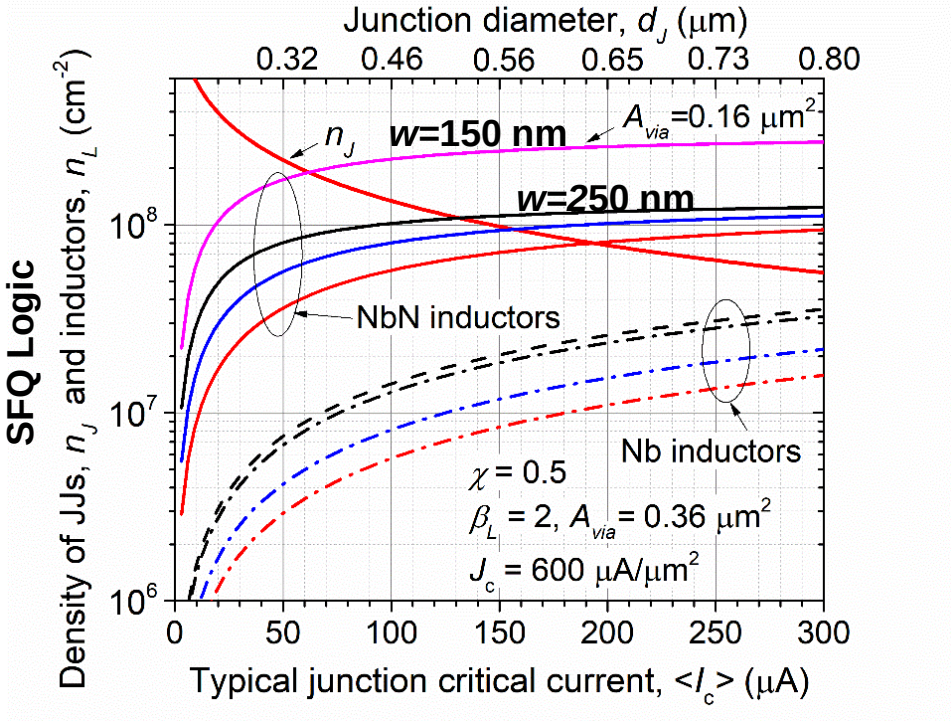
- **Excellent agreement between measurements and model**
- **Determined NbN kinetic inductance: L_K = 1.51 pH/sq**

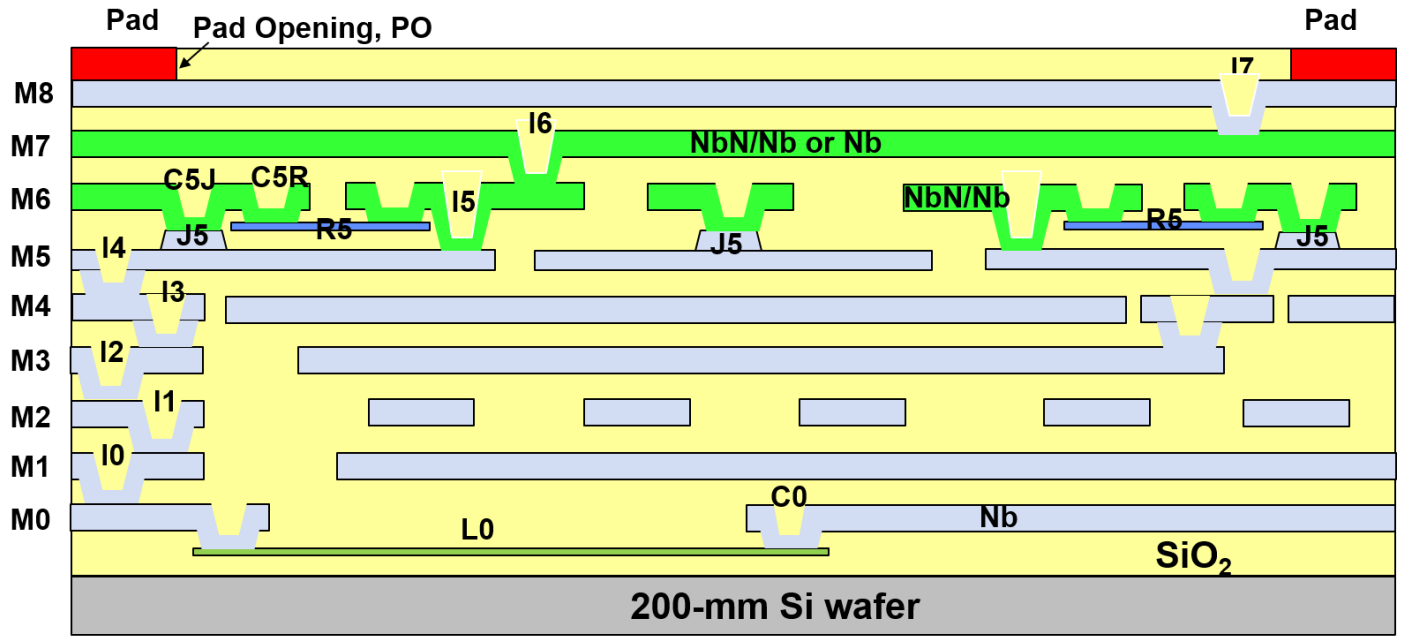
[1] S.K. Tolpygo, E.B. Golden, T. J. Weir, and V. Bolkhovsky, *IEEE TAS*, vol. 32, no. 5, Aug. 2022, Art no. 1400331

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

SFQ7ee Process

SFQ Logic





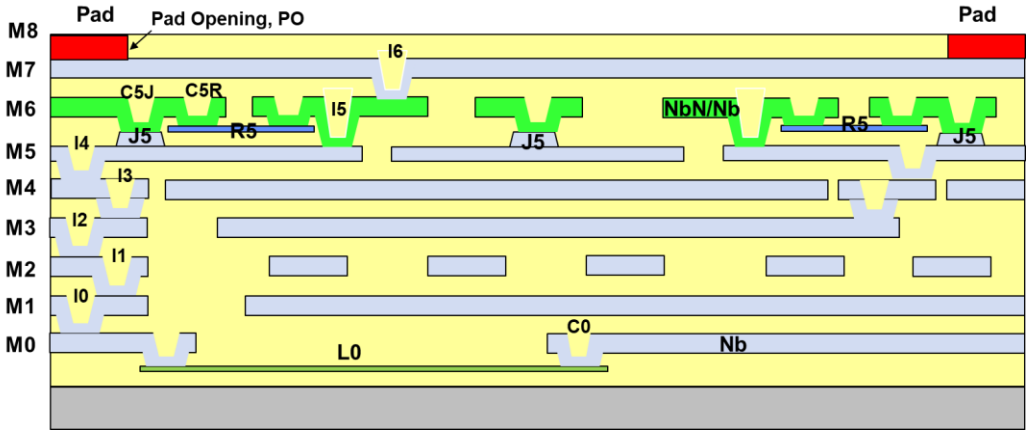
- **Balancing number densities of self-shunted Josephson junctions and inductors requires compact kinetic inductors**
- **Circuit densities ~ 100M JJs per cm^2 are achievable in the SFQ7ee process**
  - **Target J_c = 600 μm/μm^2, self-shunted, d = 400 nm**
  - **One – two layers of kinetic inductors w = 250 nm for logic, and one layer for bias inductors**

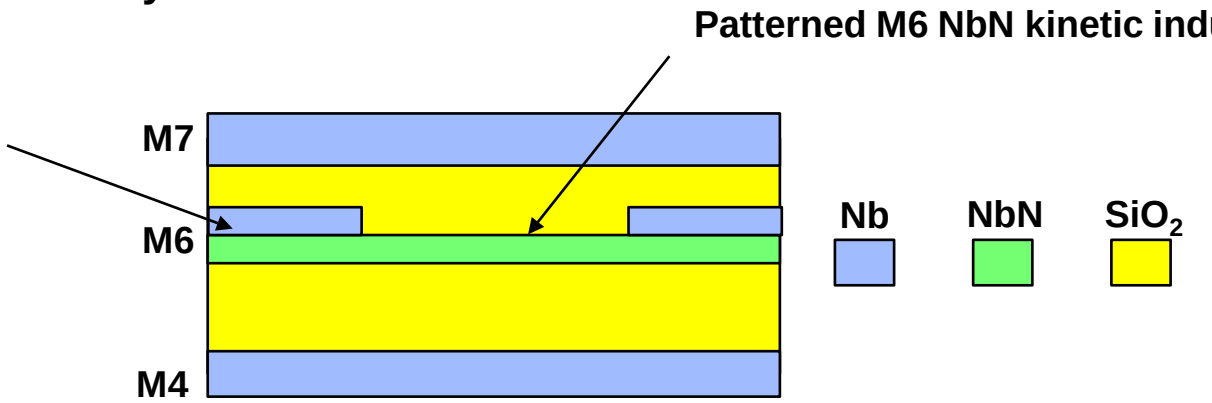
[ref] Tolpygo et al., *IEEE Trans. Appl. Supercond.*. 33 (Article # 1101512) (2023)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Development of Compact Inductors with NbN/Nb Bilayers

- NbN thin films have high kinetic inductance (resulting from large penetration depth λ ~ 490 nm)
  - L_{KI} proportional to λ^2/tw
  - Larger than 200-nm film thickness, thus compromising shielding properties
- Developing alternative approach utilizing NbN/Nb bilayers
- NbN-only regions have high kinetic inductance, tunable over wide range up to 30 pH/μm
- Bilayer inductance is the same as of 100-nm Nb layer – effective for shielding



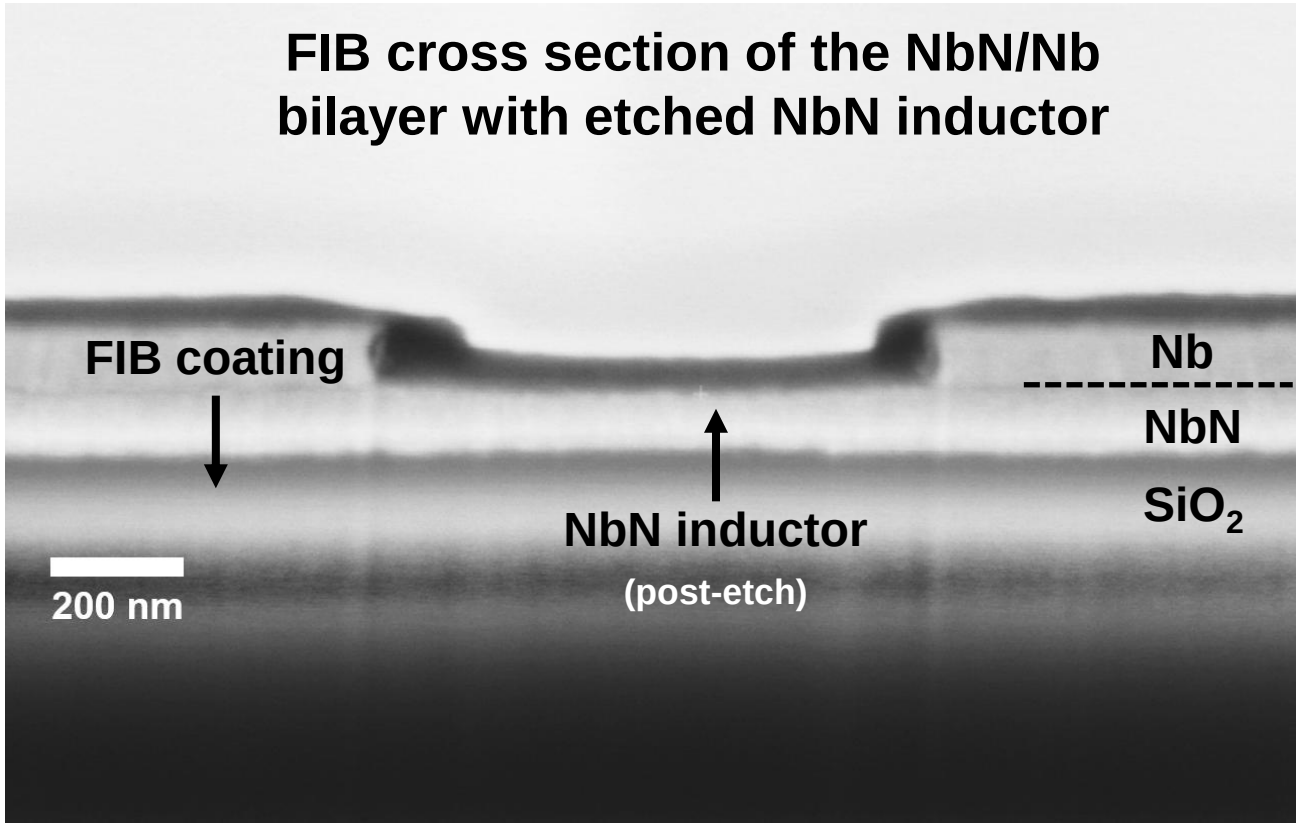


Bilayer behaves electrically as 100-nm-thick Nb layer at 4 K

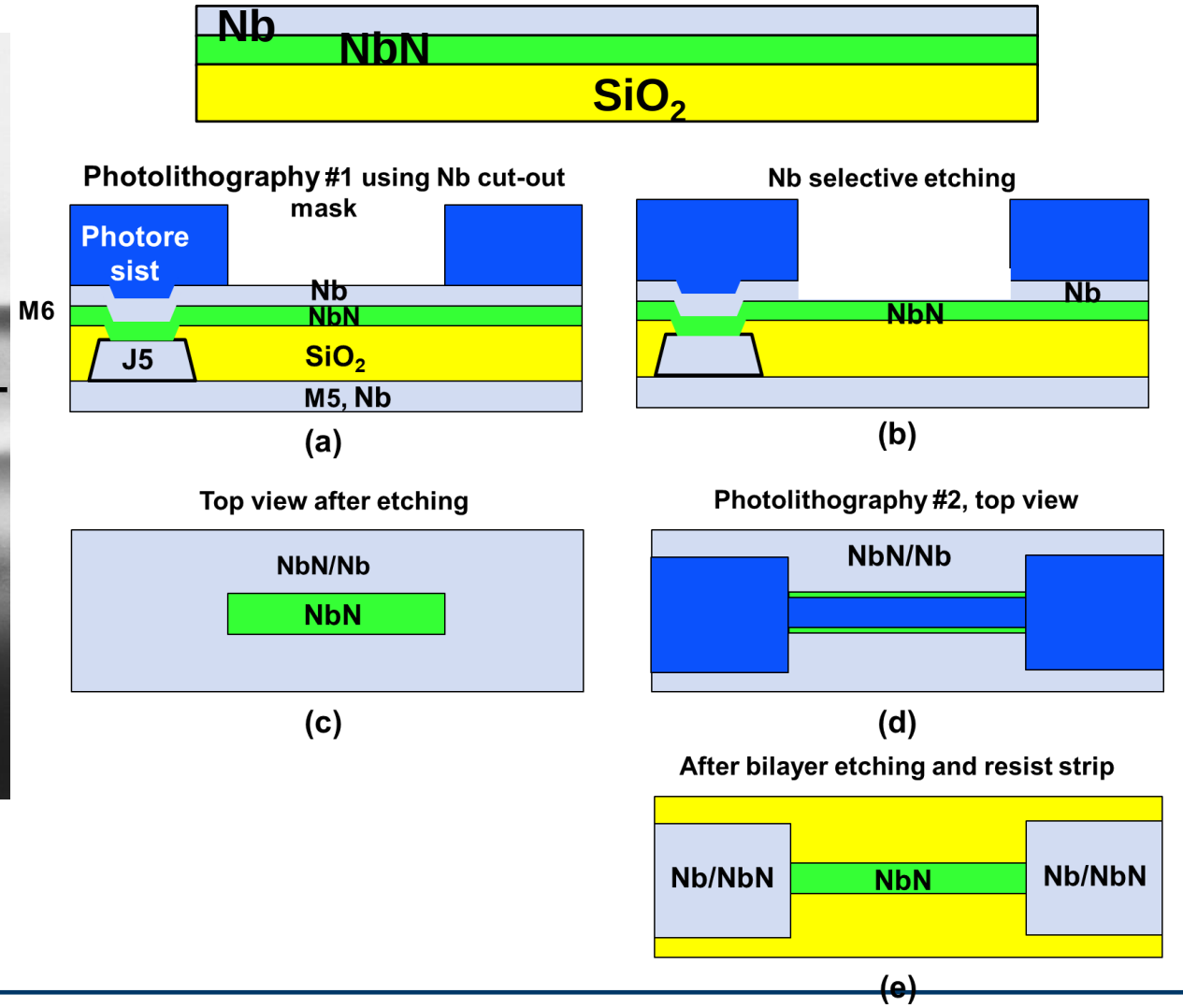
[ref] Tolpygo et al., *IEEE Trans. Appl. Supercond.*. 33 (Article # 1101911) (2023)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Bi-Layers for Circuit Inductors and Transformers



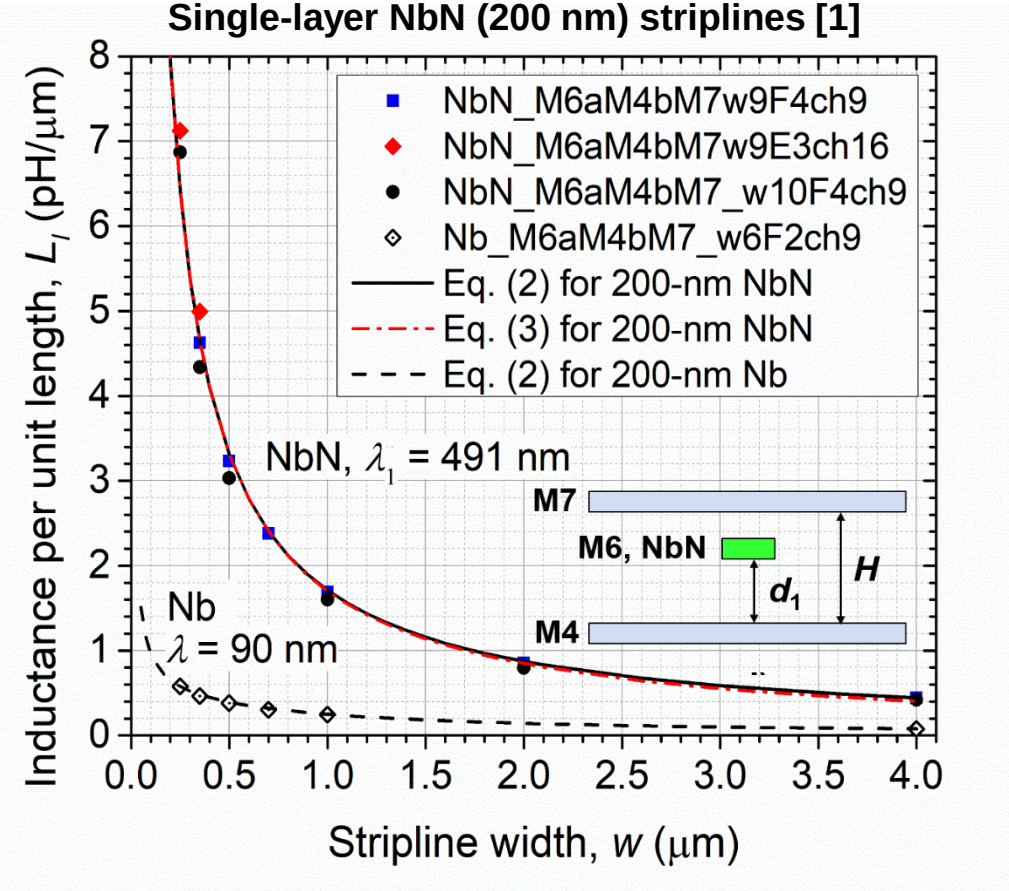
NbN/Nb bilayers as inductor layers

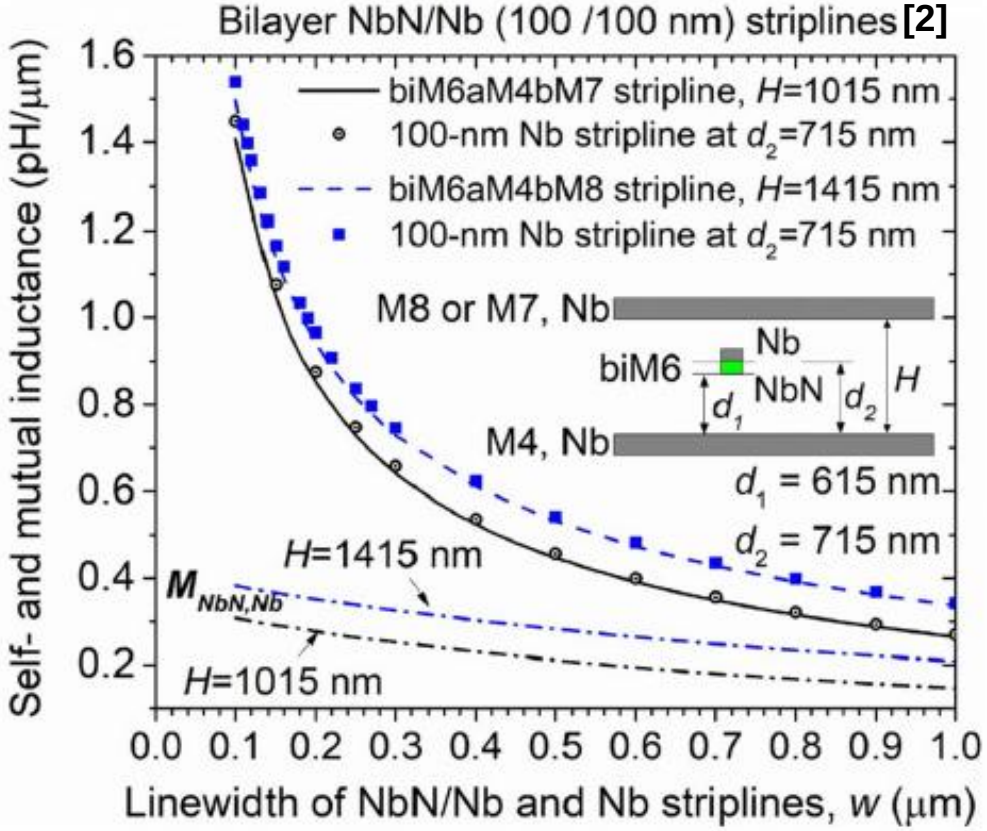


[ref] Tolpygo et al., *IEEE Trans. Appl. Supercond.*. 33 (Article # 1101911) (2023)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Single-Layer & Bilayer Stripline Inductors



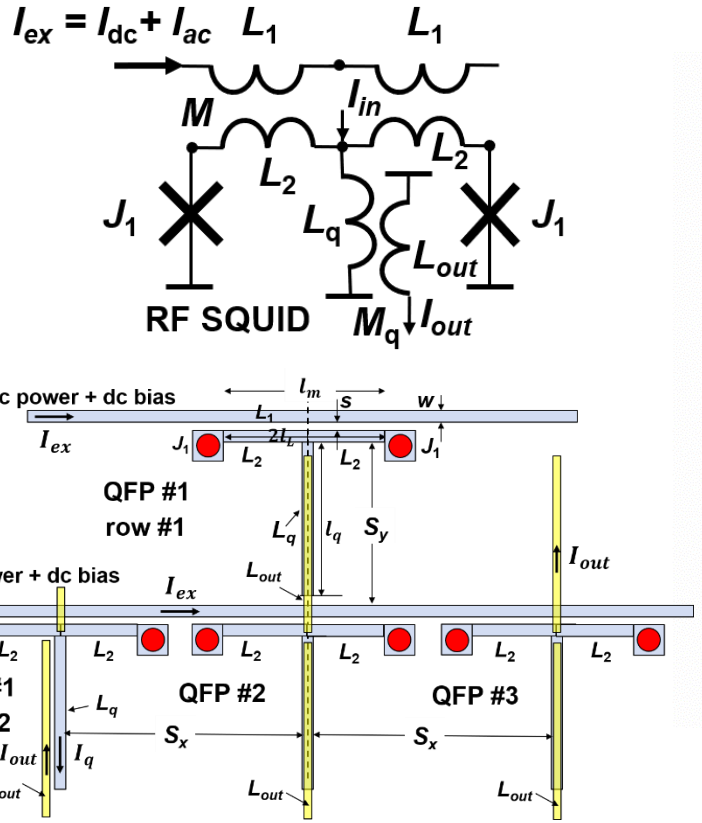


Bilayer (NbN/Nb) striplines dominated by Nb geometric inductance (as expected)

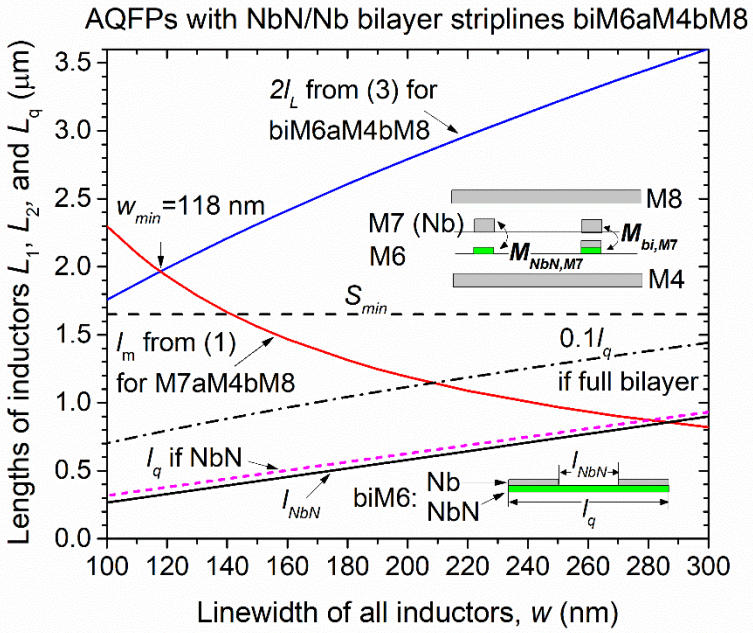
[1] Tolpygo et al., *IEEE Trans. Appl. Supercond.*. 33 (Article # 1101911) (2023)
[2] Tolpygo, *IEEE Trans. Appl. Supercond.*. 33 (Article # 1300419) (2023)

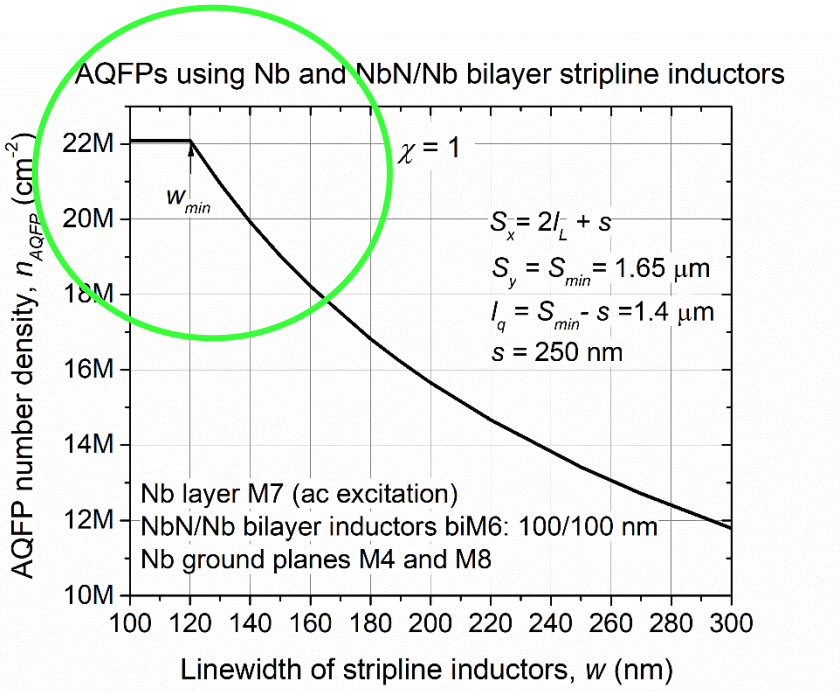
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 82, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

AQFP Scaling in SFQ7ee & Beyond



Parameters of ac excitation transformer, AQFP cell inductors (Nb & NbN striplines)





$$\beta_L = \frac{2\pi I_{CJ} L_2}{\Phi_0} = 0.2 \qquad \beta_q = \frac{2\pi I_{CJ} L_q}{\Phi_0} = 1.6$$

$$J_C = 100\ \mu A/\mu m^2$$
$$I_{CJ} = 50\ \mu A$$

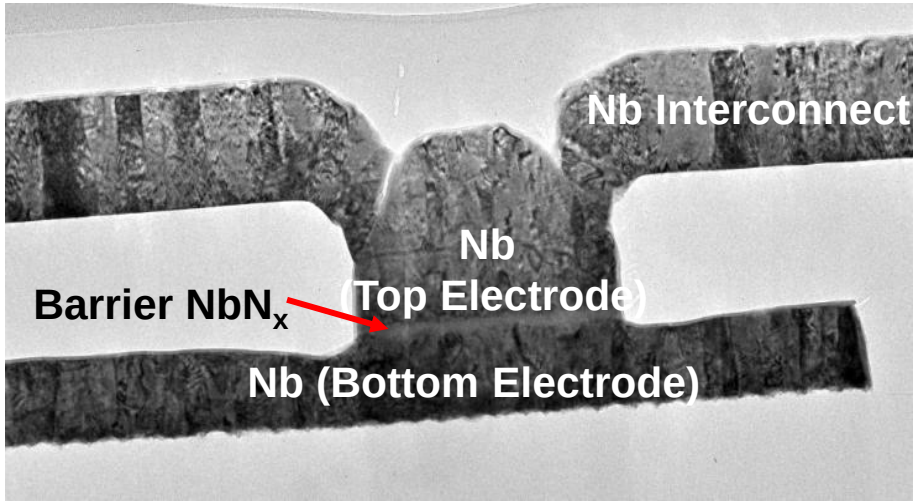
Path to ~20M AQFPs/cm^2 with advanced process node

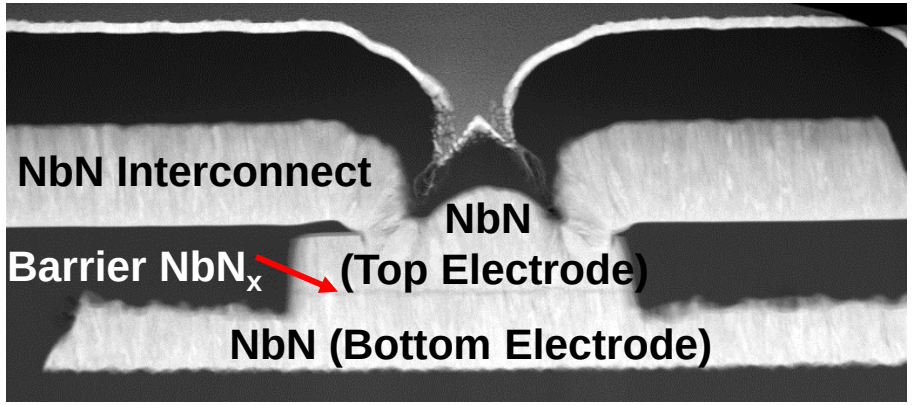
[ref] Tolpygo, *IEEE Trans. Appl. Supercond.*. 33 (Article # 1300419) (2023)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

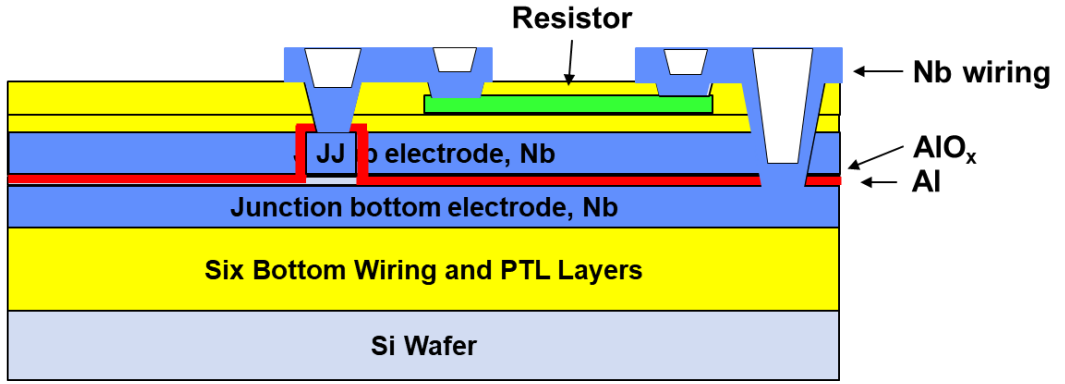
Development of SNS Self-Shunted Josephson Junctions

TEM Cross-section of the fabricated devices

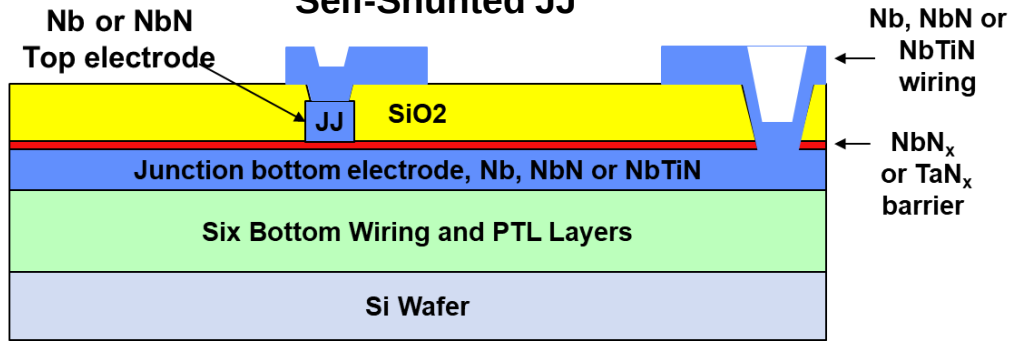




JJ with Shunt Resistor



Self-Shunted JJ

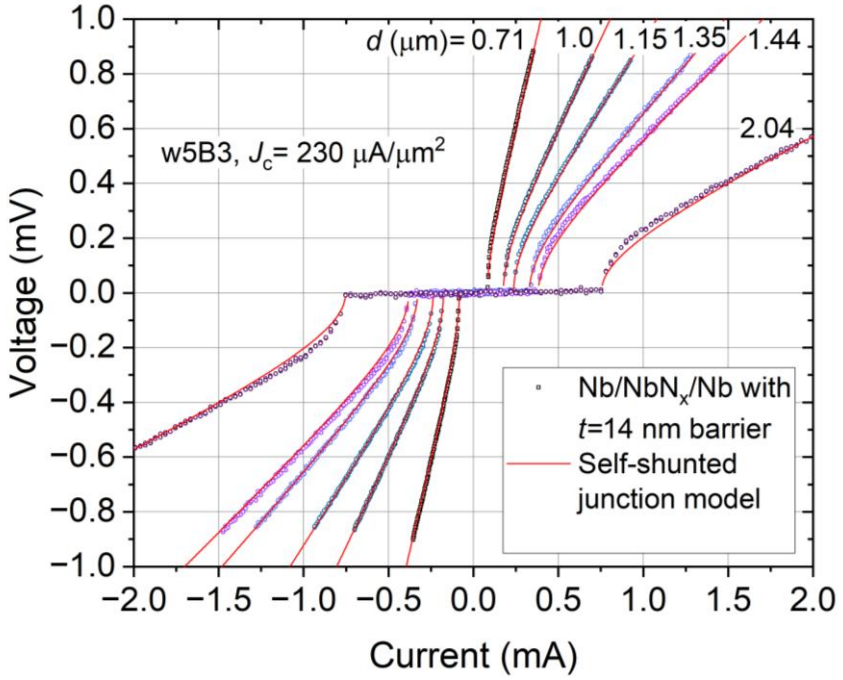


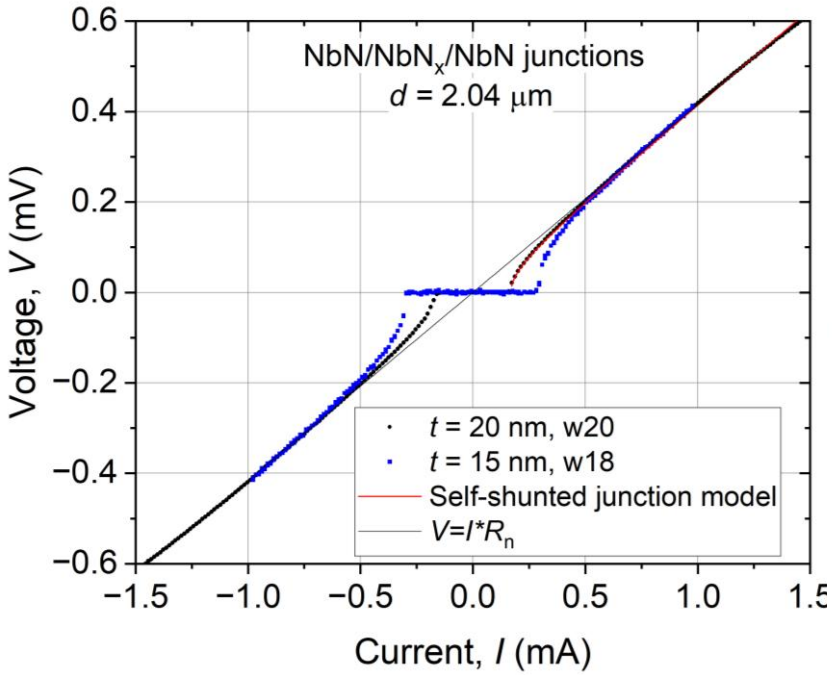
- Nb/Al-AlO_x/Nb tunnel junctions are used as active devices in SCE
  - These JJs are hysteretic and require resistive shunting to remove hysteresis
  - Shunt resistor increases the device area by about 10x
- Replaced 1-nm AlO_x barrier with 5-10 nm high-resistivity NbN_x or TaN_x to obtain self-shunted JJs with the same critical current density (J_c)

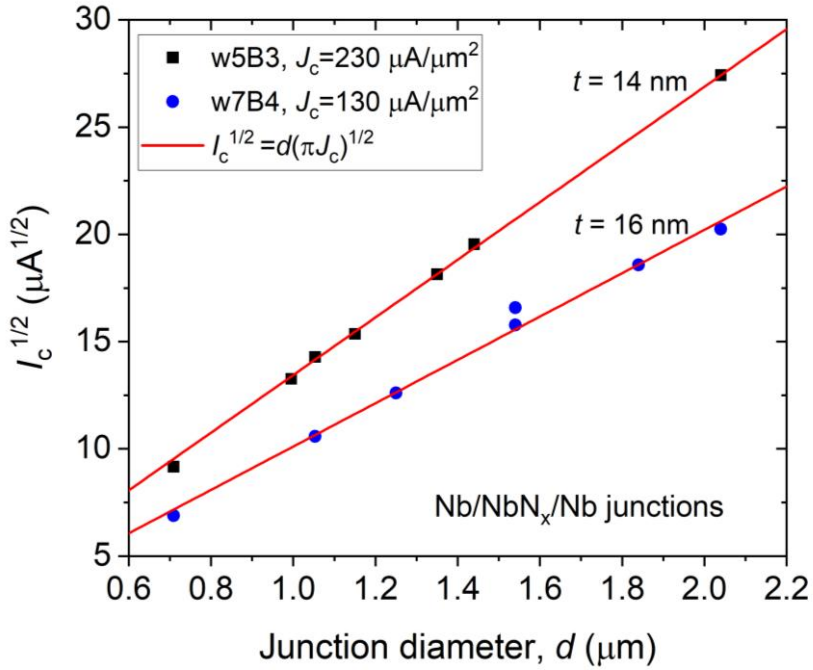
[ref] Tolpygo et al., *IEEE Trans. Appl. Supercond.*. 34 (Article # 1101008) (2024)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Electrical Properties of Nb/NbN$_x$/Nb and NbN/NbN$_x$/NbN Josephson Junctions





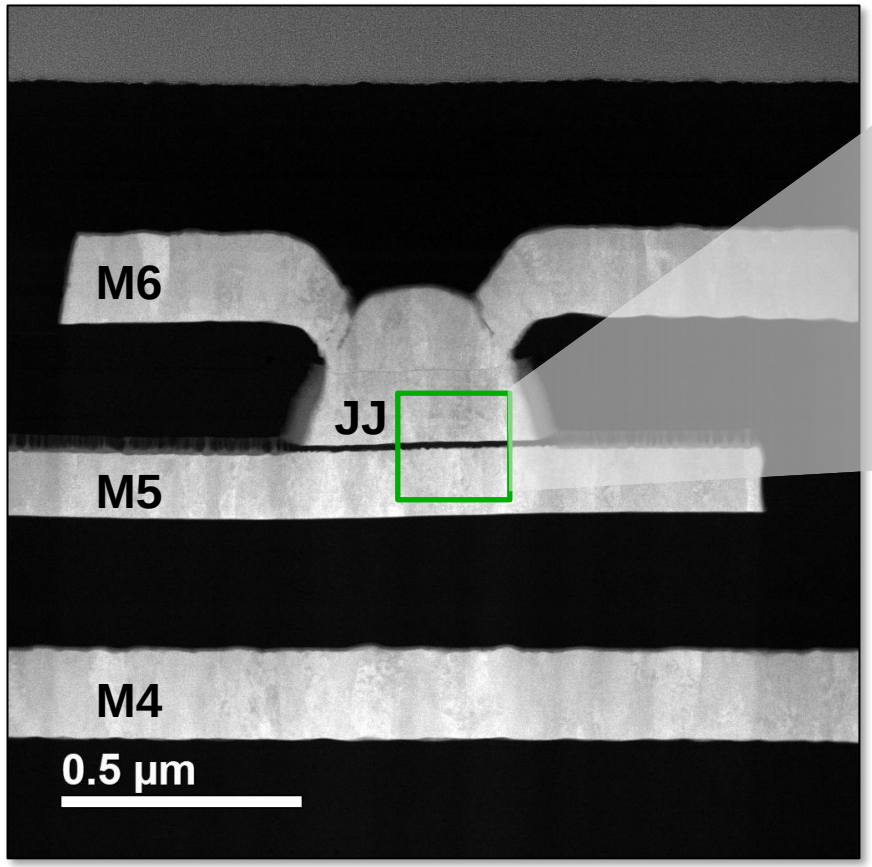


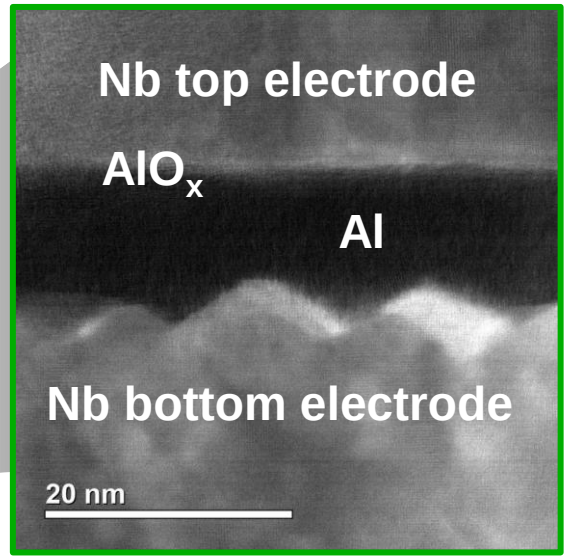
- ***I-V*** **characteristics show no hysteresis and are very well described by a self-shunted (intrinsically shunted) junction model**
- **Critical current of the junctions properly scales with the junction area,** $I_c \propto A \Longrightarrow \sqrt{I_c} \propto d$

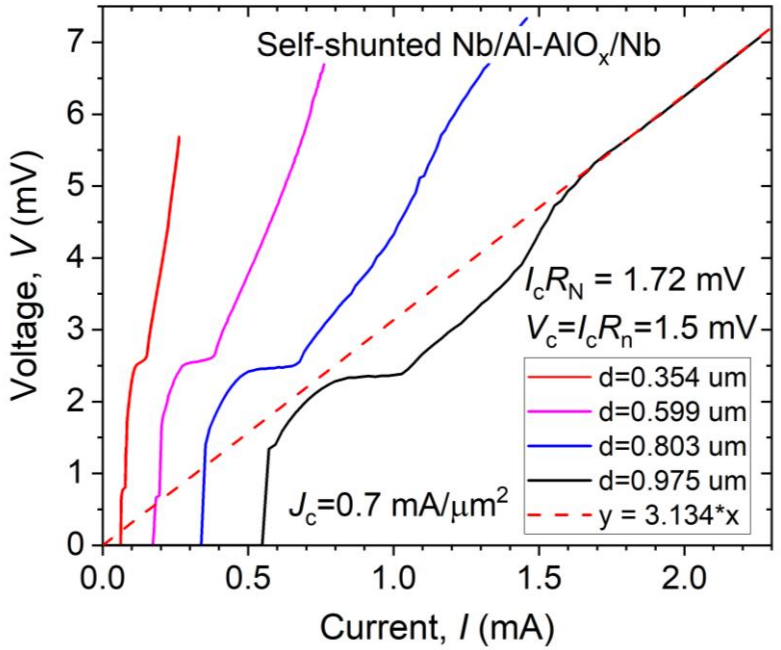
[ref] Tolpygo et al., ***IEEE Trans. Appl. Supercond.***. 34 (Article # 1101008) (2024)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

AlO_x-Based Self-Shunted JJs







- **Self-shunted AlO_x–barrier JJs are more difficult to fab because J_c is**
  - **sensitive to film stress and roughness in Nb bottom and top electrode**
  - **sensitive to Al thickness, roughness, and granularity**
- **However, Nb/Al-AlO_x/Nb JJs have a 4x – 5x larger $V_c = I_c R_n$ than JJs with deposited disordered barriers (NbN_x, TaN_x, doped a-Si,…)**
- **Much weaker critical current temperature dependence $I_c(T)$; better across wafer J_c uniformity**

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

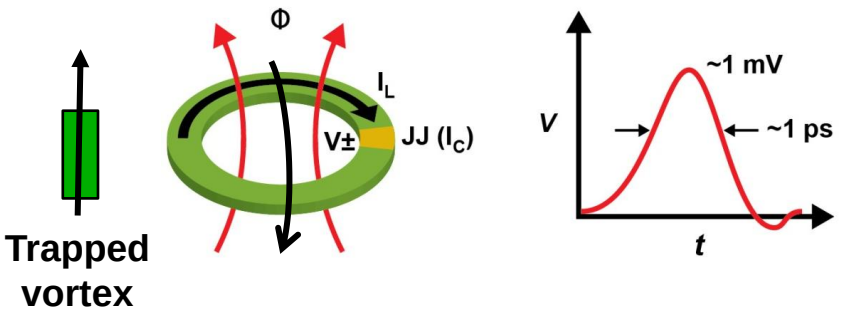
Outline

- Overview of MIT Lincoln Laboratory SCE integrated circuit foundry
- SCE digital logic applications and motivation for advanced process nodes
  - In context of continuing advances in digital CMOS technology
- Advanced process node development (SFQ7ee)
  - Emphasis on increasing SCE circuit density
    - Compact kinetic inductors
    - Self-shunted Josephson junctions
- Flux-trapping diagnostics and mitigation

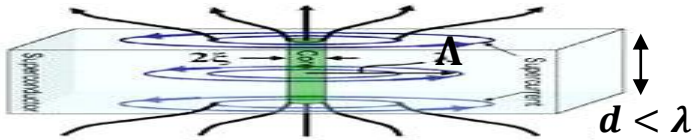
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

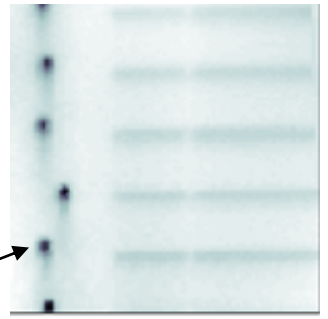
Superconducting Digital Logic
Flux Trapping

Superconducting loop

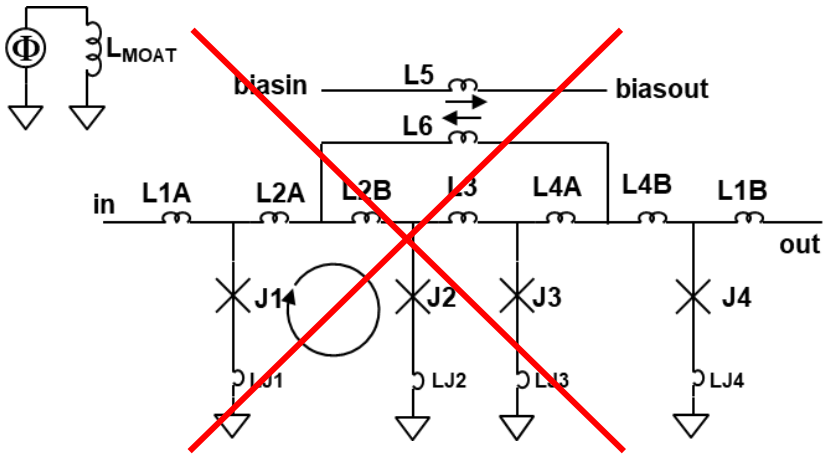


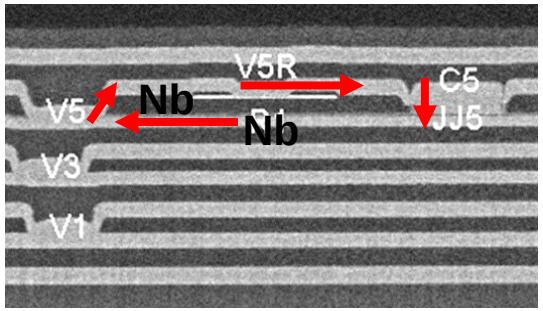
Pearl vortex

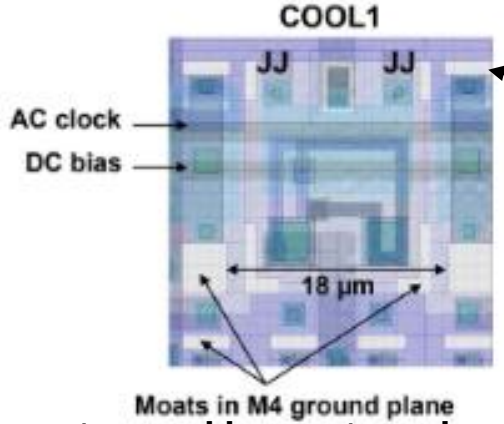




Flux trapped in film







Moat in AQFP cell [1]

Fluxon trapped in moat produces a much smaller magnetic field than a vortex in the film

Trapped flux can adversely affect SFQ circuit operation: need effective mitigation techniques

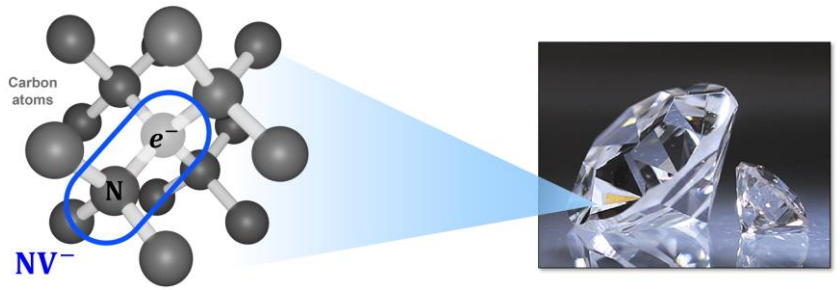
[1] Tolpygo, Ayala, Schindler et al., *IEEE Trans. Appl. Supercond.*. 35 (Article # 1300806) (2024)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

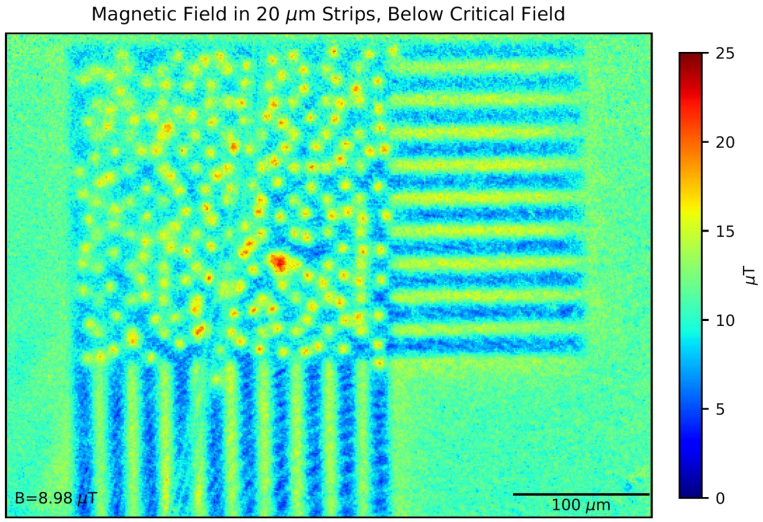
QSWIFT: Magnetic Microscopy for SDL Diagnostics

Quantum Solid-state Widefield Imager of Flux Trapping

Diamond Nitrogen-Vacancy (NV) Centers Sense Magnetic Fields

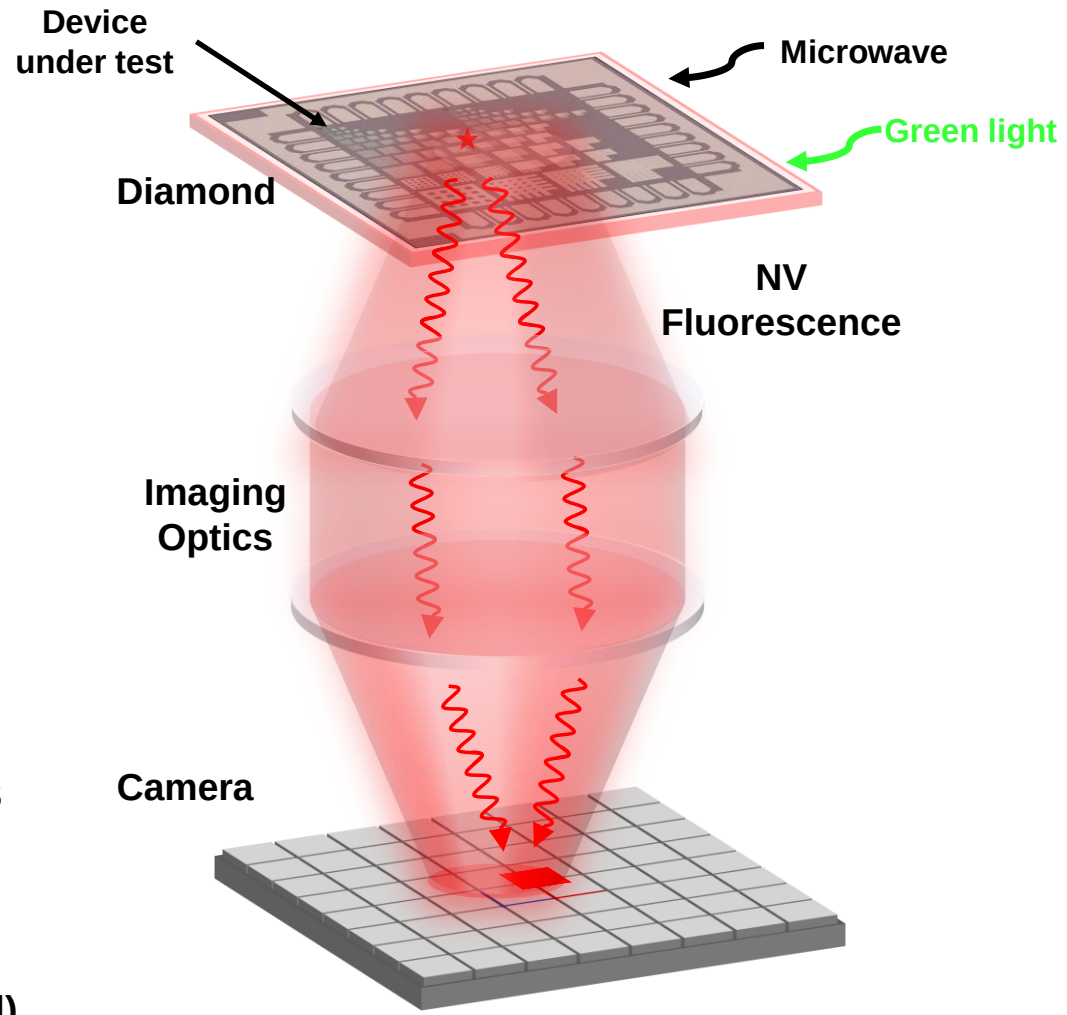


QSWIFT Magnetic Image of Trapped Flux in Superconducting Test Structure



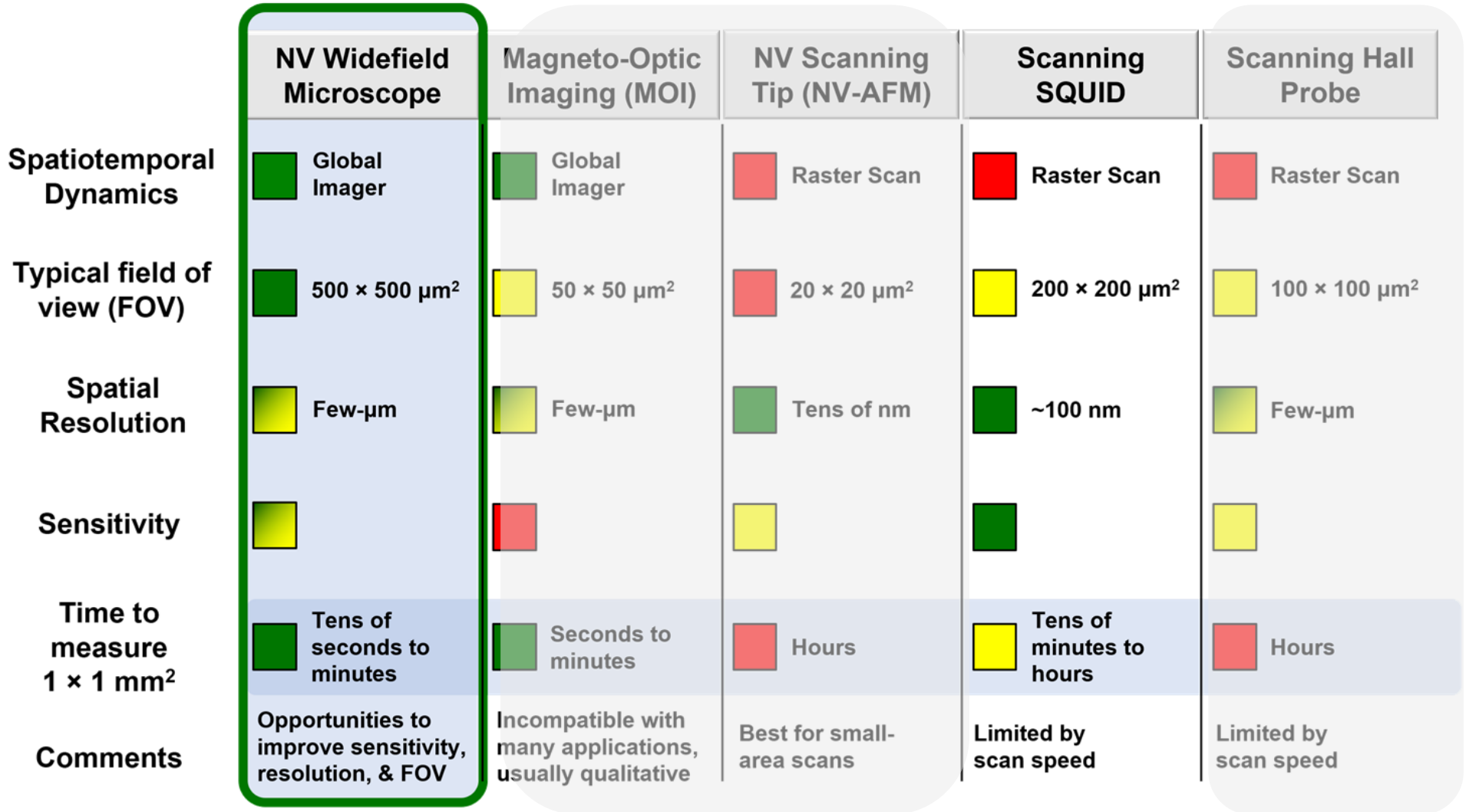
- **Fast, global imaging**
- **Micron-scale resolution**
- **Repeated measurements across T_c**

See arXiv:2506.01906 (Kapur et al)



IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

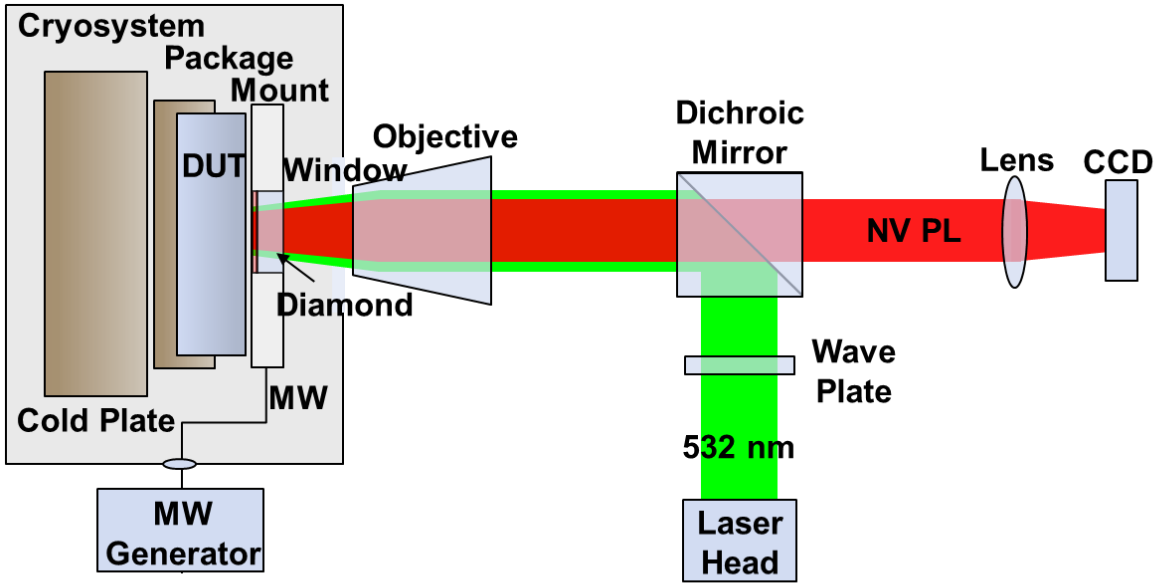
Magnetic Imager Comparison

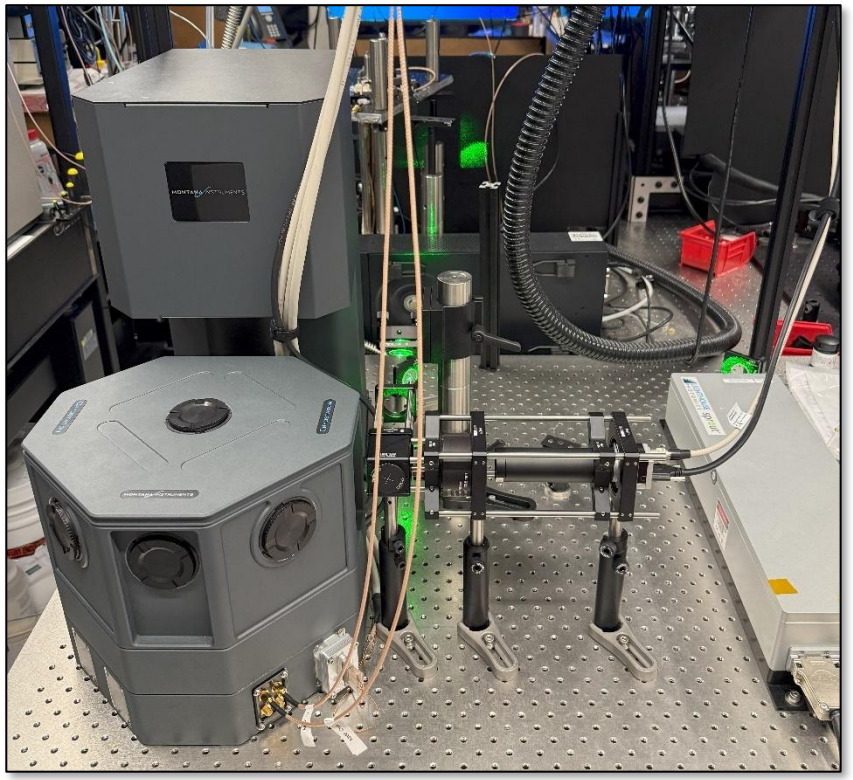


IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

QSWIFT Architecture

Widefield magnetic imager purpose-designed for flux trapping diagnostics





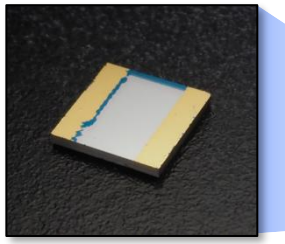
QSWIFT: Quantum Solid-state Widefield Imager of Flux Trapping

[ref] Kapur, Kehayias, Mallek, Schloss et al., *arXiv 2506.01906* (2025)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

QSWIFT Architecture

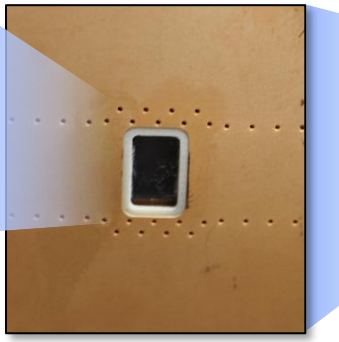
NV Diamond



Tailored production & custom coatings

Sample isolation from laser light

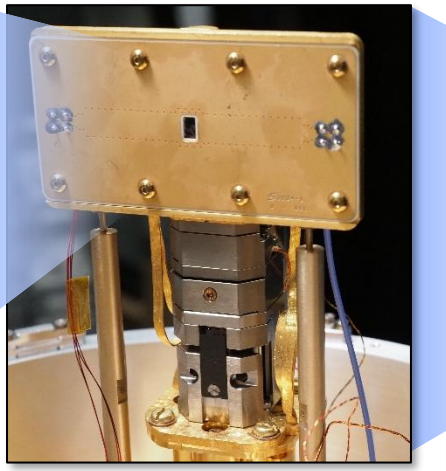
Diamond Stackup



EM shielding, microwave delivery, & sample interfacing

Micron-scale proximity to sample

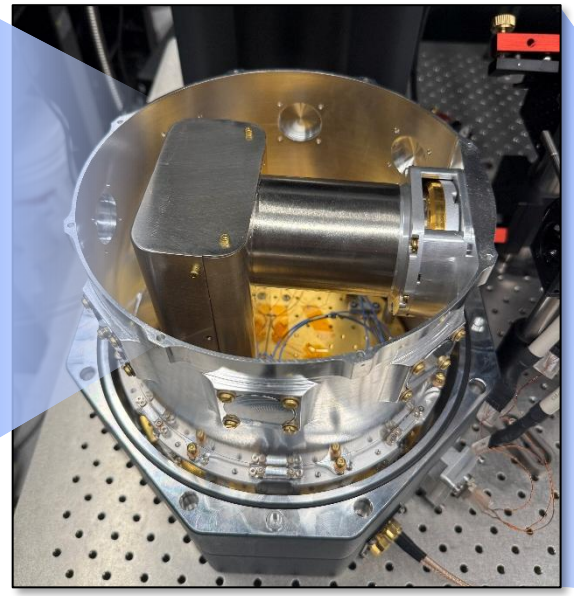
Sensor Head



Thermal management, sensors, coils, & translation

10 nT background magnetic field

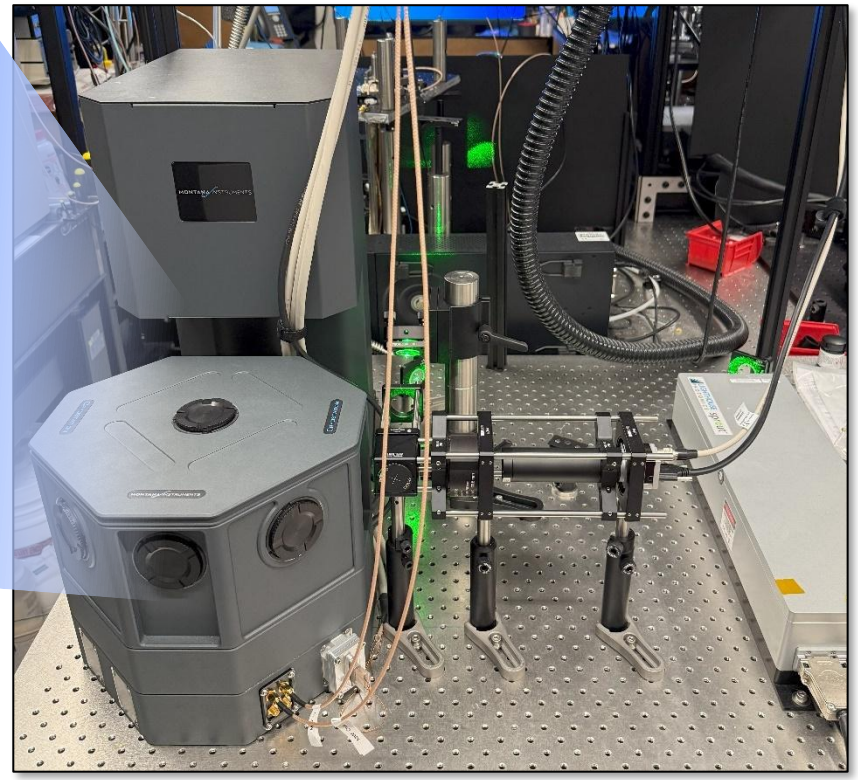
Measurement Chamber



Customized cryostat & custom magnetic shielding

4 K operation (<T_c of niobium)

QSWIFT Cryomicroscope System

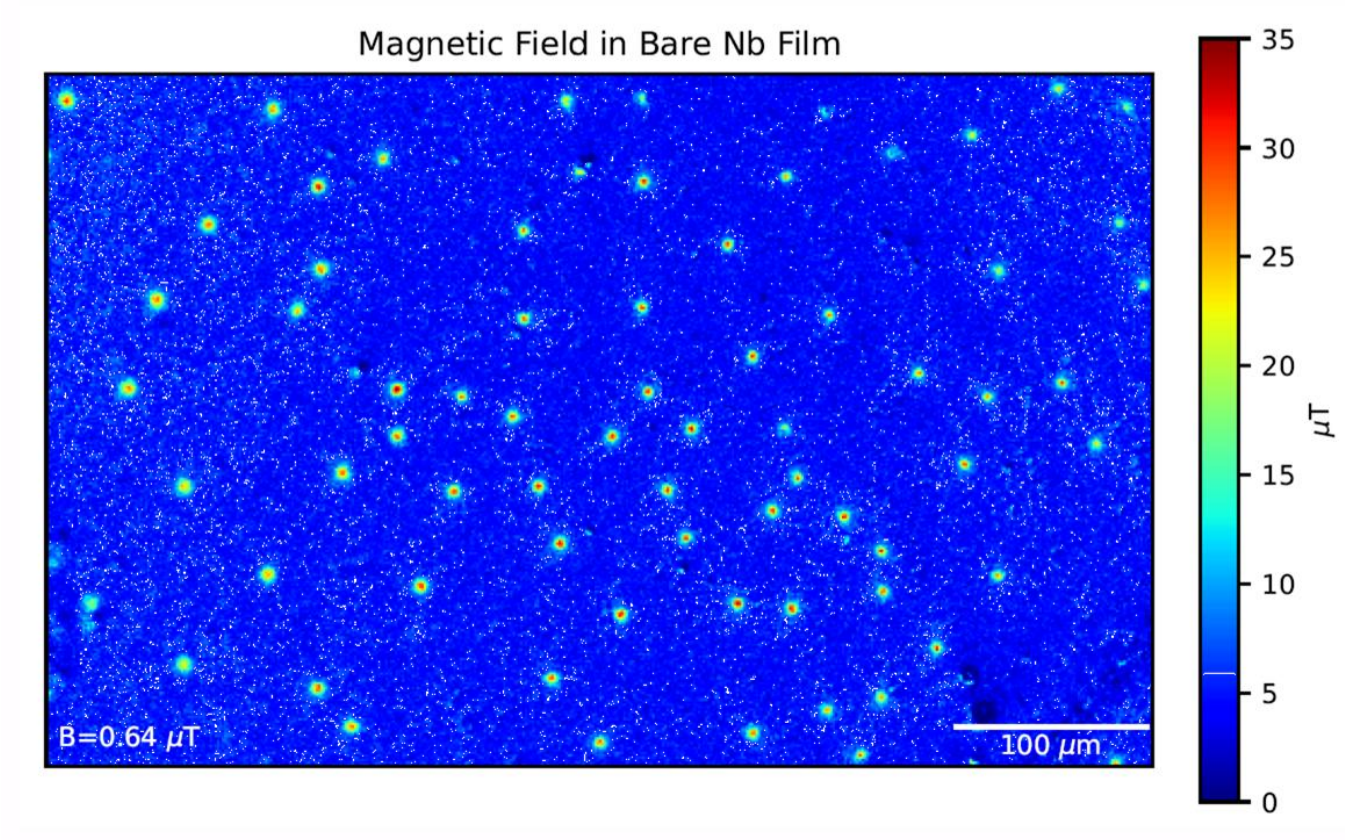


Optical microscope and system control outside cryostat

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Imaging Vortices in a Bare Niobium Film

- **Vortices visualized in 200nm Nb film**
  - **High SNR in minutes per image**
  - **Few-micron resolution**
  - **580 x 360 μm², tileable field of view**

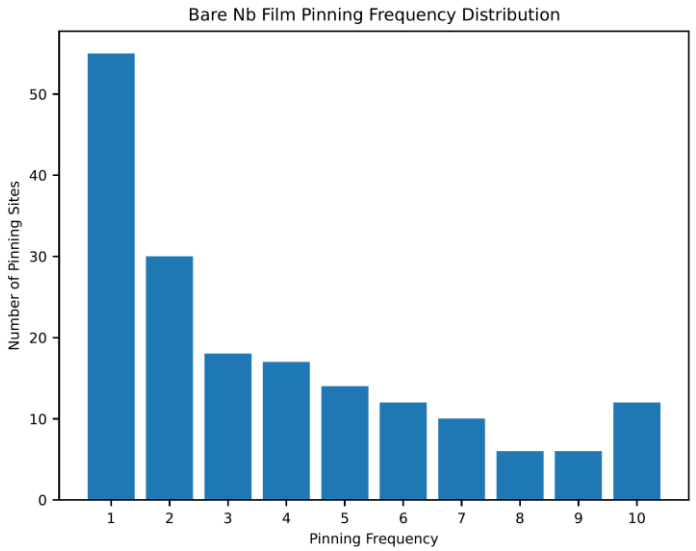


[ref] Kapur, Kehayias, Mallek, Schloss et al., *arXiv 2506.01906* (2025)

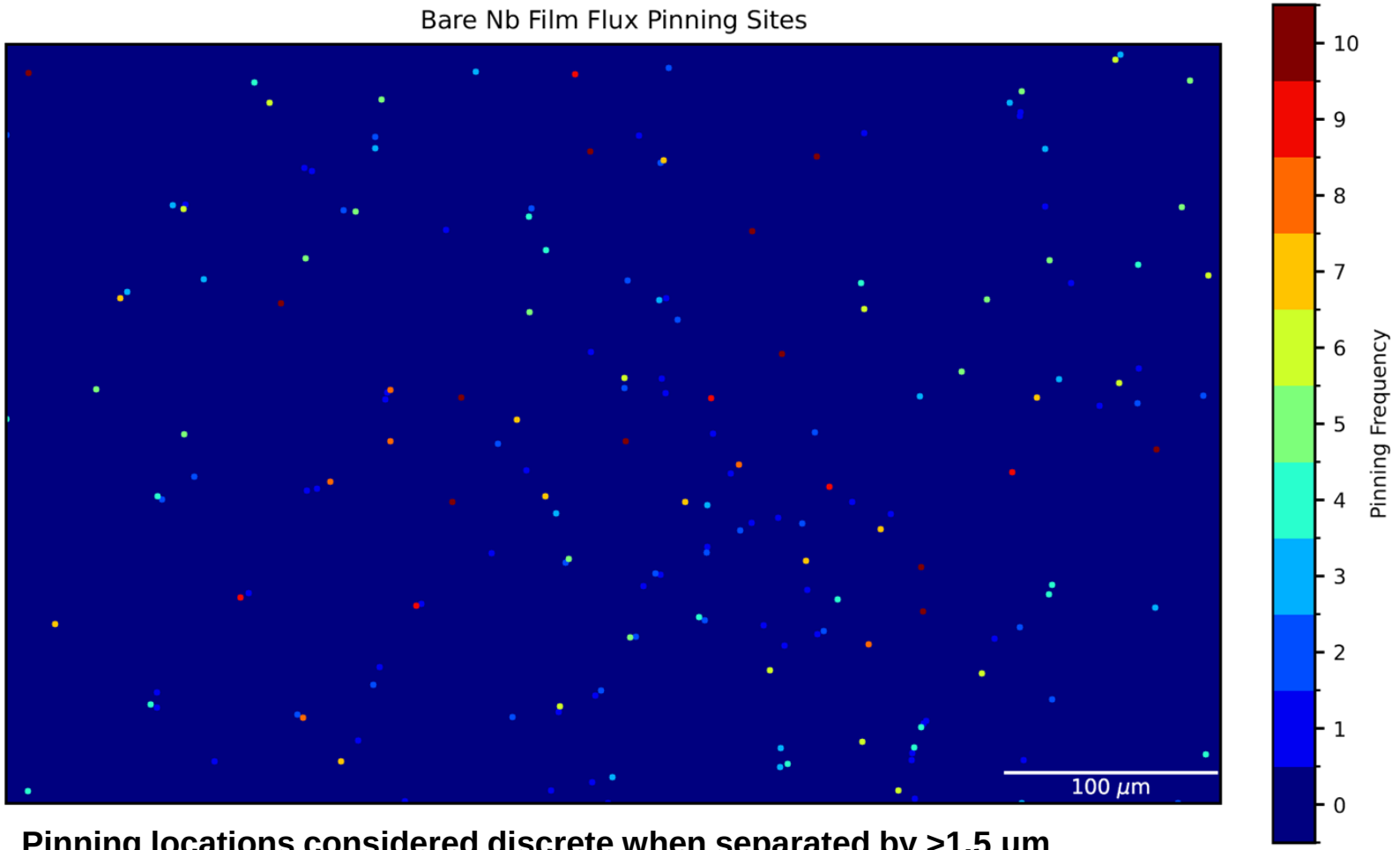
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Preferential Flux Pinning in Nb Film

Vortex statistics upon 10 cooldown cycles through T_c



A majority of sites are observed to pin vortices multiple times



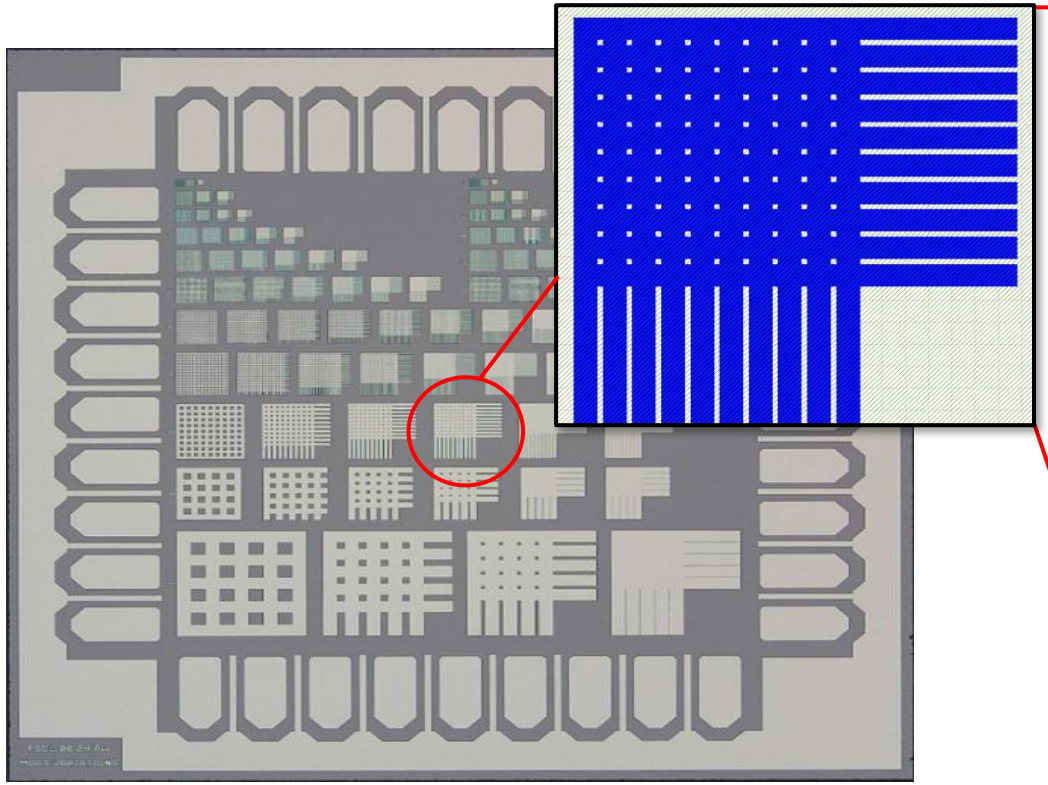
Pinning locations considered discrete when separated by >1.5 μm

[ref] Kapur, Kehayias, Mallek, Schloss et al., *arXiv 2506.01906* (2025)

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

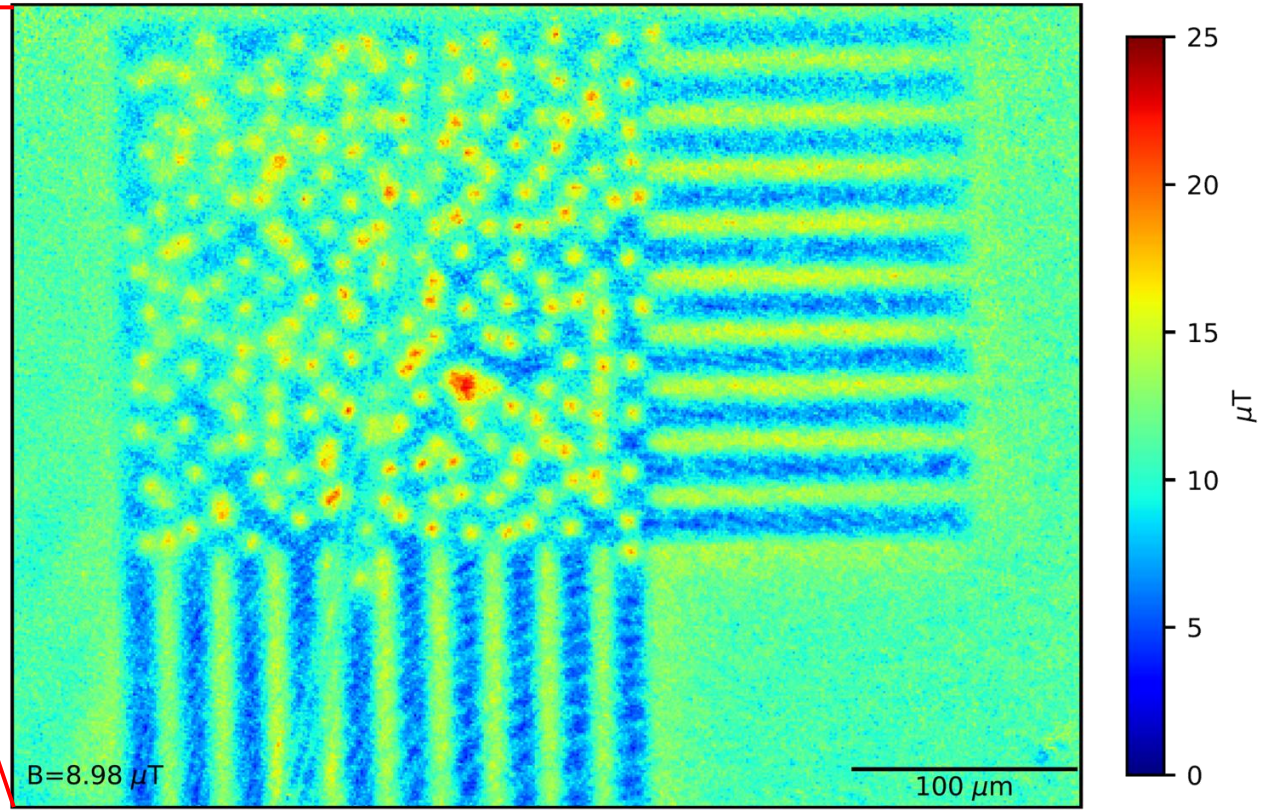
Field Expulsion in Intersecting Strips and Moats

Intersecting 20 μm Strips



FOCuS Intersecting Strip Array Test Chip

Magnetic Image Below Critical Field of Strips



>20x lower critical expulsion field in intersecting regions than in strips

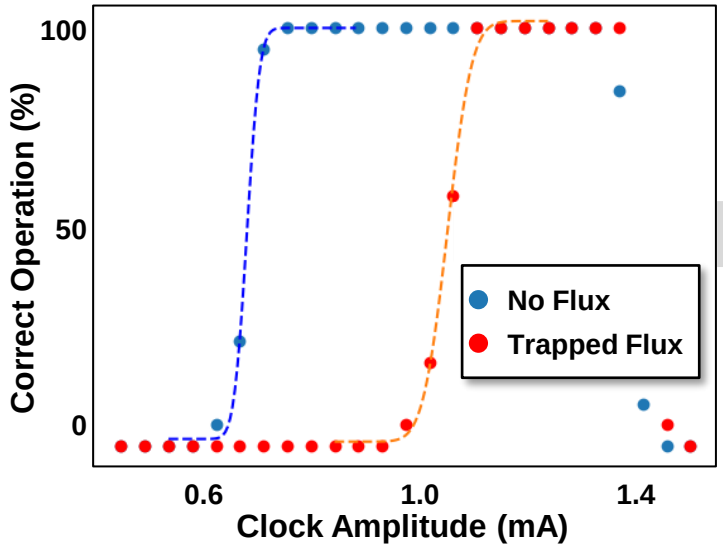
Early indication that flux trapping in 2D circuits does not follow intuition based on 1D systems

[ref] Kapur, Kehayias, Mallek, Schloss et al., *arXiv 2506.01906* (2025)

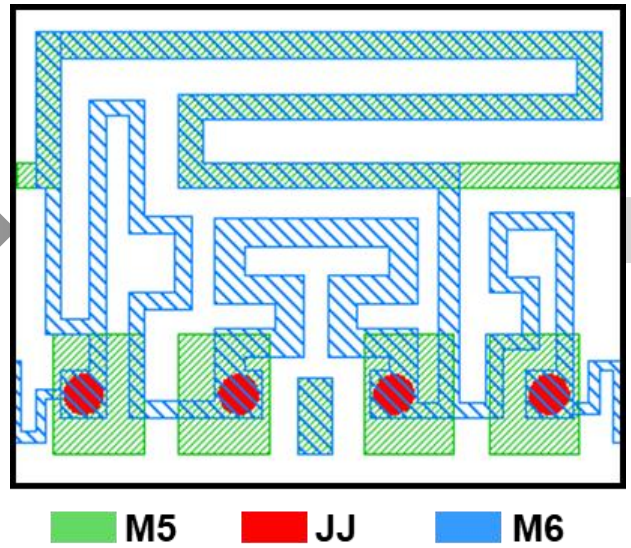
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

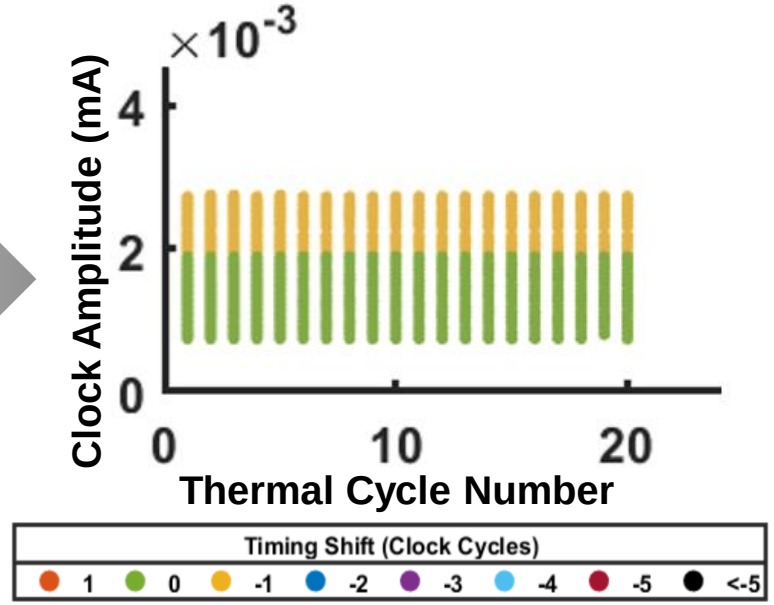
Flux Observation Control and Sequestration (FOCuS)

Circuit Simulation



Design





Integrate flux simulations into circuit design workflows

Design and fabricate benchmark circuits to study flux trapping

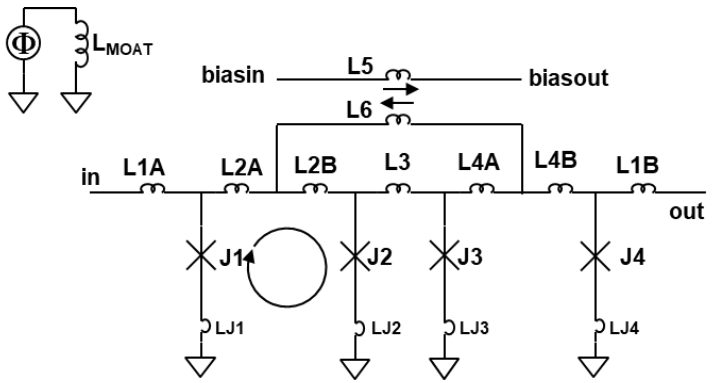
Perform in-house electrical testing to verify simulation results

MIT LL is working toward a foundational understanding of flux trapping in superconducting digital logic circuits

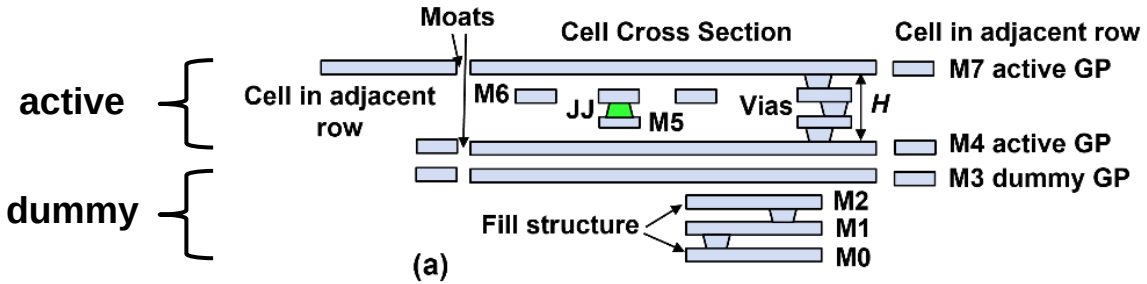
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

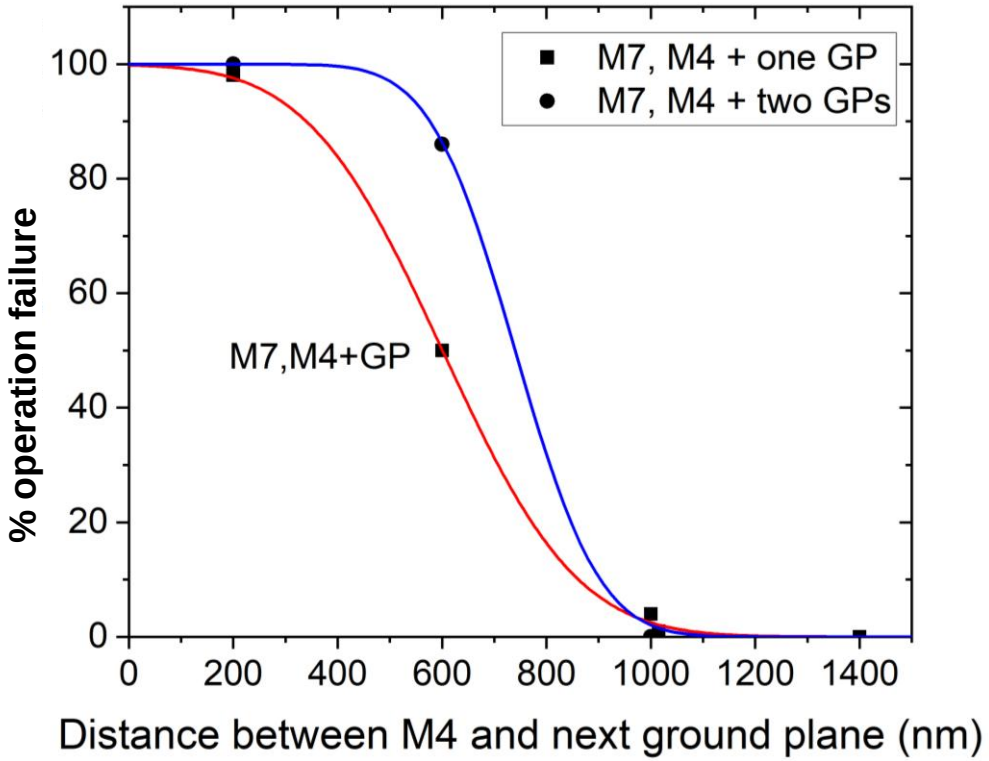
Effect of Multiple Ground Planes on Flux Trapping

Flux-shuttle shift register



Single 'dummy' ground plane





Closely spaced GPs can strongly enhance detrimental flux trapping outside moats

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Summary

- **Superconducting electronics provides a combination of higher speed and lower energy dissipation exceeding that of any other beyond-CMOS digital logic integrated circuit technology**
- **Increasing circuit density (gates per cm^2) enables future applications**
- **Both compact (kinetic) inductors and self-shunted Josephson junctions are key elements of advanced process nodes**
- **Continuing progress in evaluating and mitigating causes and effects of flux trapping in SCE integrated circuits**

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 62, Jan. 2026. Presentation given at QUEST 2025, Yokohama, Japan, Oct. 2025.

Acknowledgements

Quantum-Enabled Computation Group

Group Leaders: Mollie Schwartz, Jonilyn Yoder, Joe Belarge, Julie Haiar, Kyle Serniak, Steven Weber

Senior Staff: Jeffrey Birenbaum, A. Jamie Kerman, Lenny Johnson, Kevin Obenland, Sergey Tolpygo

Group: James Aguilar, Kate Azar, Peter Baldo, Anthony Bishop, Logan Bishop-Van Horn, Maria Blood, Tristan Brown, Luke Burkhart, Gregory Calusine, Glenn Carl, Lynn Clifford, Felipe Contipelli, John Cummings Jr, David Danza, Rabindra Das, Daniel Davis, Renee DePencier Pinero, Steve Disseler, Justin Elenewski, Ben Freiman, Jeffrey Gertler, Michael Gingras, Evan Golden, David Goldfinger, Ben Goodwin, Kevin Grossklaus, Karen Harmon, Thomas Hazard, Michael Hellstrom, Cyrus Hirjibehedin, Gerard Holland, Jennifer Hritz, Bethany Huffman, Sokharom Huon, Erin M. Jones-Ravgiala, David Kim, Jeffrey Knecht, Parker Kuklinski, Arthur Kurlej, Shavonne LaFauci, Justin Mallek, Andrew McKie, Roderick McNeill, Scott Meninger, Duncan Miller, Nathan Miller, Jovi Miloshi, Maddie Morocco, Kaitlyn Morrell, Zain Mughal, Rylee Neumann, Chris O'Connell, Neel Parmar, Susan Pitman, Maria Prado Rodriguez, Mallika Randeria, Ravi Rastogi, Benjamin Rempfer, Matt Ricci, Lila Rodgers, Rob Rood, David Russo, Gabriel Samach, Andrew Savage, Meghan Schuldt, Arjan Sevi, Arnav Sharma, Marcus Sherwin, Katrina Sliwa, Basil Smitham, Hannah Stickler, Manz Thompson, Chris Thoummaraj, Kate Thurmer, Andrew Wagner, Jennifer Wang, Terry Weir, Charles Woodrum, June Woods, Alex Wynn, Donna Yost

MicroElectronics Laboratory

Group Leaders: Dan Pulver, Carrie Huguenin

Group: Mike Antos, Christine Baker, Fredda Bauer, Creda Beauchamp, Susan Bengtson, Matt Blago, Heather Brum, Anne Cappucci, Mark Carroll, Curtis Castello, Brandon Chea, Kevin Checkosky, Vanndy Chhuon, Matt Cook, Jeff DeCaprio, Aishik Dhori, Phil Dimitroglou, Kathy Doan, Charly Em, Timmy Em, Howie Gallant, Jim Gallo, Ben Hall-Seelig, Bob Healey, Bob Holden, Craig Hill, Denise Holohan, John Hunt, Charlie Huoth, Sal Ieni, Matthew Jacobs, Rebecca Kelley, Venne Laine, Dilip Mahenthiran, Mitch Makowicz, Paul Makowicz, Joel Maldonado, Stephen Margiotta, Matt McClellan, James McNaney, Brian Mulloney, Lindina Nith, Samuel Ogura, Nick Oum, John Pentoliros, Penny Phengsavath, Segundo Pichardo, Gianni Pinelli, Alistair Plotnick, Chris Porter, Joe Powers, Angel Reinold, Nazeem Saddeek, George Scetta, Chris Segni, Dmitri Shapiro, Rowan Smith, Bob St. Martin, John Stegner, Jim Stilian, Robin Vitale, Chris Weinburg, TJ Wlodarczak, John Wong, Zallay Yun, Scott Zarr