

► Towards Ultra-Low Power Computing: SFQ Brownian Logic Circuits

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Outline

- **Motivation & Research Goal**
- **SBLC (SFQ Brownian Logic Circuit)**
- **Functional Validations & Performance Evaluations**
- **Summary**

Outline

□ Motivation & Research Goal

➤ Toward Ultra-Low-Power Computing

□ SBLC (SFQ Brownian Logic Circuit)

□ Functional Validations & Performance Evaluations

□ Summary

SFQ Computing

□ SFQ devices are promising technologies & operate at 4 K

□ What is unique about SFQ devices?

- High switching speed ($\sim 1\text{ps}$)
- Low energy ($\sim 0.1\text{aJ}$)
- Long-distance lossless signal propagation (light speed / 3)

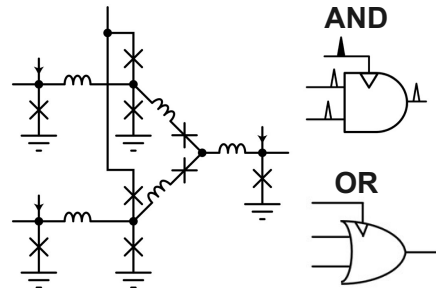
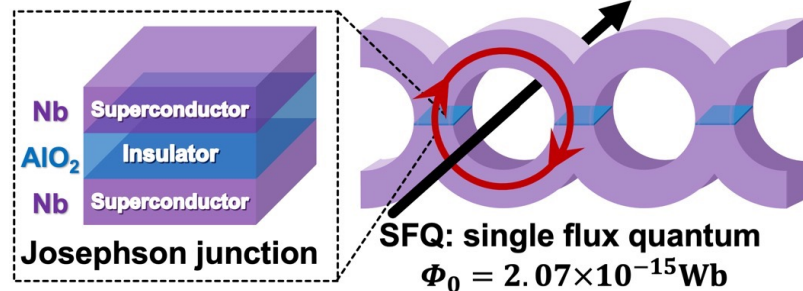


Outstanding High-Performance / Low-Power Computing Systems

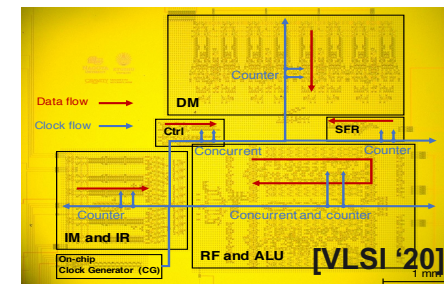
Device

Logic gate

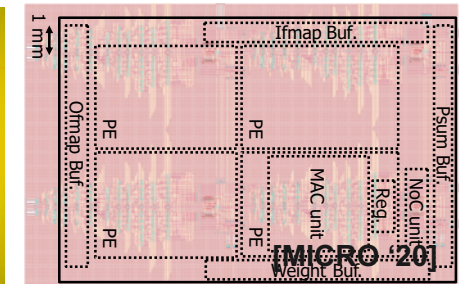
Circuit / Architecture



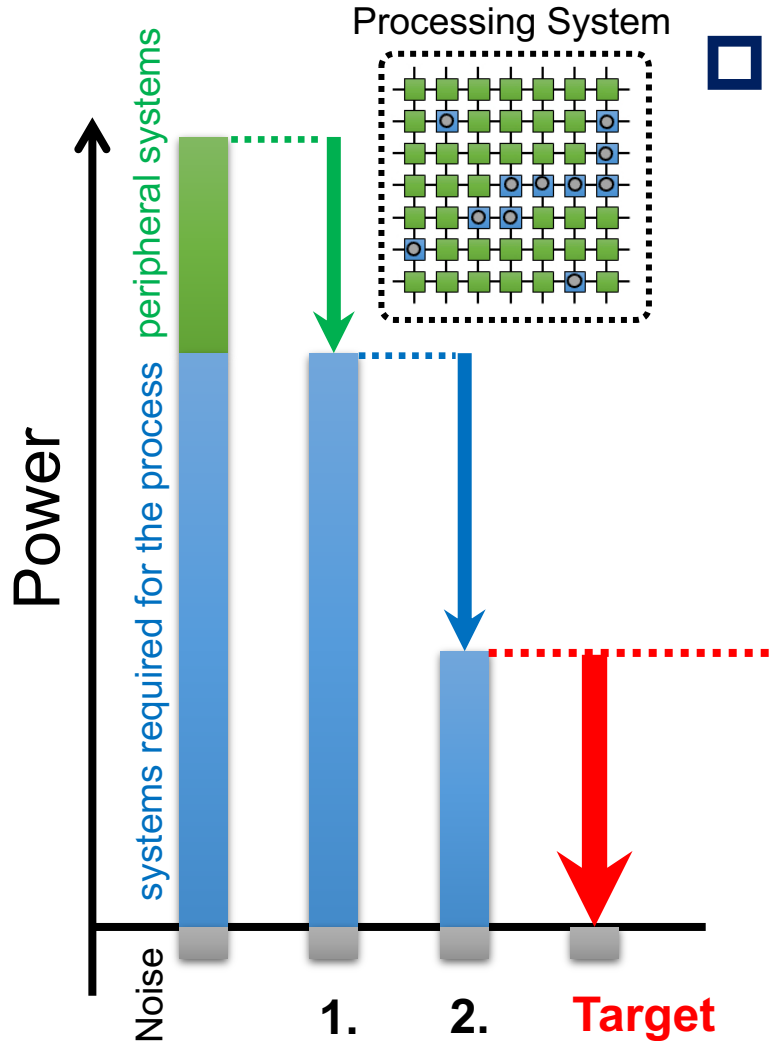
32GHz 6.2mW 4bit Processor



50GHz AI Accelerator



Toward Ultra-Low-Power Computing



□ Conventional low-power technologies

1. **Intermittent operation: How to eliminate waste?**
e.g., Normally-off, Clock gating techniques

2. **Low-accuracy: How to reduce processing energy?**
e.g., Emerging devices, Approximate, analog manner

Noise Limit



→ Power reduction limit for correct operation (S/N)

Using noise as a mechanism for circuit operation

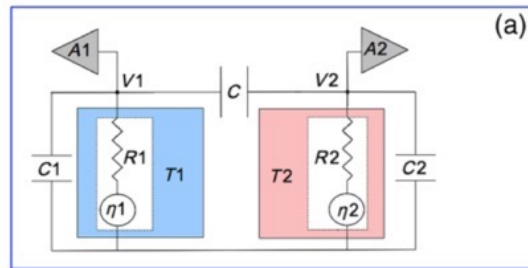
→ Noise = Energy available for “free”

Toward Ultra-Low-Power Computing

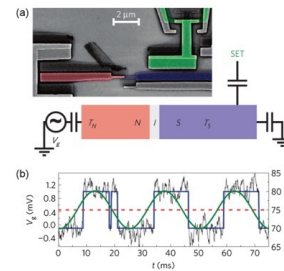
□ Stochastic Thermodynamics

➤ How to convert free energy into work?

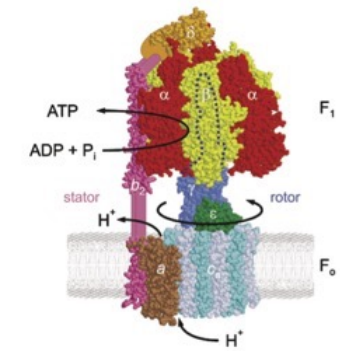
Electrical circuit



Single electron box



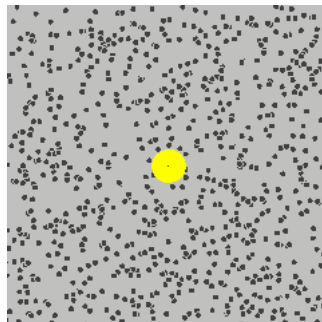
Molecular motor



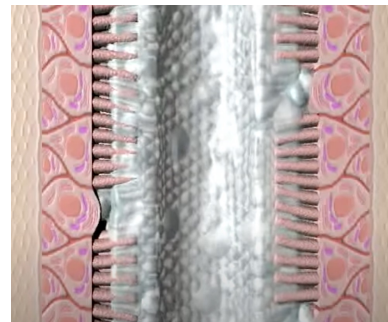
□ Compute Like Nature

➤ Trying to use Brownian motion for computations

2D Brownian motion



Ciliary movement



viewpoints

DOI:10.1145/3431282

Todd Heflin, Thomas M. Conte, and Mark D. Hill

Viewpoint

A Vision to Compute Like Nature: Thermodynamically

Advocating a new, physically grounded, computation paradigm centered on thermodynamics and an emerging understanding of using thermodynamics to solve problems.

Computational complexity theory and digital machine engineering are the bedrock of modern computing. Yet, even as we push the boundaries of Moore's Law, we face fundamental physical limits. The energy cost of computation is no longer negligible. In fact, it is becoming a significant barrier to progress. This viewpoint argues that the future of computing lies not in more transistors, but in more efficient energy use. It explores the potential of using thermodynamics to design computation systems that are not only more energy-efficient, but also more robust and adaptable to a wide range of environments. The viewpoint discusses the challenges of energy-efficient computing and the potential of using thermodynamics to overcome these challenges. It also discusses the potential of using thermodynamics to design computation systems that are more robust and adaptable to a wide range of environments.

The Laws of Thermodynamics for computation systems are well known and have been used extensively in the analysis of computational efficiency and in machine learning algorithms. Since the time of Carnot and Joule, the field of computation and thermodynamics has been a rich area of research. However, the field has not yet reached its full potential. This viewpoint discusses the challenges of energy-efficient computing and the potential of using thermodynamics to overcome these challenges. It also discusses the potential of using thermodynamics to design computation systems that are more robust and adaptable to a wide range of environments.

Challenges – SFQ Brownian Logic Circuits

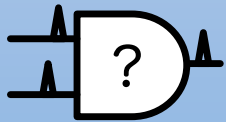
□ What is required to utilize noise in circuit operation?

- How do we calculate with uncontrollable devices? [Comp. Principle]
- What is the devices ? [Devices]
- What are the structures that implement? [Logic Circuits]
- Is the system can be “realistically” handled? [Architecture]

Reinventing from Principle to Architecture

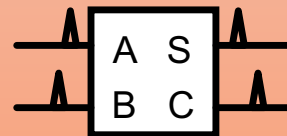
1. Principle/Device

- Transmission line
- Logic gates



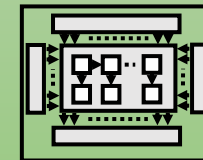
2. Circuit

- Calculation units
- ADD, MUL, MAC



3. Architecture

- Processing elements
- Hybrid arch.



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 - **Introductiong basics: random walk line / universal gate set**
- Functional Validations & Performance Evaluations
- Summary

SFQ Random Walk Line

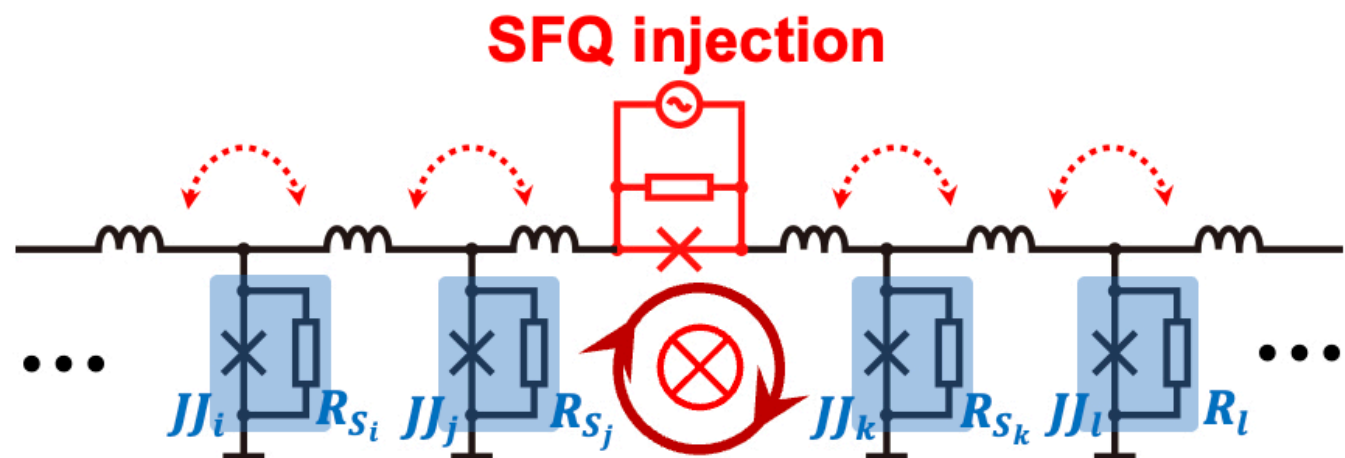
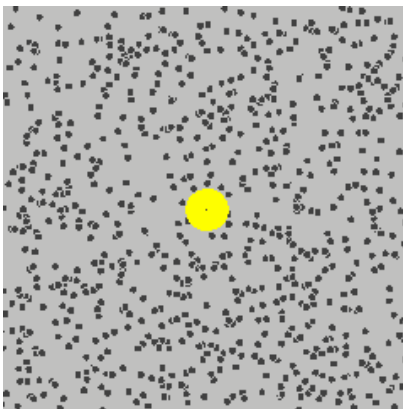
□ SBLCs: SFQ Brownian Logic Circuits

- Computation based on random search for the circuit topology

□ SFQ Random Walk Line (0.04% Power)

- Clock signal line (25%) : Clockless
- Static power (95%) : No bias voltage
- Dynamic power (99%) : Low I_c near to noise-level

2D Brownian motion



Universal Gate Set for SBLCs

□ Universal Reversible Gate Set

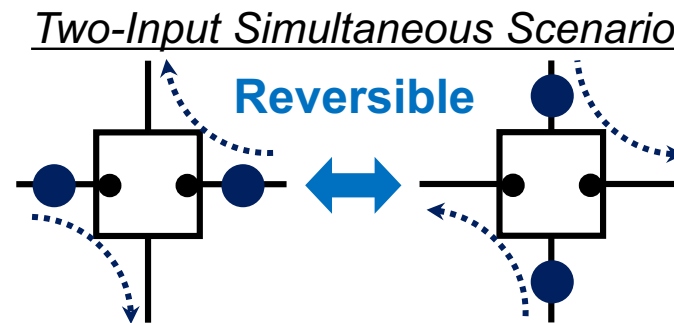
➤ Random walk line / Hub, CJoin / Ratchet

● : token

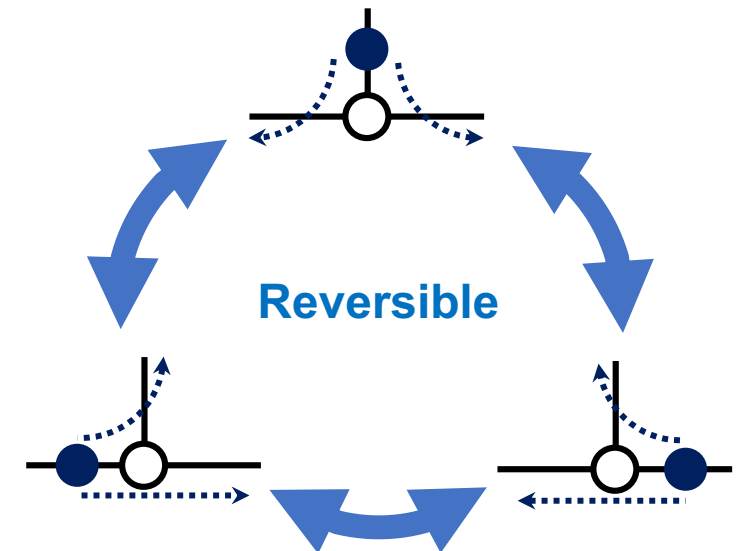
Random walk line



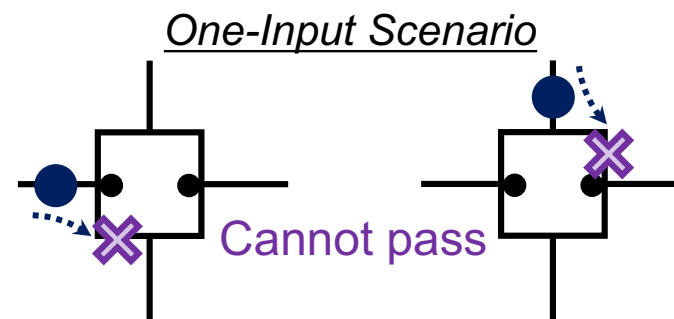
CJoin Gate



Hub Gate



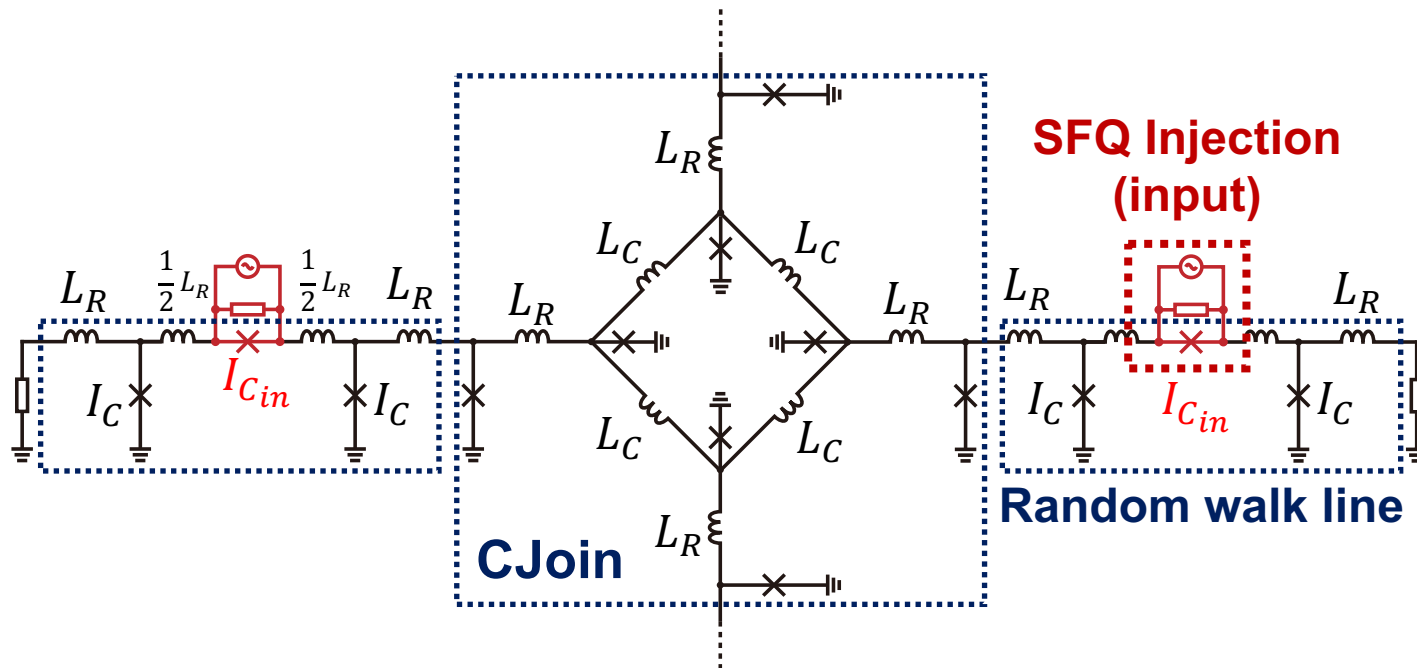
Ratchet Gate



Arbitrary Operation with SBLCs

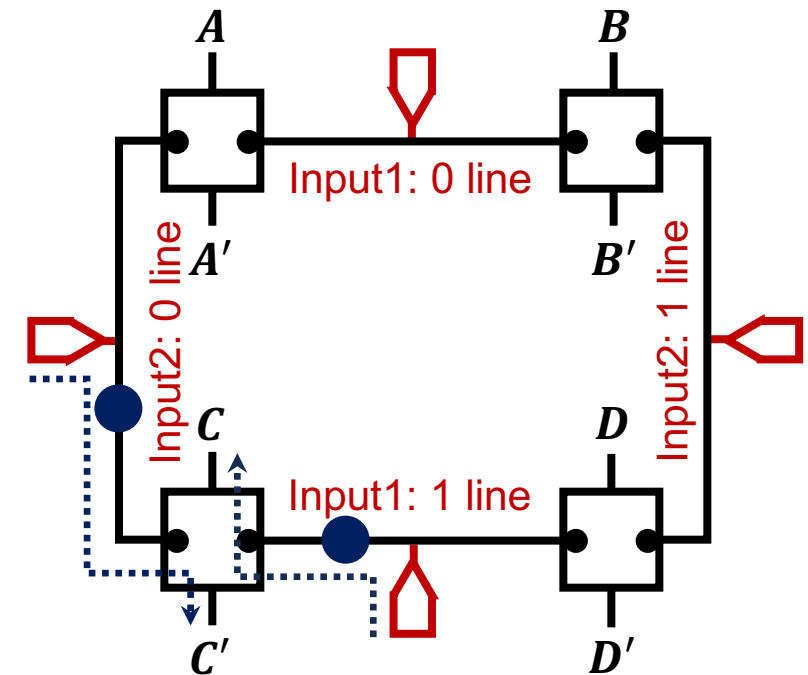
- SFQ CJoin Gate
- Arbitrary Operation with CJoin

Schematic of SFQ CJoin gate



In1	In2	Out1	Out2
0	0	A (0)	A'(0)
0	1	B (0)	B'(1)
1	0	C (0)	C'(1)
1	1	D (1)	D'(0)

Universal gate



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- Functional Validations & Performance Evaluations**
 - Random walk line / CJoin gate
 - Half-adder / Ripple carry adder / Register
- Summary

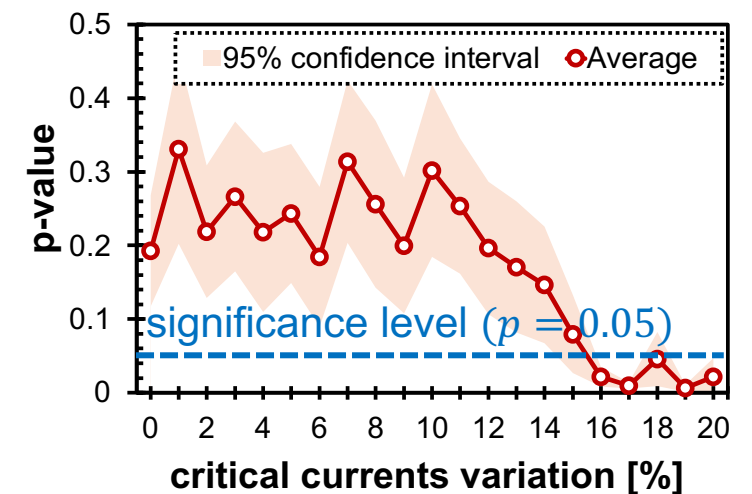
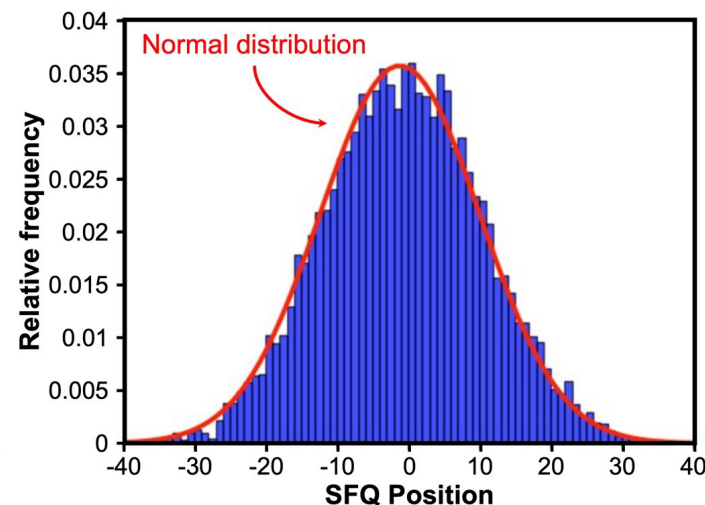
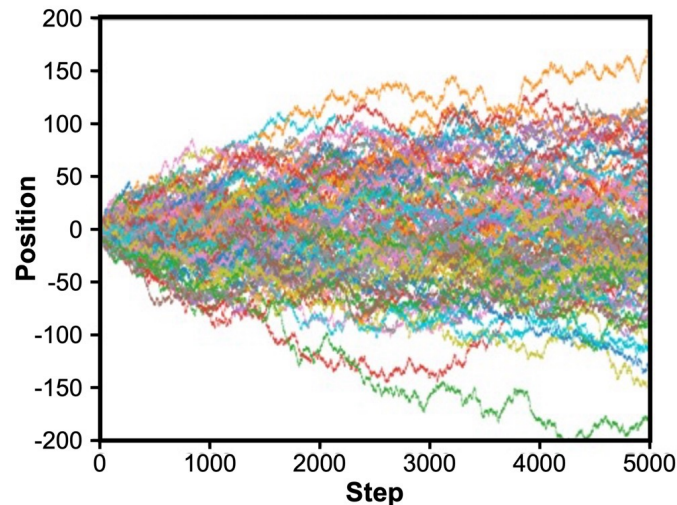
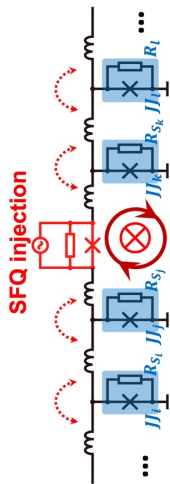
Validation: SFQ-Random Walk

□ JoSIM based Functional Validation for Random Walk Line

- Jonson noise: $\langle i_n \rangle = \sqrt{4k_B T B / R_S}$ $I_C = 1 \mu A, T = 4.2 K, B = 700 GHz, R_S = 184 \text{ ohm}$
- Shapiro-Wilk test: $p = 0.294 > 0.05$

□ Tolerance to Fabrication I_C Variations

- $I_C \pm 15\%$ can be acceptable



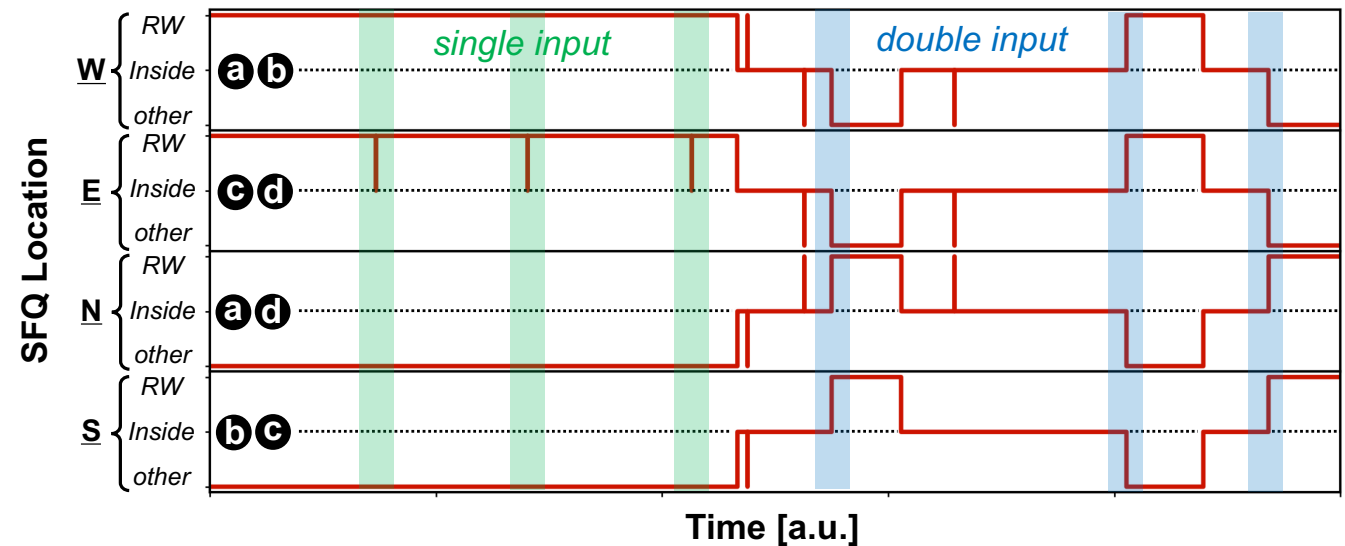
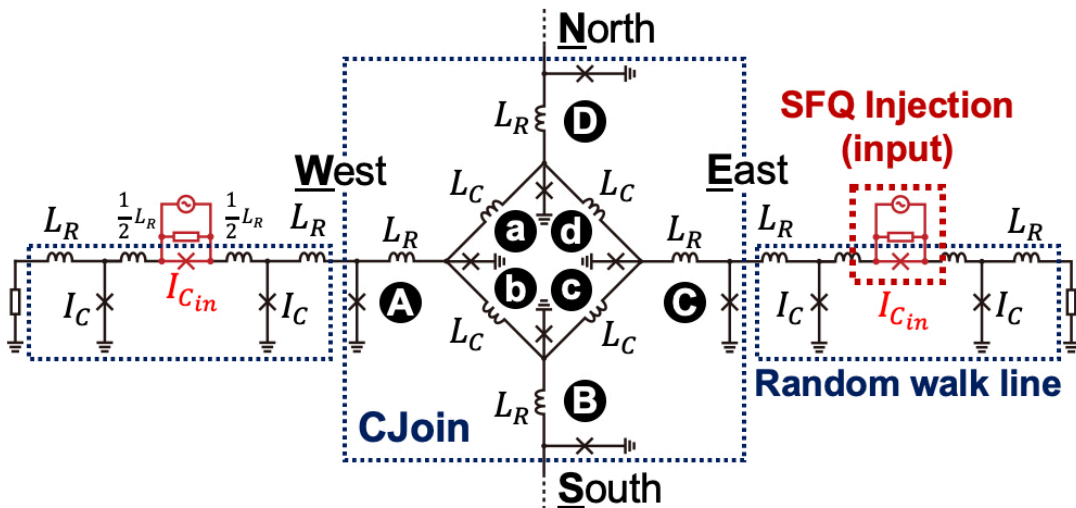
Validation: SFQ-CJoin Gate

JoSIM based Functional Validation for CJoin Gate

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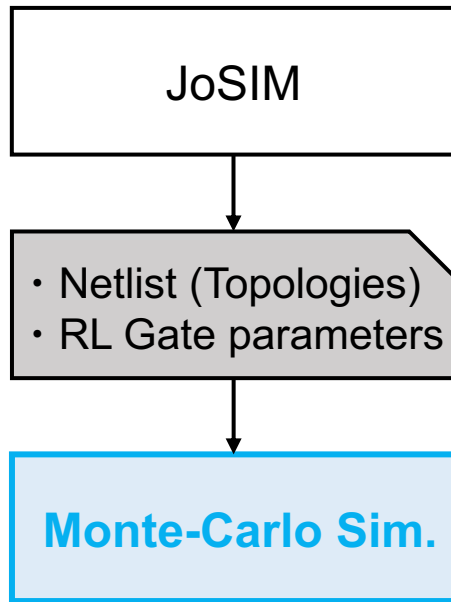
CJoin Functional Requirements

- Single input: Tokens cannot pass through. Functions as a wall.
- Double input: Tokens pass through. Reversible function.



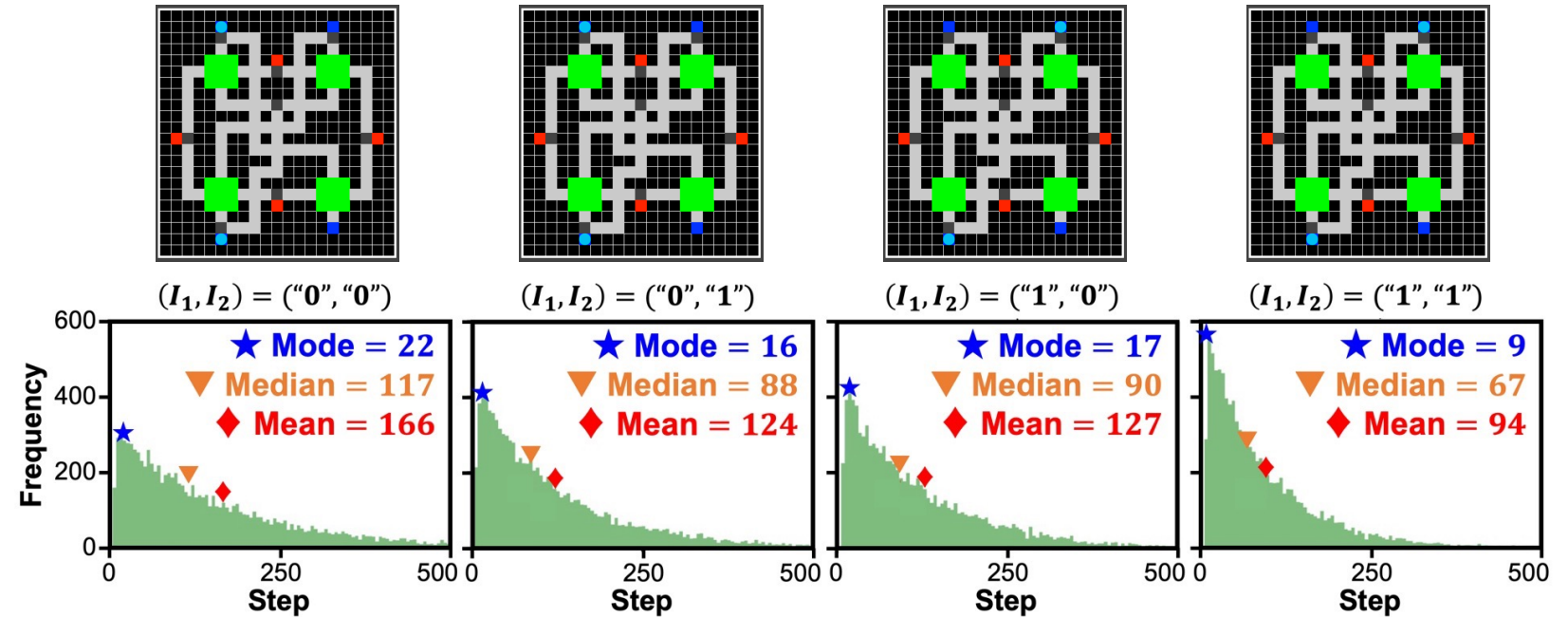
Performance Evaluations

□ Monte-Carlo Sim. for Distribution Analysis: Half-Adder



Cal. Step Distribution

$$P = \int_0^T VI_C dt \approx I_C \Phi_0 \times \#Act.$$

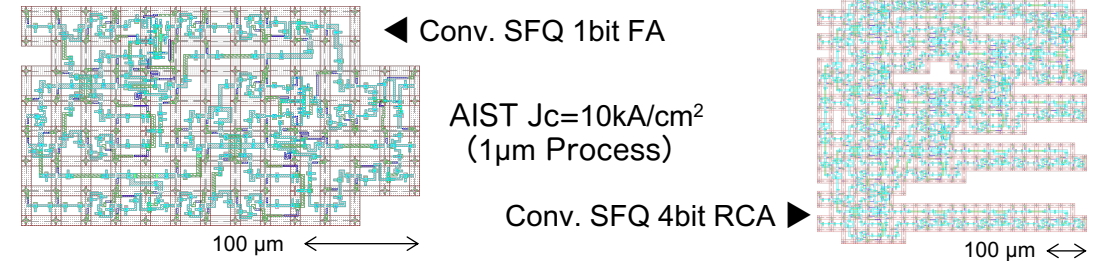
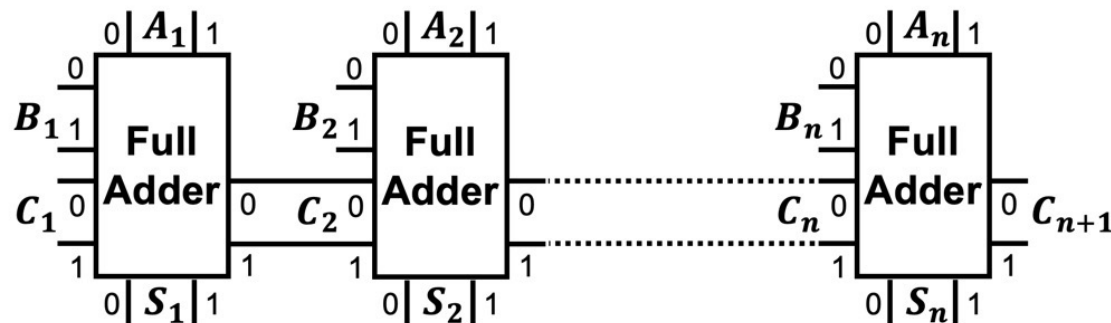
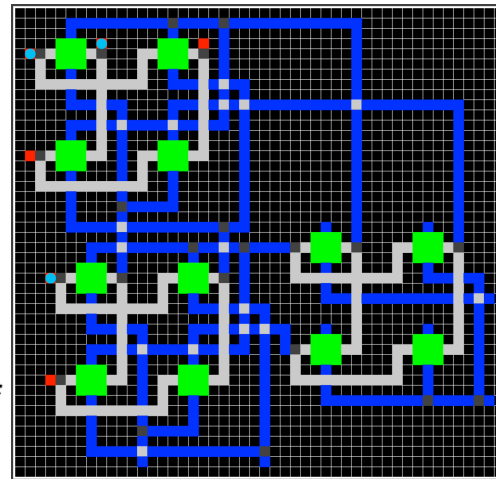
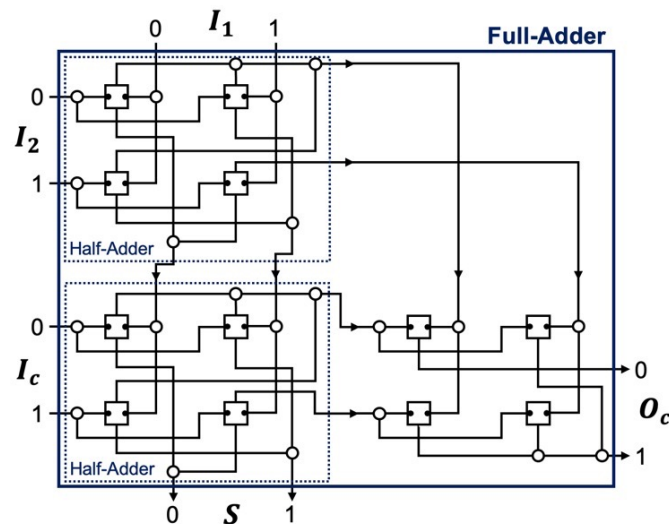


Half-Adder	Latency [ps]	Energy [aJ]	EDP [Js]
CMOS-HA (180nm)	310	43,090	13,357,900 ($\times 10^{-30}$)
Conventional SFQ-HA (1 μ m)	37.8	718.2	27,147 ($\times 10^{-30}$)
Proposed SLBC-HA (1 μ m)	179.2	0.569	102 ($\times 10^{-30}$)

Annotations: CMOS-HA to Proposed SLBC-HA: 75729x (Latency), 1262x (Energy)

Performance Evaluations

□ Monte-Carlo Sim. for Dist. Analysis: Ripple Carry Adder



	Circuits	Latency [ps]	Energy [aJ]	EDP [rJs]
1 bit	CMOS-FA (16nm)	248.5	278.3	69.2
	Conv. SFQ-FA ($1\mu\text{m}$)	33.0	2122	70.0
	SLBC-FA ($1\mu\text{m}$)	542	1.7	0.93
2 bit	CMOS-RCA (16nm)	278.4	871.3	373.8
	Conv. SFQ-RCA ($1\mu\text{m}$)	49.7	8699	432
	SLBC-RCA ($1\mu\text{m}$)	1086	3.45	3.75
3 bit	CMOS-RCA (16nm)	708.2	1520	1077
	Conv. SFQ-RCA ($1\mu\text{m}$)	66.4	15255	1013
	SLBC-RCA ($1\mu\text{m}$)	1625	5.17	8.39
4 bit	CMOS-RCA (16nm)	938.1	2495	2341
	Conv. SFQ-RCA ($1\mu\text{m}$)	83.1	21822	1813
	SLBC-RCA ($1\mu\text{m}$)	2167	6.89	14.9

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Conclusions

□ We propose a new computing method with SFQ devices

1. How do we calculate with uncontrollable devices? [Computational Principle]
 - New computing principle: the “SFQ Brownian Logic Circuit”
2. What are the devices? [Devices]
 - Random walk circuit implementation with SFQ devices
3. What are the structures for the implementation? [Circuit]
 - Several processing units show the potencial. (Over 1/1000x energy reductions)
4. How do we estimate the potential? [Evaluation Methodology]
 - Monte Carlo simulator for the proposed circuit

□ Towards Ultra-Low Power Computing

- One of the new paradigms for SFQ computing
- Unique feature: The result is deterministic, time is non-deterministic
- Chip-based PoC, Guaranteeing worst-case execution time

Thank you for your kind attention!!

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