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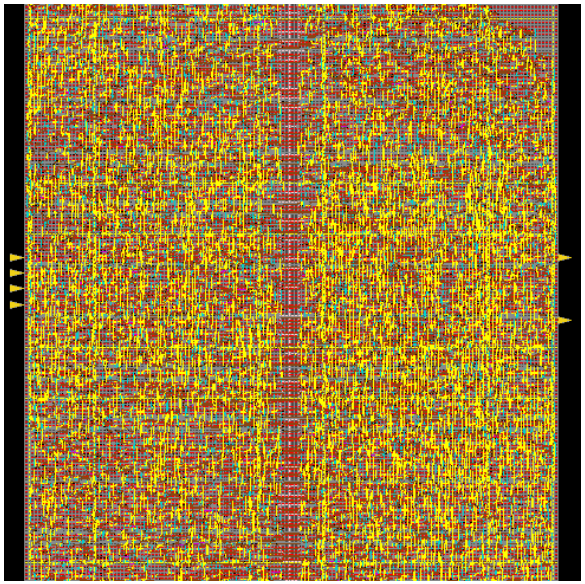
Advanced Modeling Tools for the Development of Superconducting Circuits



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October 25-27, 2025

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Outline

- Motivation
- Automated Place and Route with On-the-Fly Inductor Modeling
- Flux Trapping Simulator – 3D Ginzburg-Landau
- Quantum Circuit Simulation – Circuitizer

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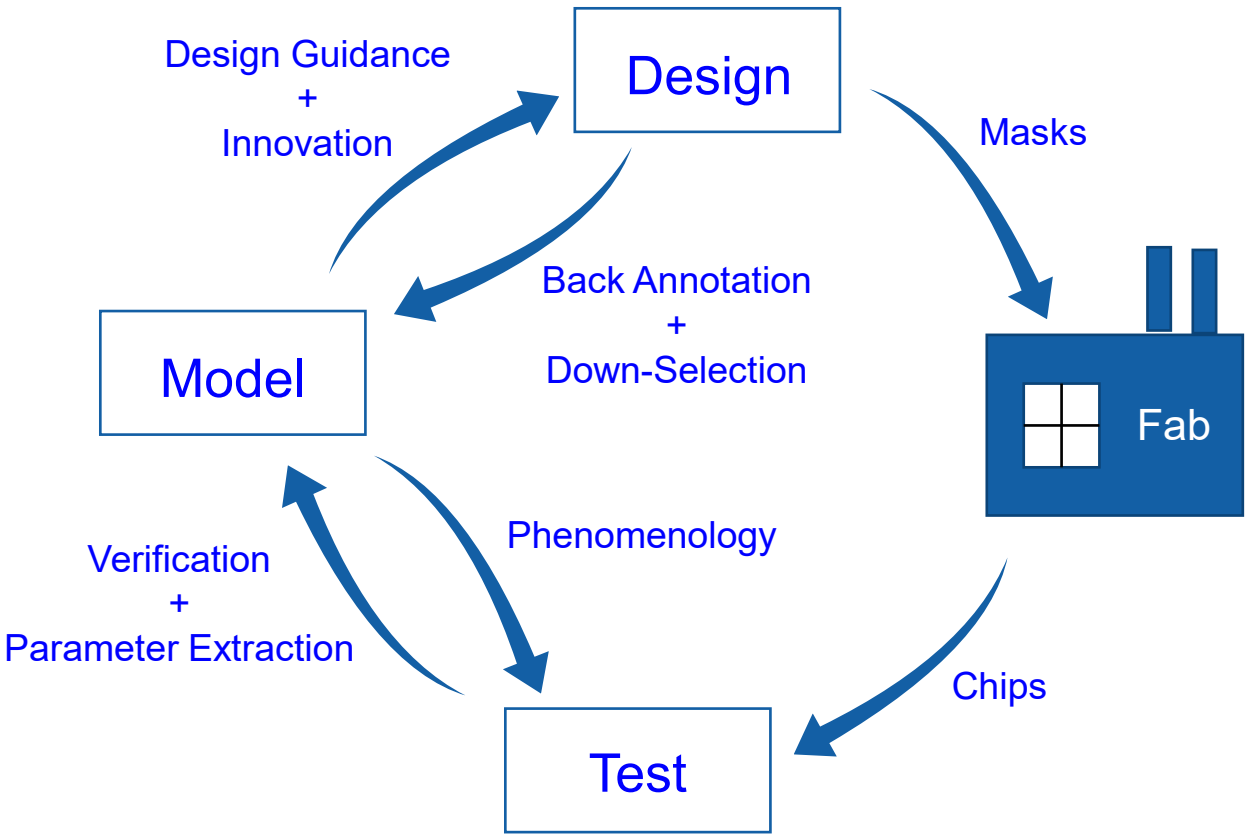
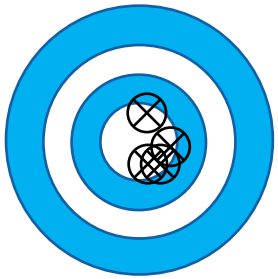
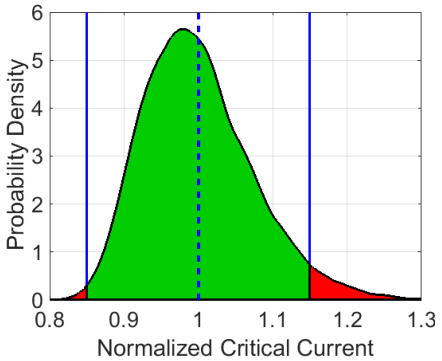
A Well-Informed Model is Critical to a Successful Design-Fab-Test Cycle



Prediction of Performance



Statistics



- The model drives innovation and puts the design on target.
- It is a window into the device behavior and is necessary for extracting device parameters.
- Good = Bullseye Better = Target Shape Great = Predicts Spread

Automated Place and Route Enabled by Inductor Modeling

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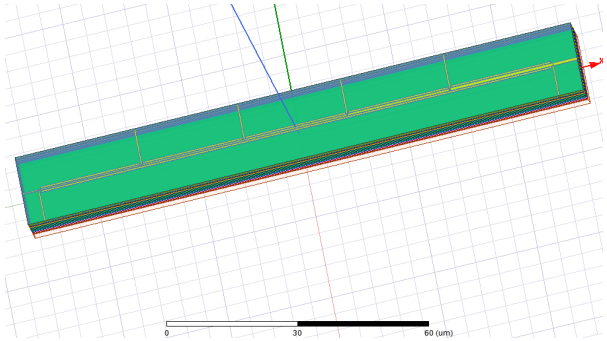
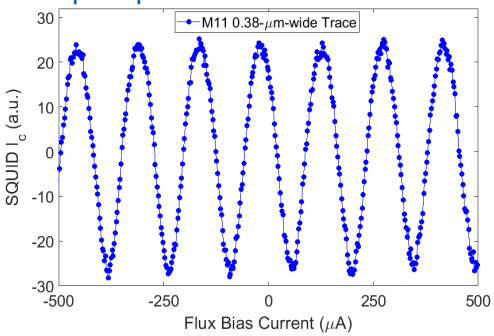
Informed Models are Necessary for Well-Targeted RQL Circuits

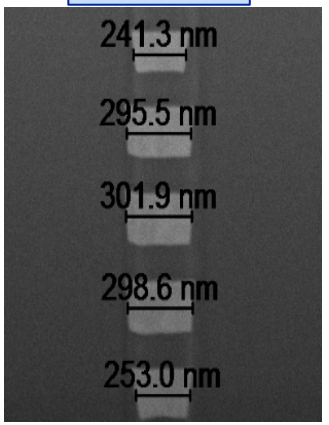
HFSS™ Model of Inductor



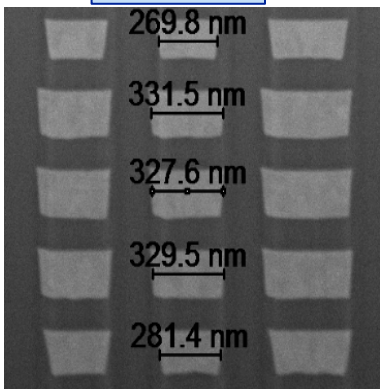
Φ_0 Inductance Measurement



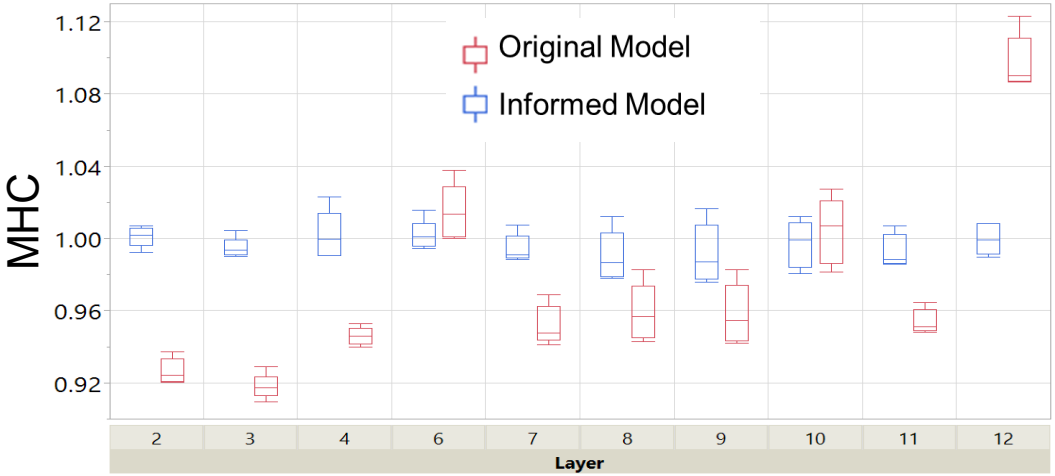
"Isolated"



"Dense"



Model to Hardware Correlation



- HFSS™ inductor model showed poor model-to-hardware correlation (MHC) initially
- Investigation of wire thicknesses and λ showed dependence on local metal density
- New inductor designs informed by density-aware model showed great MHC!

[1] Ansys and HFSS are trademarks of Ansys, Inc.

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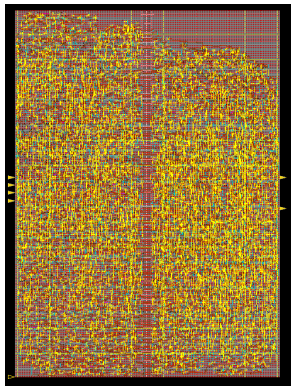
Lightweight Model Informed by 3D EM Simulations Enables On-The-Fly Inductance Extraction

Cadence® Innovus™



Routed Design

LEF/DEF

On-The-Fly Inductance Extractors

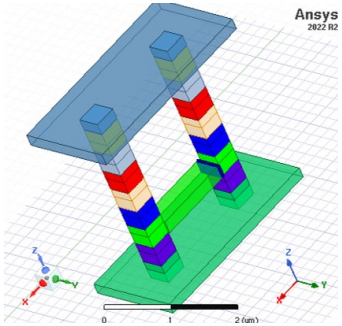
Cadence® NanoRoute® Extraction

Prototype For

NG Inductance Checker

Compact Models

Ansys® HFSS™



E&M Simulations

Extraction Report

netName1	self1	netname2	self2	mutual
FE_OFN105_n	20.845259	u_enable_in_reg/FE_OFN89_sr_q_1__0	30.147332	-0.037489
FE_OFN105_n	20.845259	u_enable_in_reg/sr_q\[1\][0]	28.511142	-0.080836
FE_OFN108_n	21.970794	u_enable_in_reg/FE_OFN133_n	30.383416	-0.723660
FE_OFN108_n	21.970794	u_enable_in_reg/FE_OFN92_sr_q_0__0	28.511142	-0.044034
FE_OFN110_n	30.991354	u_data_in_reg/FE_PHASE_PAD_N165_io_net_data_in	25.437207	-0.021165
FE_OFN110_n	30.991354	u_enable_in_reg/FE_PHASE_PAD_N178_io_net_enable_in	25.530116	-0.039807
FE_OFN110_n	30.991354	u_enable_ret_reg/FE_OFN117_n	30.138479	0.012990

Cadence® NanoRoute®

Cadence® V4 Timing

NG SIRQL

Routing Closure to Target Ind Spec

Timing & Verification

Failure Detection

Margin Degradation

Current Specification

- 3D EM models are too resource intensive for on-the-fly inductor generation.
- 3D model results were used to develop polynomial-based inductor model that runs fast.
- Automated place and route tools build complicated RQL layouts from schematics.

[1] Ansys and HFSS are trademarks of Ansys, Inc.

[1] Cadence, Innovus, and NanoRoute are trademarks of Cadence Design Systems.

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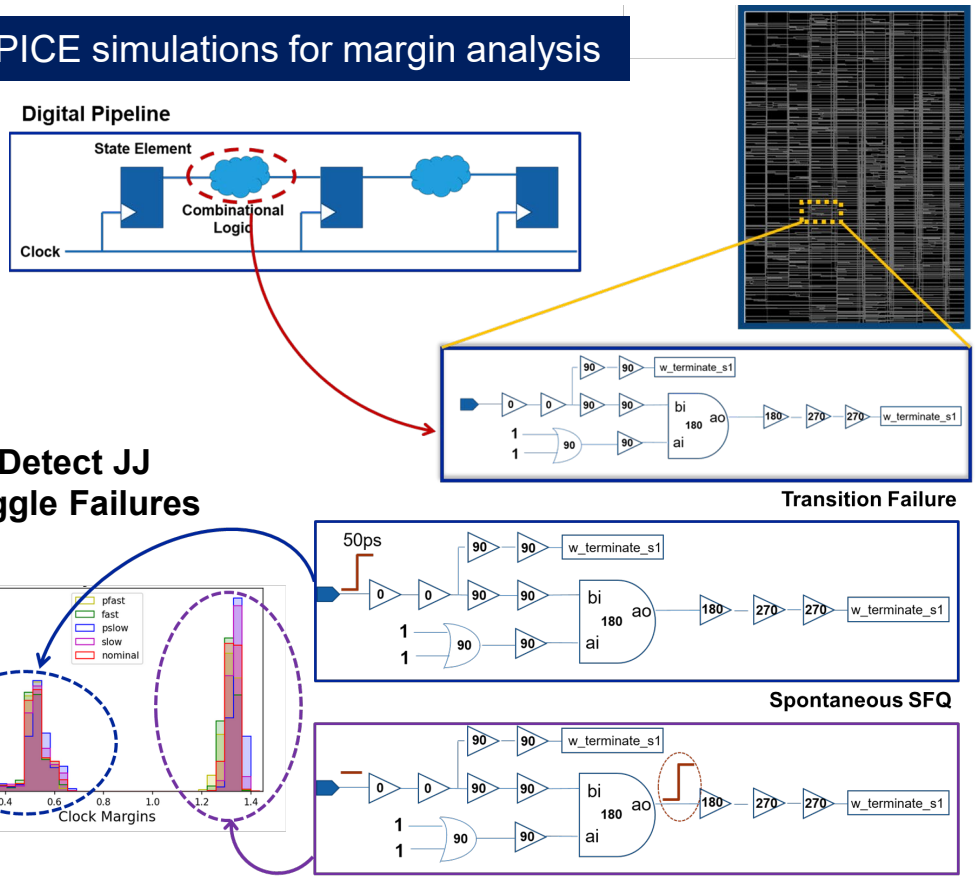
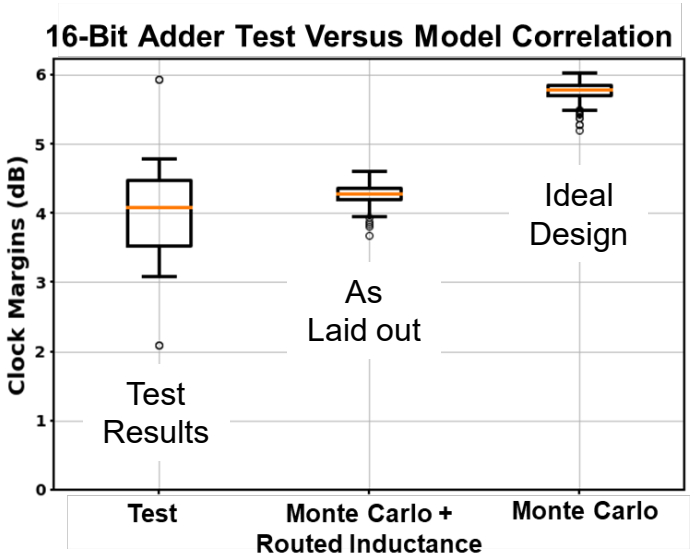
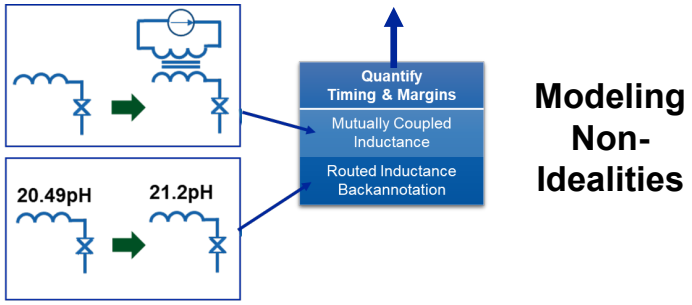
Margin Verification with Back-Annotated Inductance Provides Predictive Model-to-Hardware Performance

SPICE simulations for margin analysis







- 16-bit RQL adder laid out with automated place and route flow
- Test showed reduced margins compared to initial design model
- After back-annotation, simulated margins agree with measured performance!

Flux Trapping Simulator

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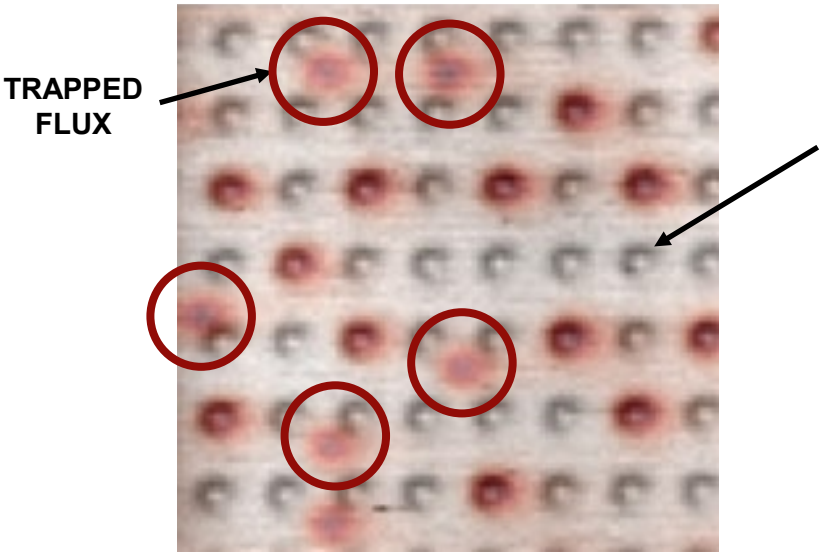
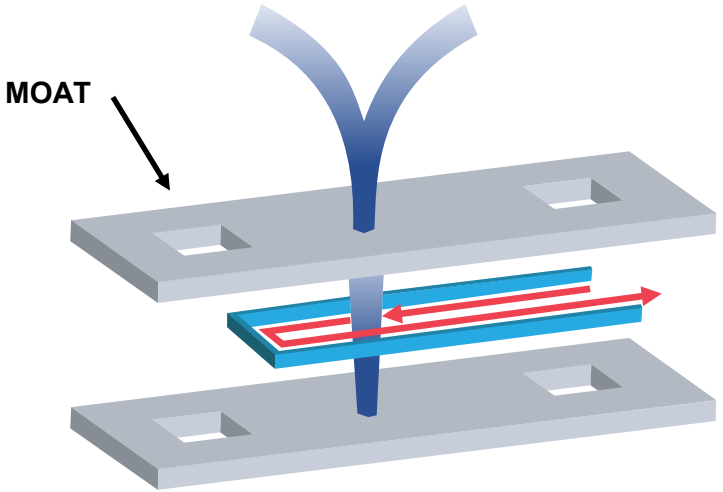
Superconducting Digital Circuits Fail Intermittently Due to Trapped Flux Vortices

SSM Magnetometry-Susceptometry Overlay



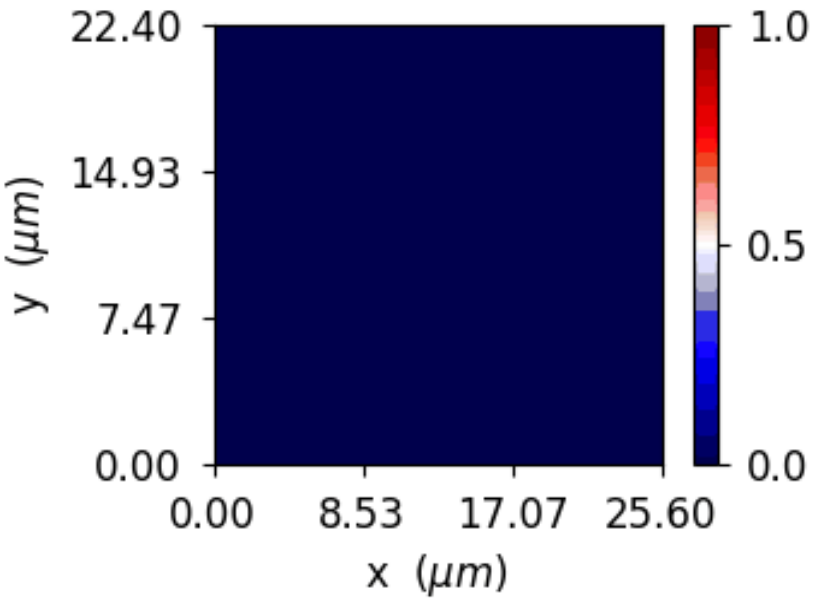
Two Ground Planes with Trapped Flux Threading an Inductor



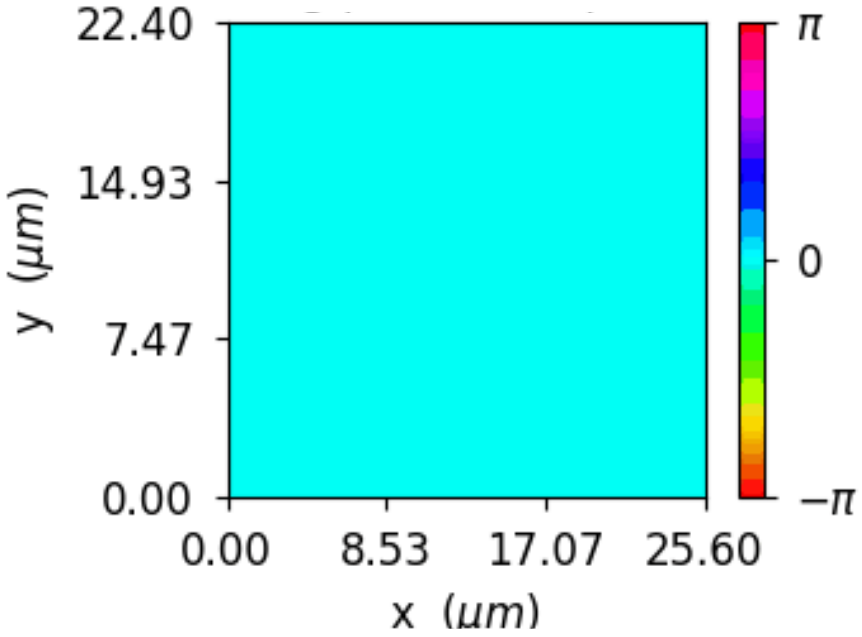
- Pinned flux vortices apply current offsets to digital gates that interrupt operation
- Holes in superconducting ground planes help to safely sequester flux vortices
- Sub-optimal moat designs can reduce moat effectiveness

Flux Trapping Simulator Developed at Northrop Grumman to Inform the Design of Flux Sequestration Moats

Cooper Pair Density and Supercurrent



Ginzburg-Landau Phase



- FTS is a 3D Ginzburg-Landau physics simulator
- Optimized for HPC utilization. More cores enable larger models!
- Capable of performing time-dependent simulations of vortex nucleation and motion

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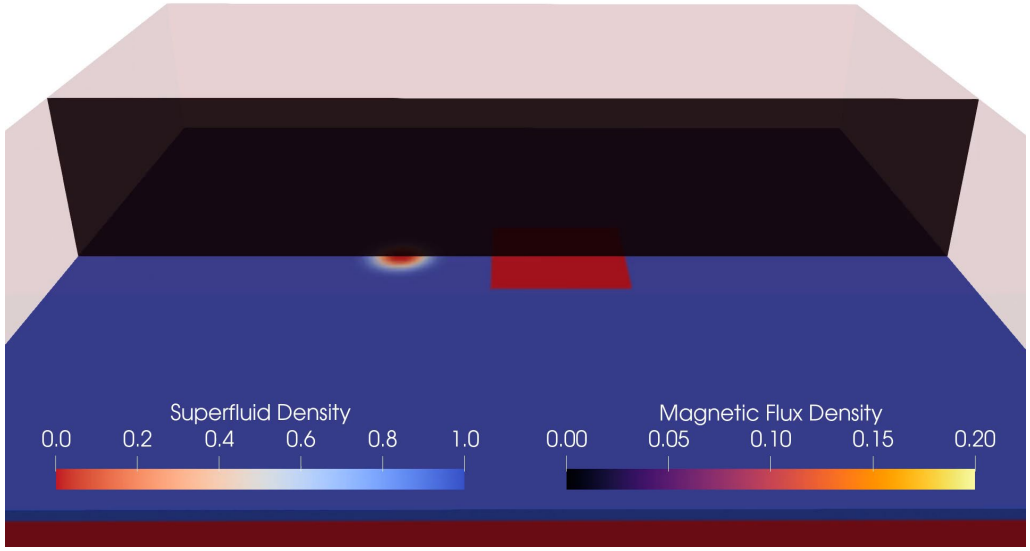
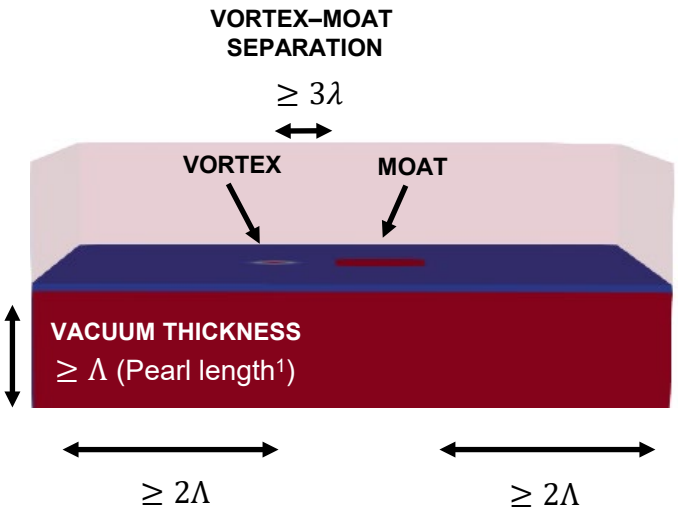
Moat Attraction Forces Derived from Time-Dependent Vortex Simulations Match Literature Values



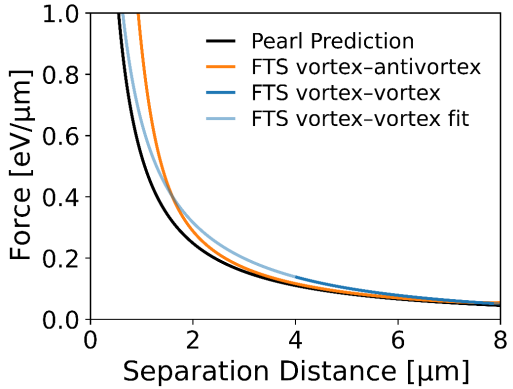
Vortex-Moat Simulation Setup



$$u_{\mathrm{Pearl}}(r) = \frac{\Phi_0^2}{2\mu_0 \Lambda}\left[\mathbf{H}_0\left(\frac{r}{\Lambda}\right) - Y_0\left(\frac{r}{\Lambda}\right)\right]$$

[1] J. Pearl, *Appl. Phys. Lett.* **5**, 65–66 (1964).

Computed vs. Predicted Vortex Interactions



- Predictions of interactions between vortices in thin films are well established in the literature.
- Moat attraction force models are used to determine the optimal moat spacing
- As the model is validated further, it can be used to save expensive empirical design-fab-test cycles when searching for the best moat pattern

[1] Applied Physics Letters owned by AIP Publishing, subsidiary of American Institute of Physics

Quantum Circuit Simulation: Circuitizer

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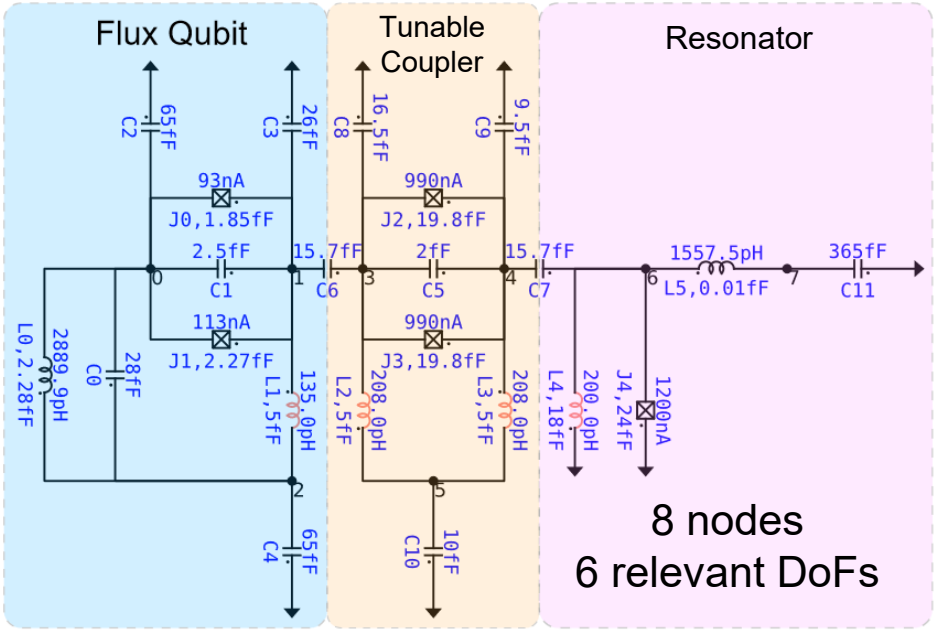
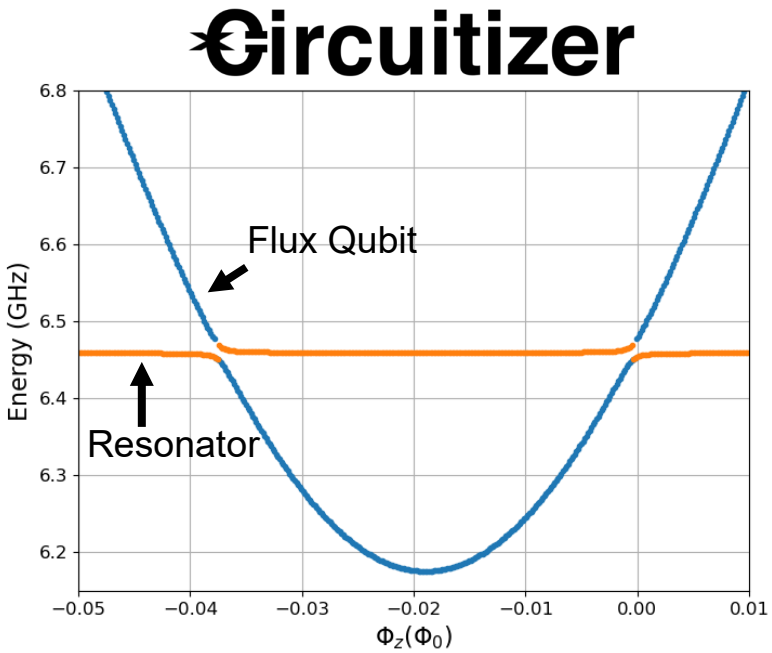
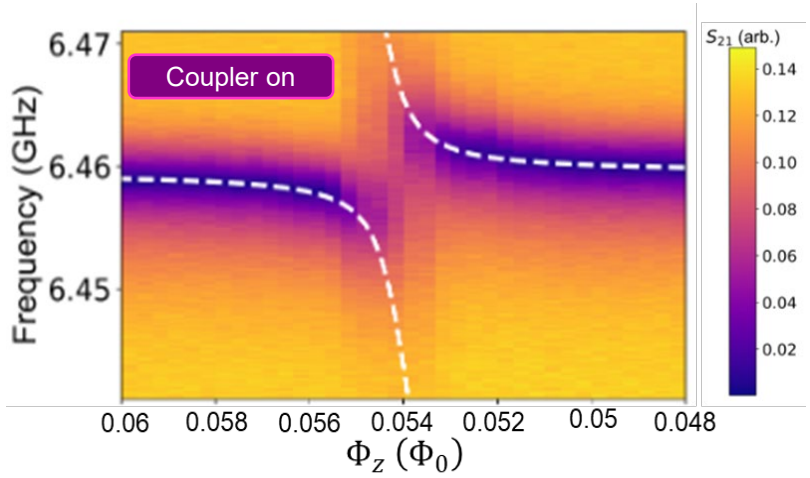
Circuitizer Automatically Generates Quantum Hamiltonians from Circuit Schematics



*Grover, et al., PRX Quantum **1**, 020314 (2020)



- Handles Josephson junctions, capacitors, inductors, and some composite elements
- Supports external flux and voltage bias controls
- Test results of this tunable coupler circuit match the eigenenergies calculated in Circuitizer model



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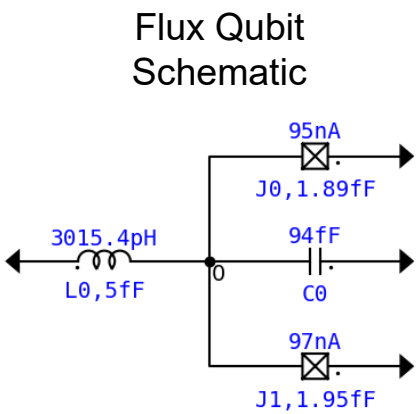
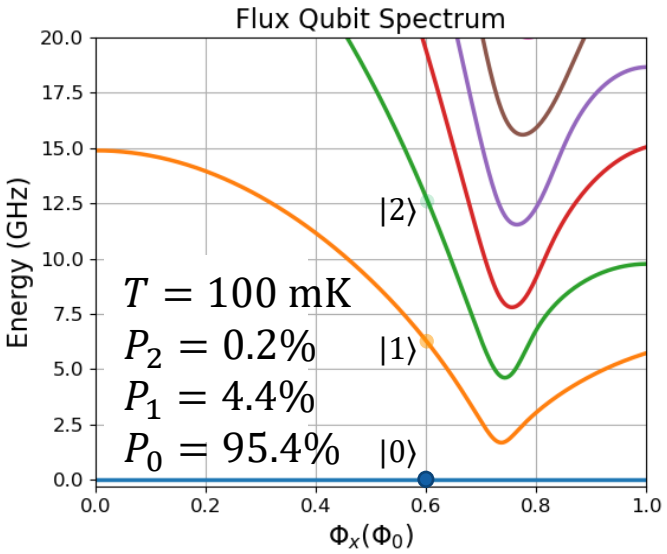
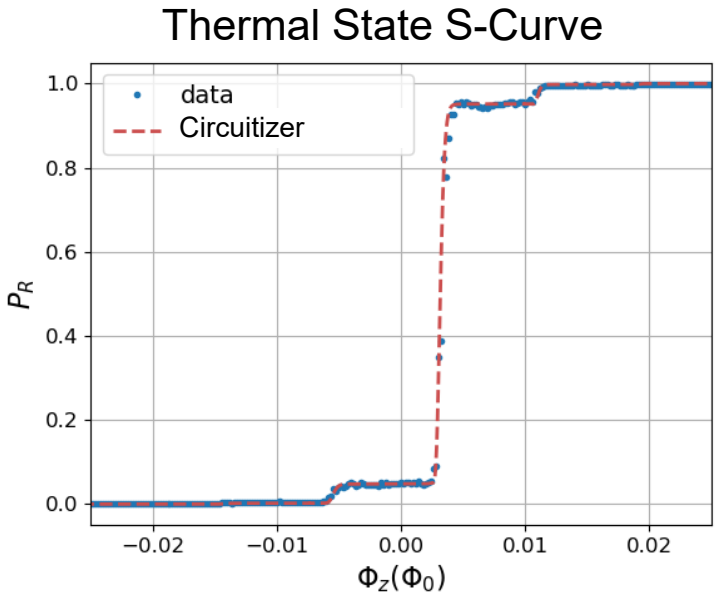
Time Domain Simulations of Quantum Processes Agree with Observed Device Performance







- Circuitizer capable of modeling evolution of quantum states under time-dependent current and voltage controls.
- Flux qubits undergo a transformation from oscillator-like states to circulating current states during annealing.
- Measurements revealed anomalous steps in the S-curve.
- Circuitizer simulations of the annealing process illuminated thermal population as the source.

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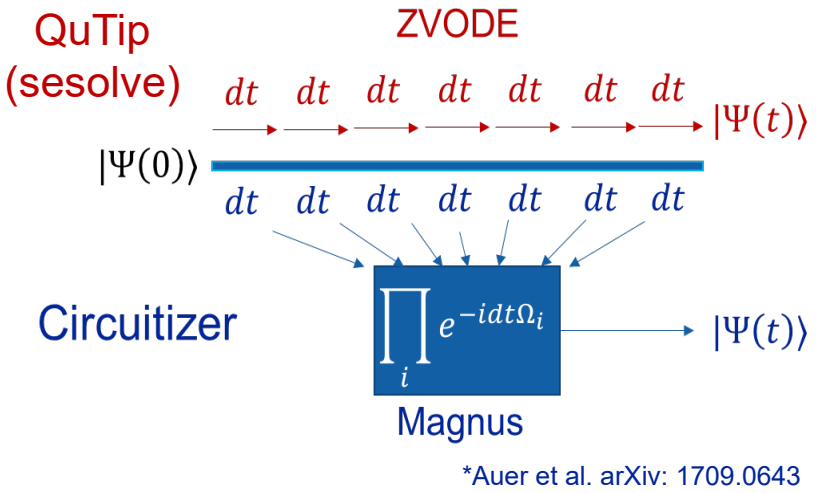
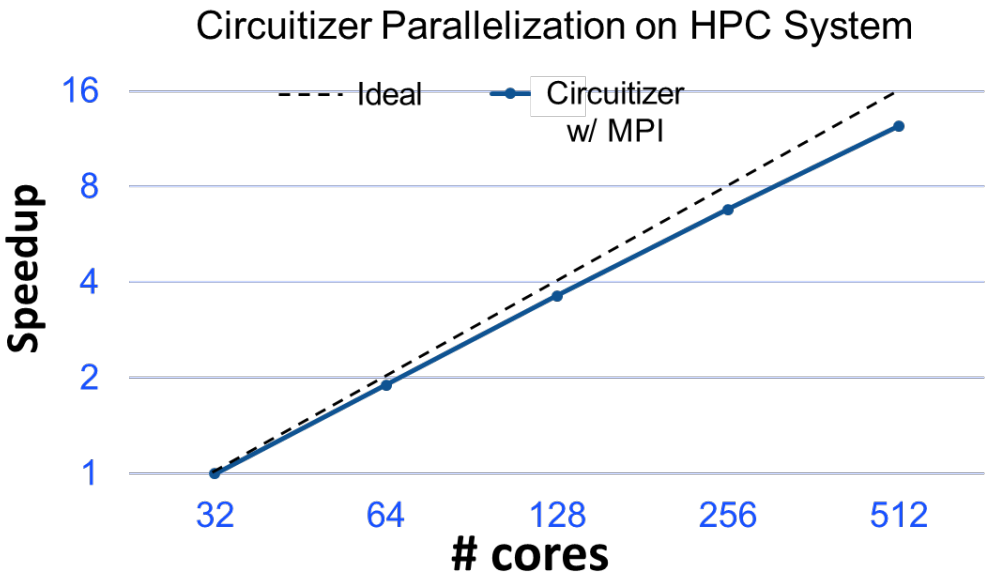
Circuitizer Utilizes Computational Resources to Speed Up Quantum Simulations

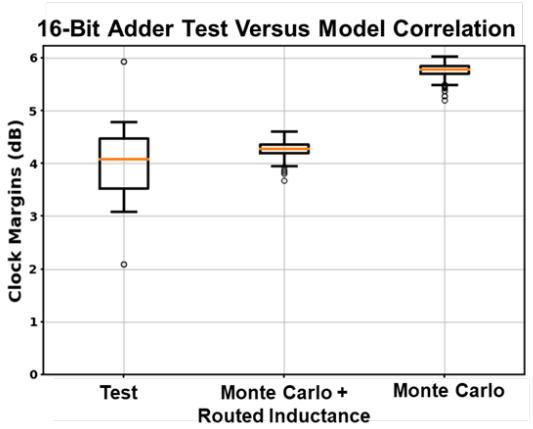


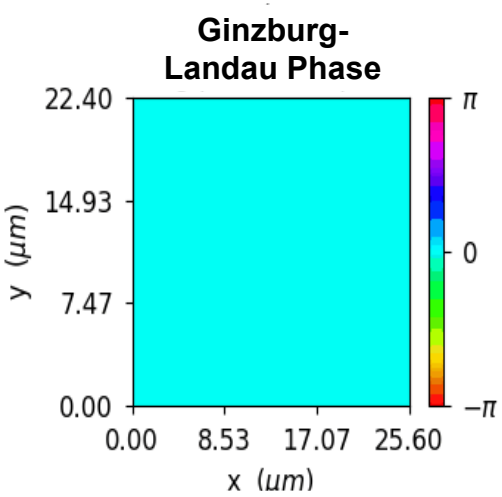
*Auer et al. arXiv: 1709.0643

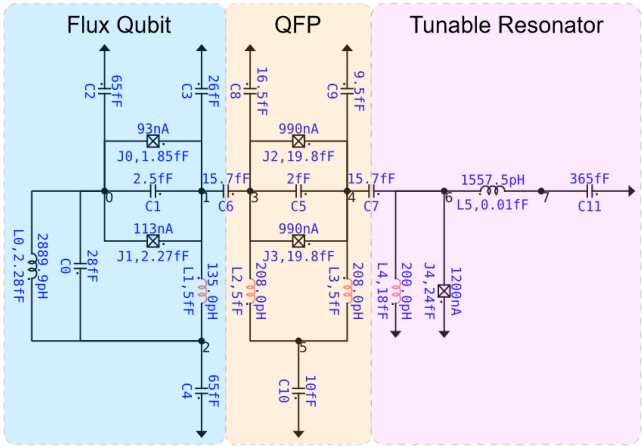


- Conventional state evolution is slow because time integration steps must be evaluated serially.
- Circuitizer maps finite time integration steps to effective propagators, Ω_i, and calculates them in parallel.
  - The big time cost is computing eigenstates at each time step.
- Benchmarking of parallel eigensolves on HPC system show favorable performance compared to ideal multiplicative speedup.

Summary







- Well-informed, experimentally validated inductor model enables automated place and route of complex RQL digital circuitry
- Northrop Grumman has built a 3D GL simulator to model flux trapping and inform the design of superconducting ground plane moat arrays
- Circuitizer performs quantum simulations of arbitrary schematics with support for time-dependent control signals and demonstrated speed-up on HPC

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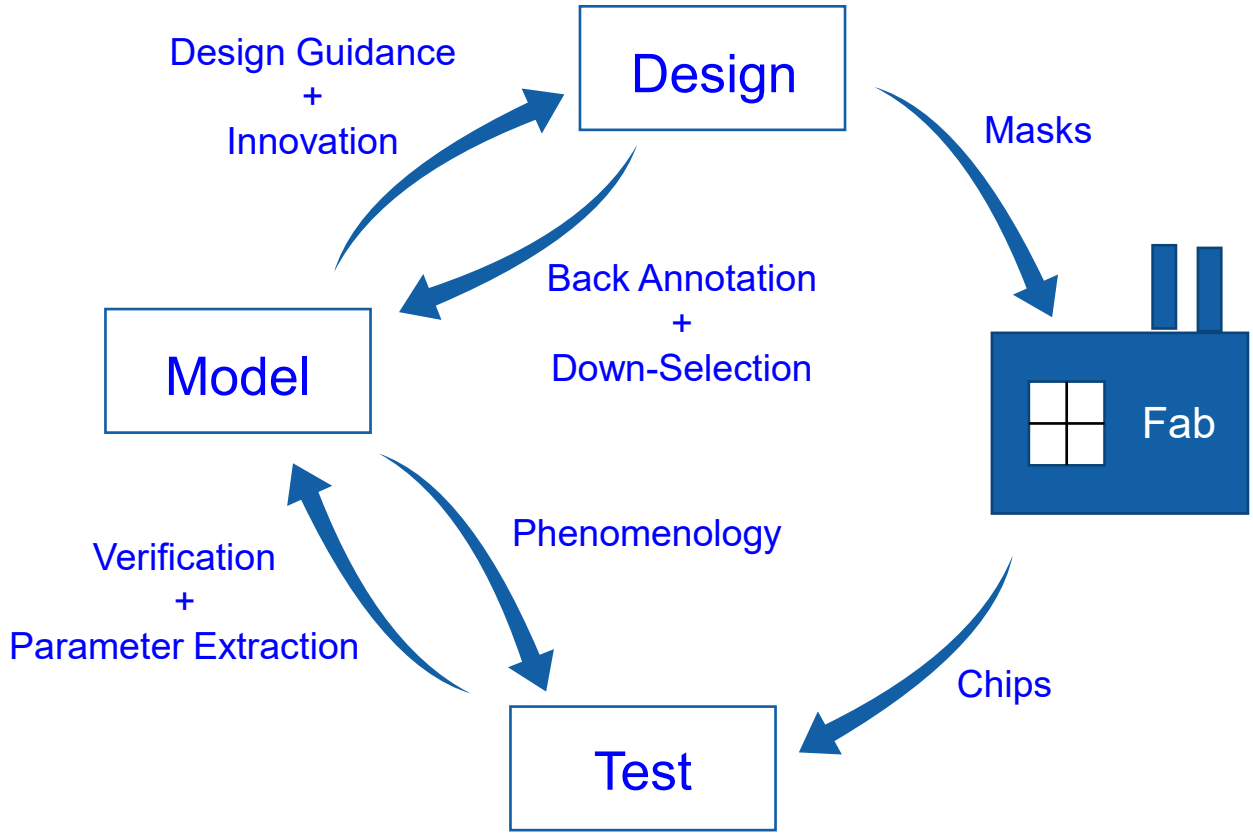
A Well-Informed Model Drives Successful Technology Development



Thank you very much! Any Questions?

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