From SFQ to Quantum Sensing: A versatile NbTiN superconducting digital platform

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SuperConducting Digital (SCD) at imec

US team:
- Circuit design and simulation
- Mask design
- Cryogenic characterization

NeoCity, Florida

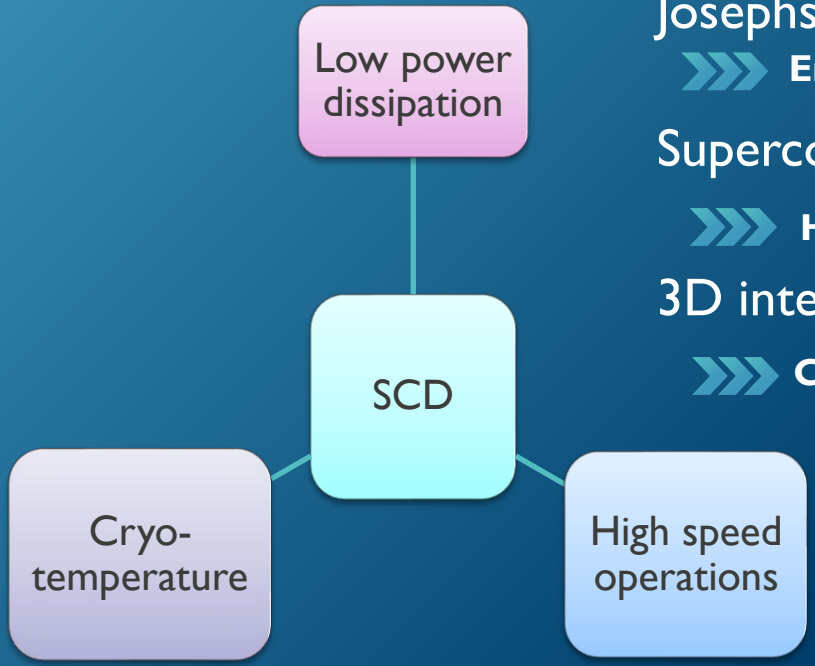
Leuven, BE (HQ)

Belgium team:
- Fabrication
- System and Architecture
- Material & device characterization

12,000 M² CLEANROOM
CAPACITY

>25 SKILLED PEOPLE
FROM OVER 9 NATIONALITIES

Superconducting Digital Logic (SCD)



Josephson Junction Logic
- **Energy efficient**

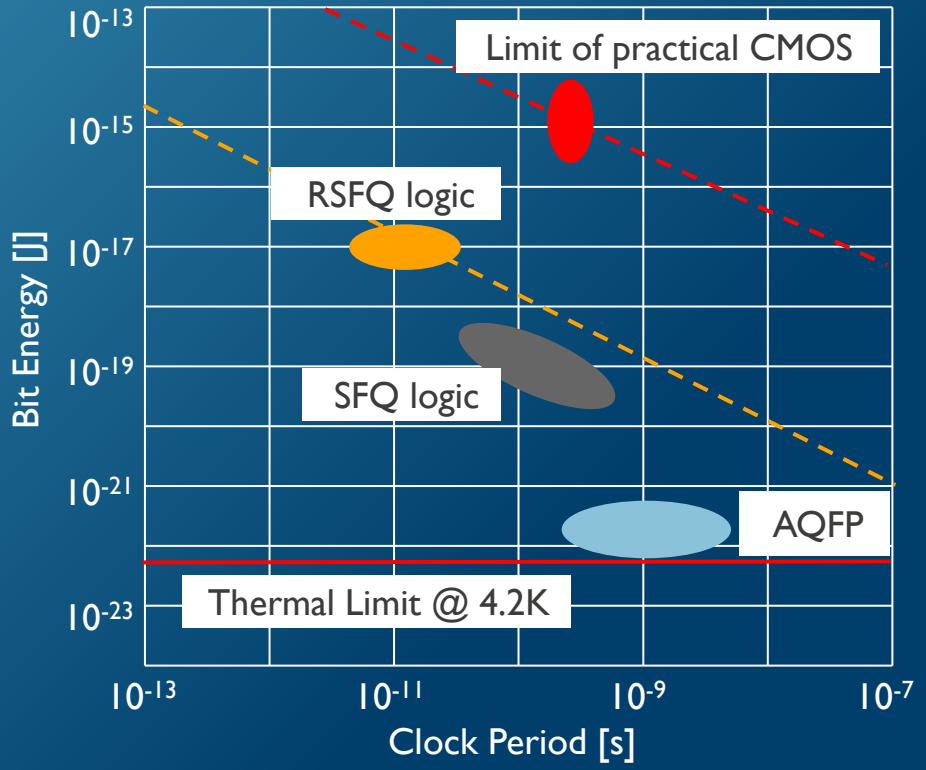
Superconducting backplane
- **High Bandwidth**

3D integration
- **Cryo CMOS and Optical**

A DATA CENTER IN A SHOEBOX

IMEC'S VISION TO USE SUPERCONDUCTORS TO SHRINK COMPUTERS

Single-Flux-Quantum (SFQ) Circuits



SFQ circuits can reduce switching energy by >1000x

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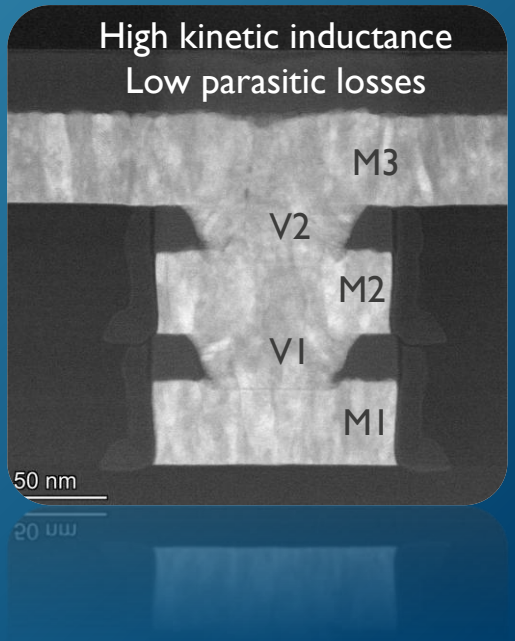
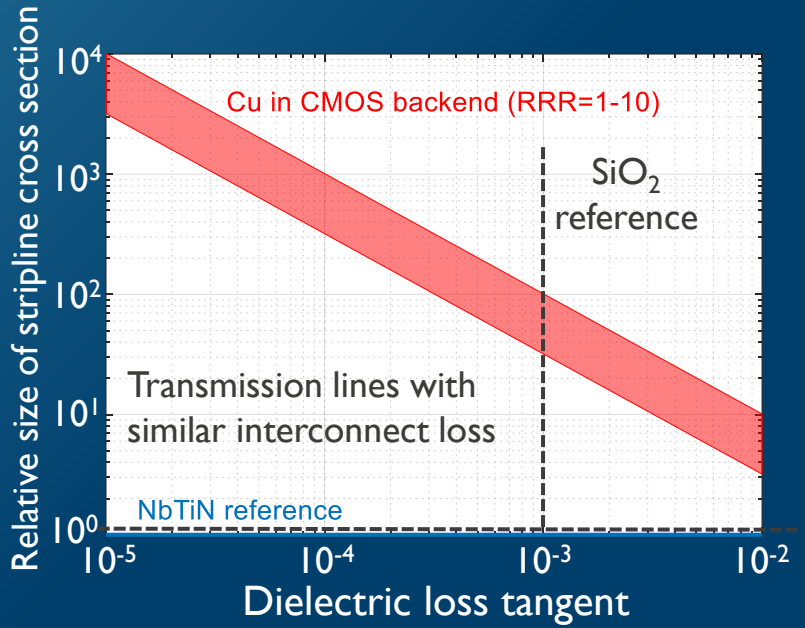
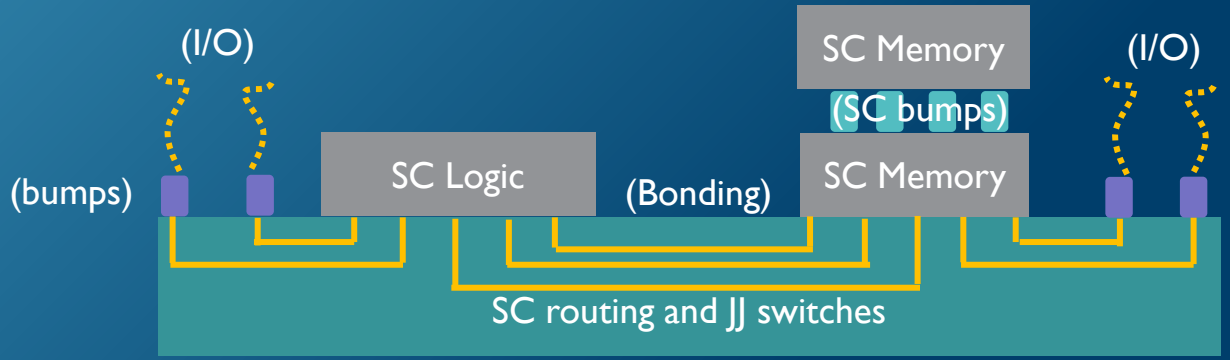
Superconducting Transmission Lines





NbTiN interconnects are 1000x better at >100Gb/s bandwidth at 4.2K

Superconducting 3D



Heterogeneous Integration with CMOS Quantum and Photonics

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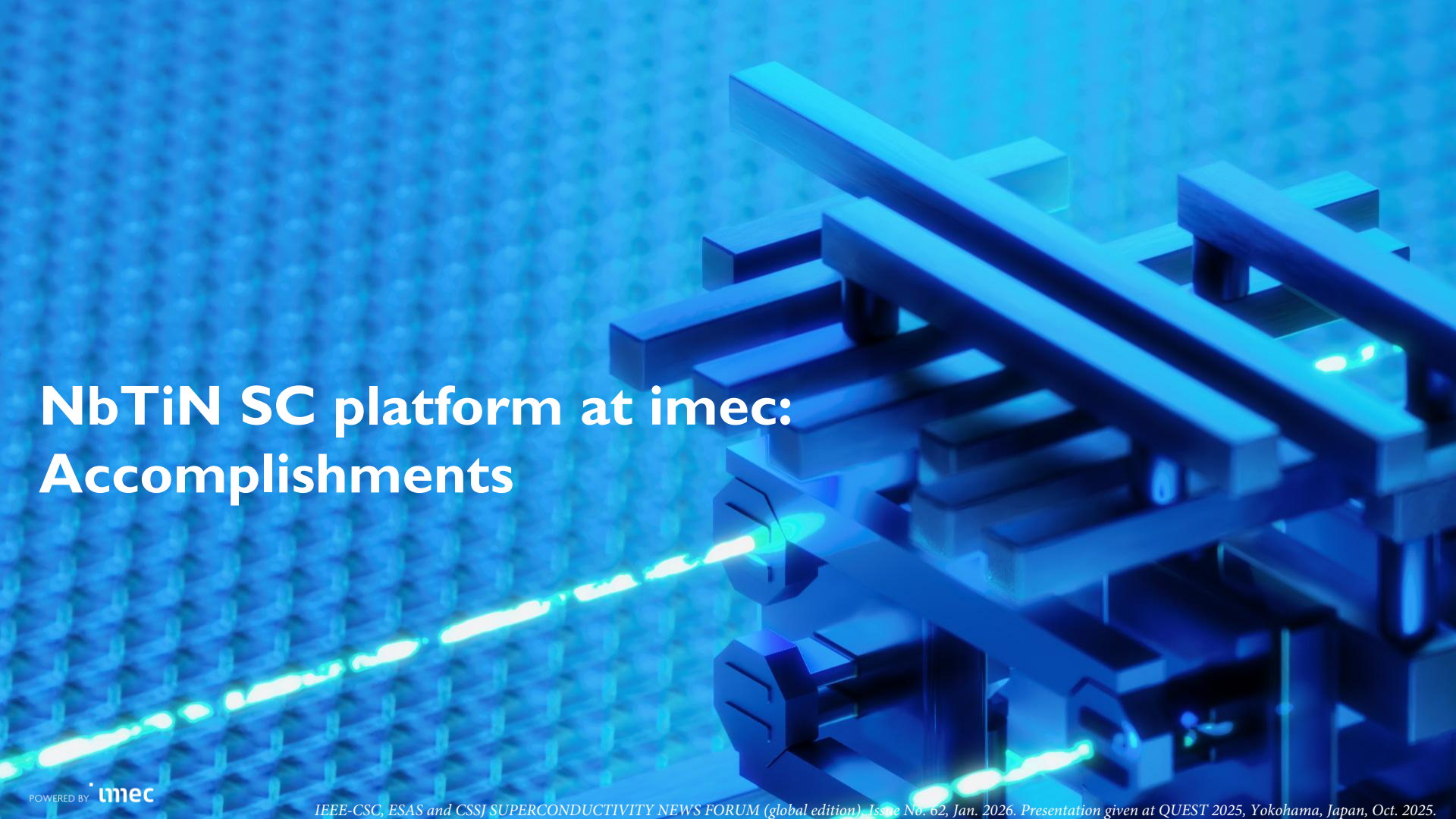
NbTiN SC platform at imec: Accomplishments



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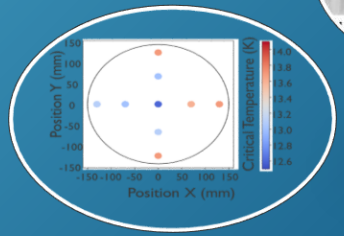
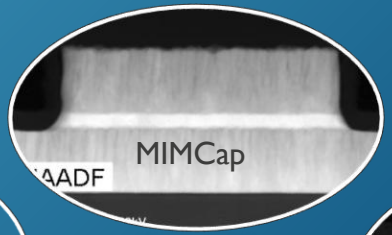
Superconducting Digital Logic (SCD)

State-of-the-art **Nb** technology		**NbTiN** technology
200°C budget	Process compatibility	>420°C budget
250 nm feature size	Device density	50 nm feature size
200 mm wafers	Process scalability	300 mm wafers
T_C ~ 9 K	Material properties	T_C > 13 K
Low L_{kinetic}	Inductor density	High L_{kinetic}
AlOx	Junction Area	αSi

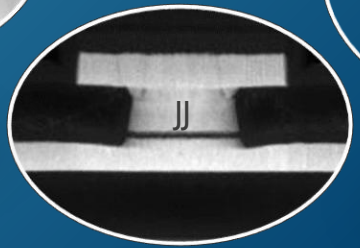
NbTiN SC platform at imec



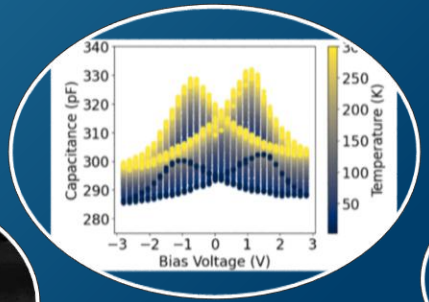
SC NbTiN film



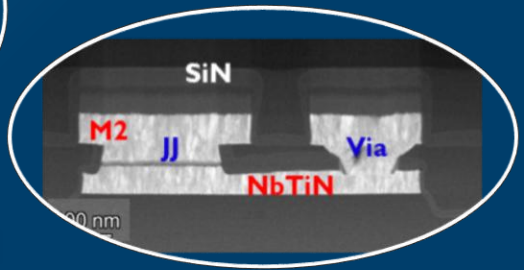
Varactor (low *f*)



First JJ fabrication



MIMCaps meet specs (high *f*)

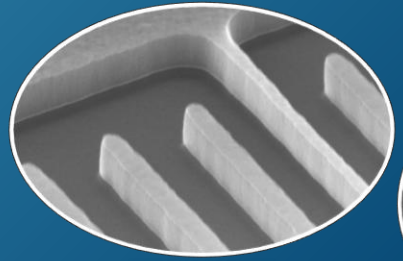


2ML JJ + vias

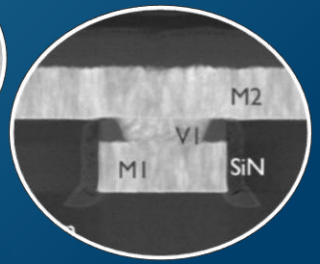
2022

Q1'22 Q2'22 Q3'22 Q4'22 Q1'23 Q2'23 Q3'23 Q4'23 Q1'24 Q2'24 Q3'24 Q4'24 Q1'25 Q2'25 Q3'25

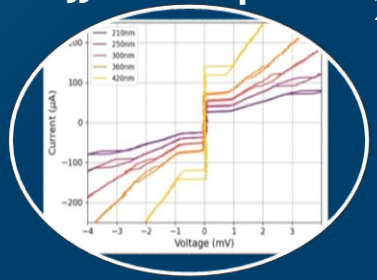
50 nm NbTiN wires



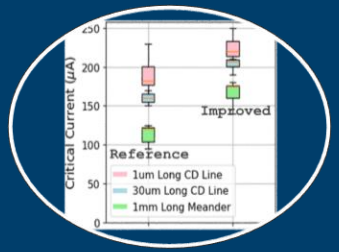
50 nm 2ML BEOL



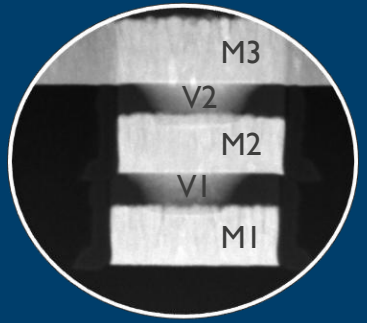
JJs meet spec



2X *Ic* (2ML BEOL)

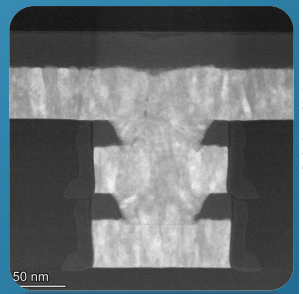


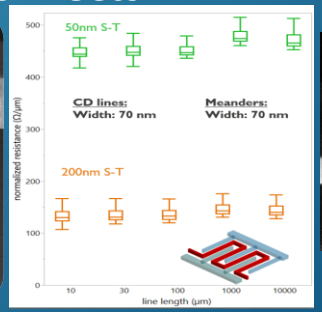
3ML BEOL



NbTiN SC platform: unit process development

Interconnects





New Material: NbTiN

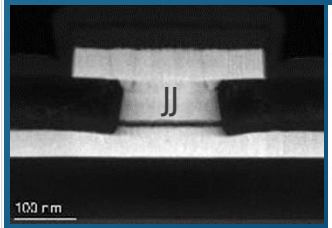
Litho: 193i (50nm CD)

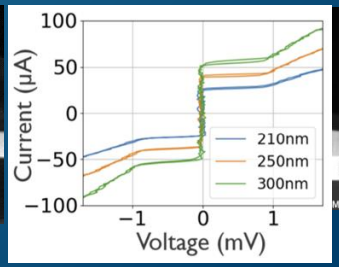
Process: PVD semi-damascene

High density routing

Low loss interconnects

Josephson junctions





New stack: NbTiN/aSi/NbTiN

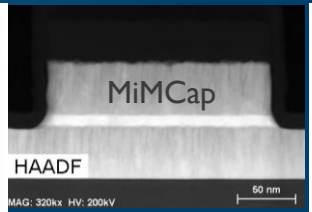
Litho: 193i (210nm CD)

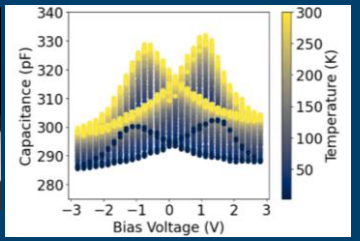
Process: PVD & etch

Density logic and memory 4 MJJ/mm^2

Clock speed 30 GHz

Capacitors





New stack: NbTiN/HZO/NbTiN

Litho: 193i (195nm CD)

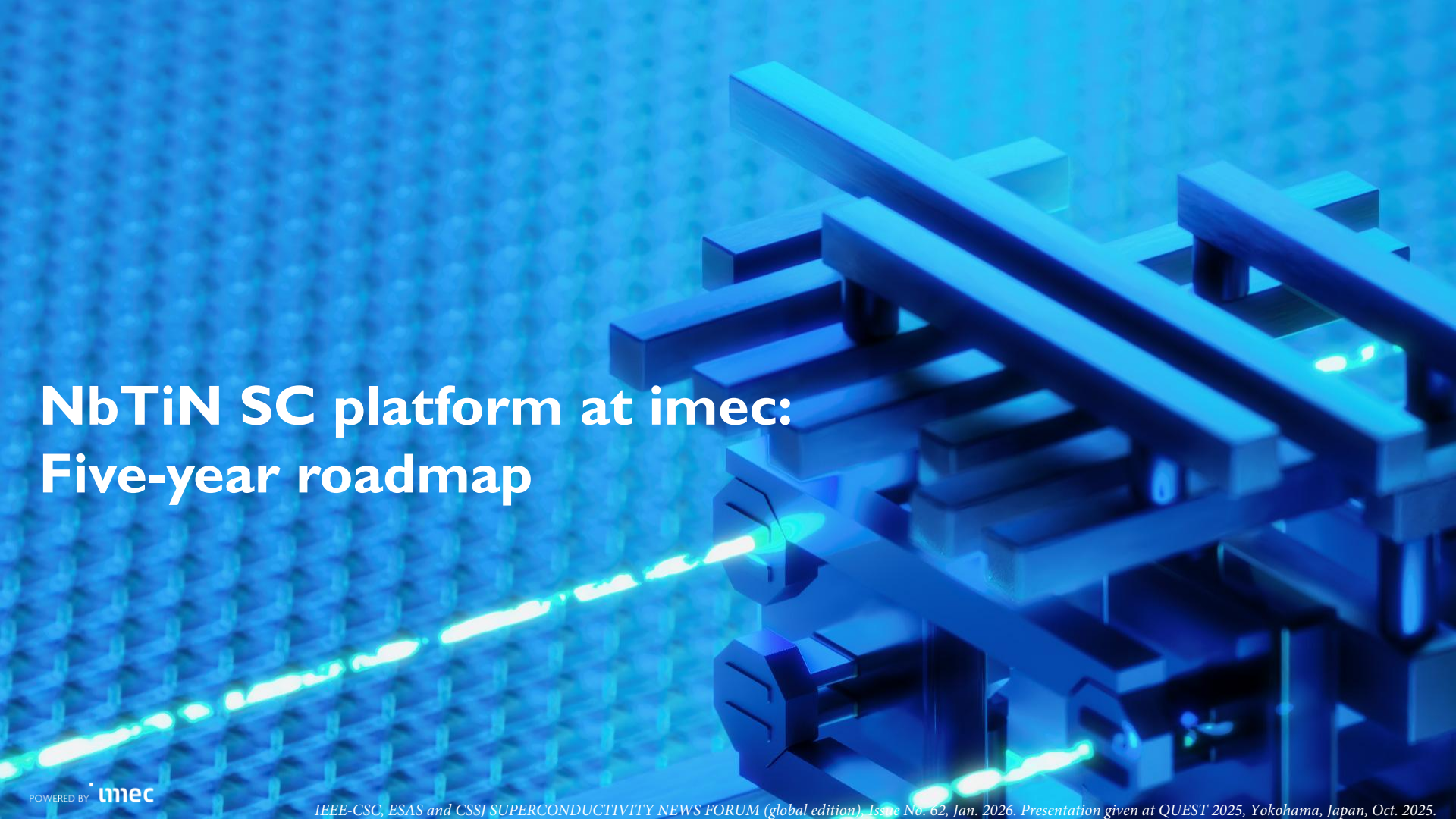
Process: PVD (NbTiN), ALD (HZO) & etch

Dense power delivery

Tunable AC power delivery 30 GHz

Electrical demonstration of key building blocks of NbTiN SC platform

NbTiN SC platform at imec: Five-year roadmap



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Timeline: Process Technology

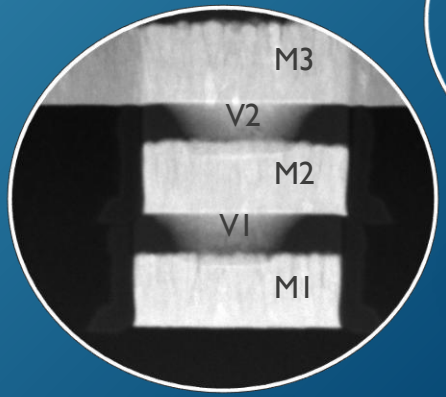
2025	2026		2027		2028		2029		2030	
H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2

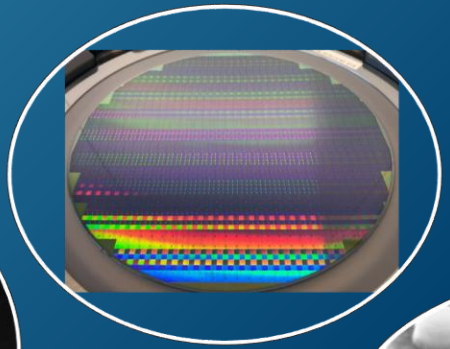
Baseline Calibration to Specs (2ML/3ML): JJ, Resistors, Inductors, Capacitors, Wires & Vias

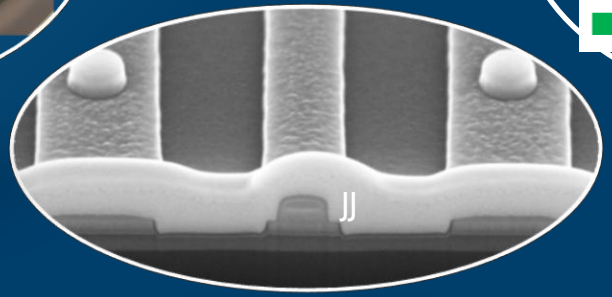
Pathfinding, Device & Process optimization (3ML/5ML)

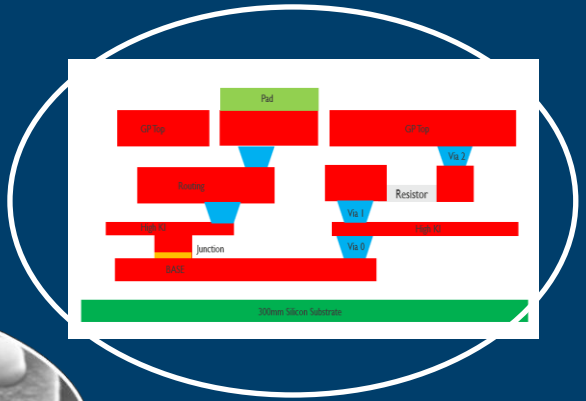
Process optimization (3ML/5ML) Platform Flow for MPW

Process optimization (5ML/7ML), integration with new materials and technologies (CMOS Photonics III-V)









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Timeline: DTCO

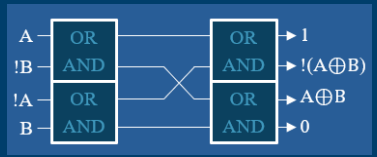
2025	2026		2027		2028		2029		2030	
H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2

Device Modeling and PEX extraction → Standard cell libs and memory → Advanced core lib and memory macro → Macro design, benchmark suites & verification flows

RTL

Verilog Design

Design Database



Gate-Level Netlist

synthesize

PCL Gate libaray and memory macros

Starling EDA Tool

- Uses Python to generate a graph model for the Verilog netlist
- Performs modifications for
  - Single to dual rail conversion
  - Splitter insertion
  - Phase balancing
- Writes the modified netlist back to Verilog

Superconducting Netlist

Translate the netlist using a custom tool

Timing/Noise

Superconducting Simulation Library

Place & Route

JTL insertion-flux-inductance

GDS -> FAB

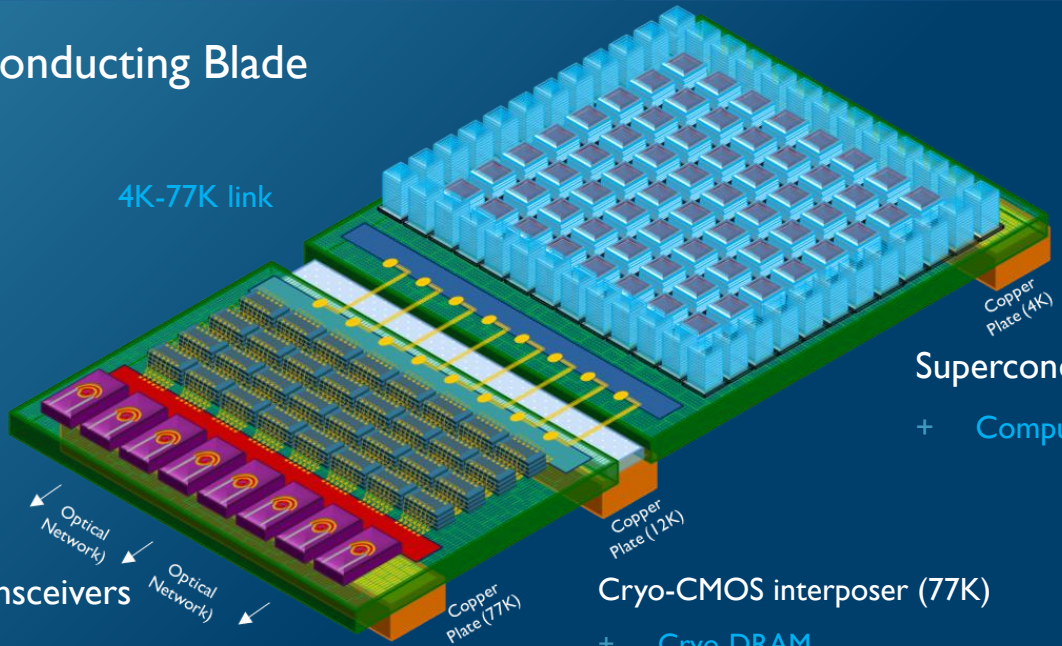
Final layout for 7 metal layer process

Timeline: Cryo-Packaging

2025	2026		2027		2028		2029		2030	
H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2

Materials development for high bandwidth 2.5D → Scaled up testing of 2.5D + 3D I/O → Board/Blade level superconducting 3D stacking → multi-level packaging CMOS and Optical

Superconducting Blade



Superconducting interposer (4K)

\+ Compute & Network stacks

Cryo-optical Transceivers

Cryo-CMOS interposer (77K)

\+ Cryo-DRAM

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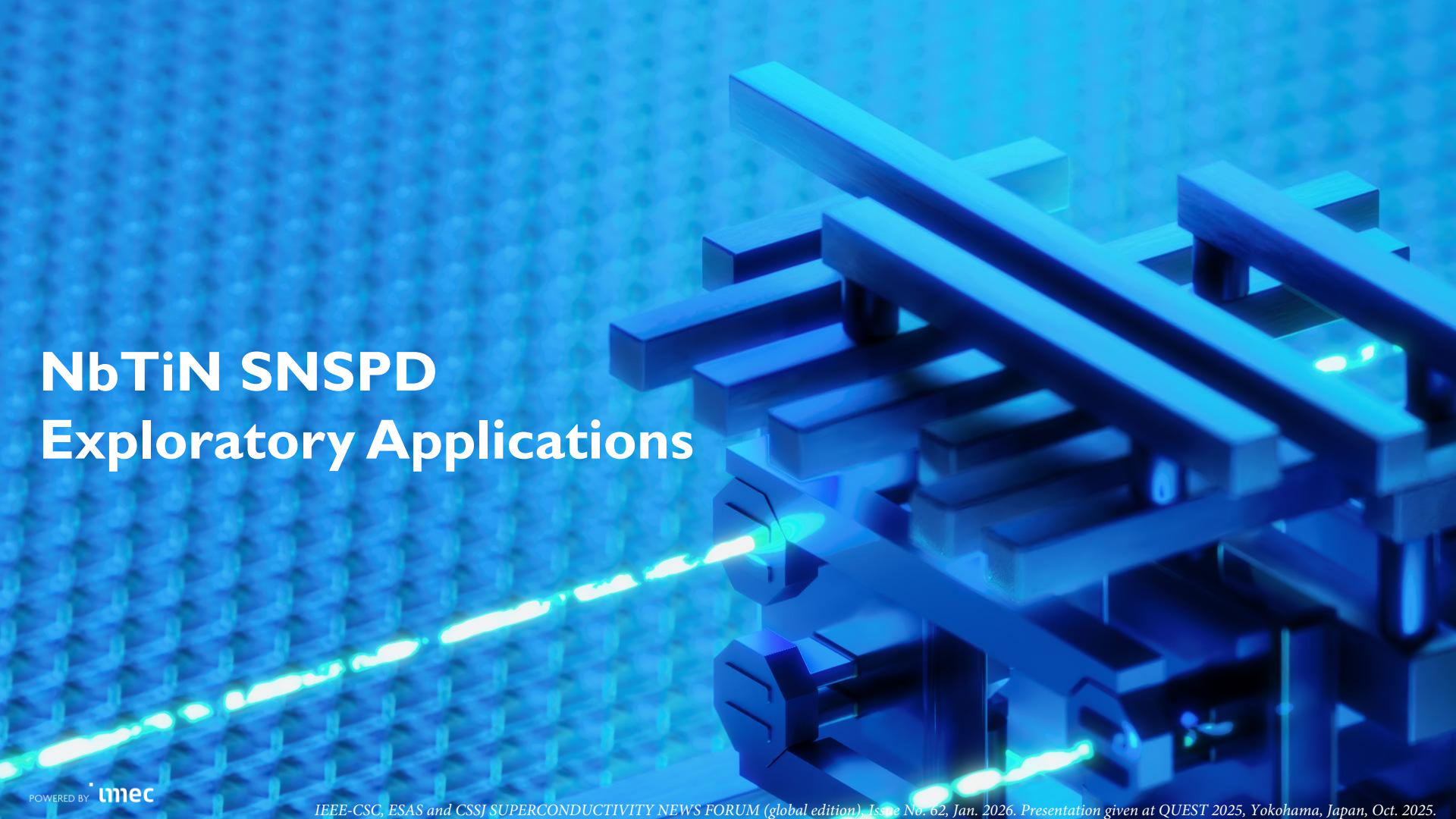
NbTiN SNSPD
Exploratory Applications



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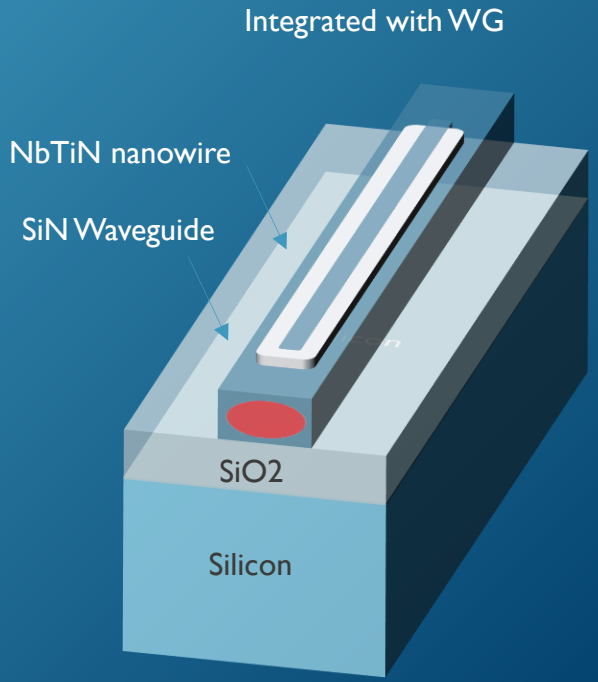
NbTiN for SNSPD



High Critical Temperature

NbTiN has a critical temperature (T_c ≈15 K,) enabling operation at elevated temperatures and reducing cryogenic cooling needs.

Low Kinetic Inductance

Lower kinetic inductance in NbTiN (compared to NbN, WSi, etc) allows faster device reset times and higher photon count rates, critical for rapid photon detection.

High Film Quality

NbTiN films exhibit smooth, uniform deposition improving device yield and reproducibility, ideal for scalable SNSPD manufacturing.

High Detection Efficiency and Integration

NbTiN detectors achieve high efficiency in telecom/visible wavelengths and integrate well with CMOS and silicon photonic platforms.

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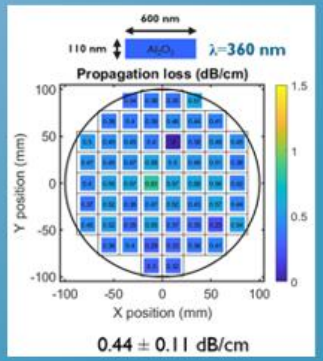
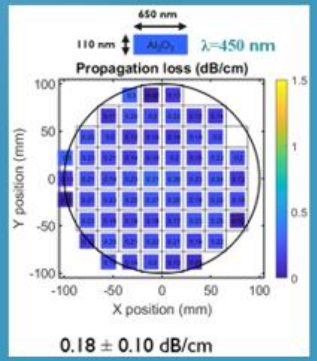
Low Loss Waveguide at IMEC

AlOx waveguide

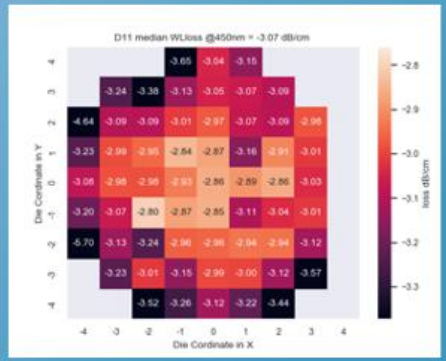
- Tool installed
- Process under development
- Wavelengths / Propagation loss:
  - 360nm / 0.44 dB/cm
  - 450nm / 0.18 dB/cm

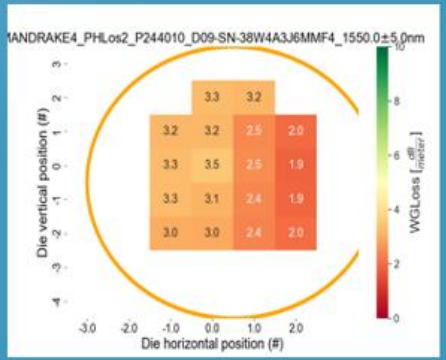




SiN waveguide

- 15 years of experience
- Material optimization for propagation loss
- Wavelengths / Propagation loss:
  - 450nm: ~3dB/cm
  - 1550nm: ~3dB/m





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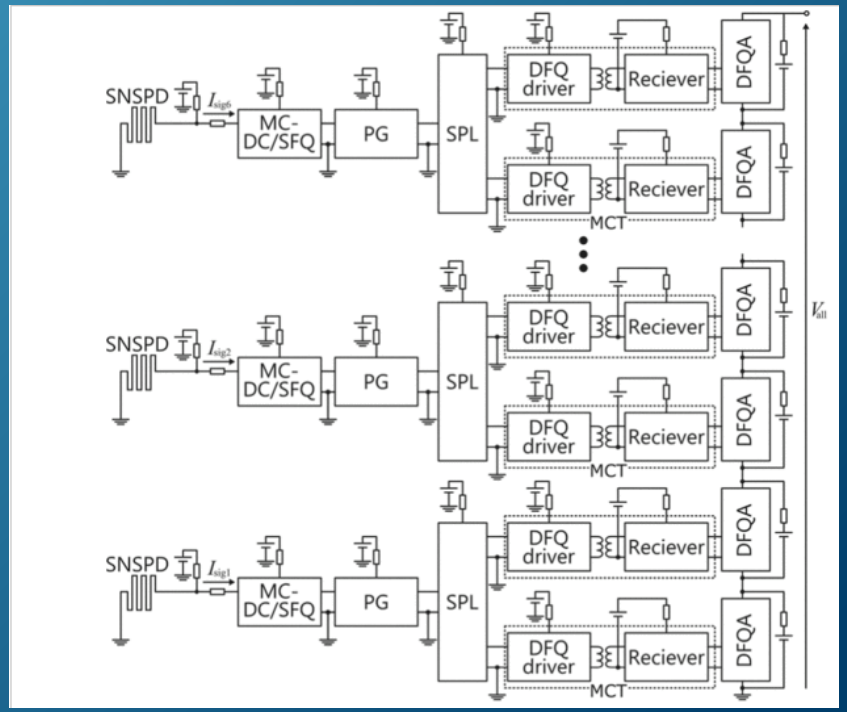
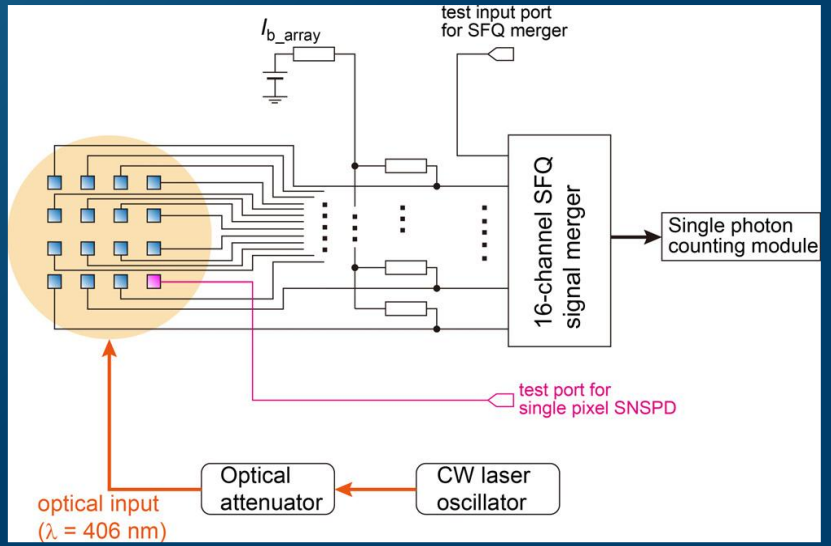
Integration with SFQ



Myoren H, Denda S, Ota K, et al. IEEE Transactions on Applied Superconductivity, 2018, 28(4): 1-4.



Shigeyuki Miyajima, et al. Appl. Phys. Lett. 122, 182602 (2023) 122

Conclusions and Outlook

- NbTiN based superconducting platform offers promising pathway to complement current CMOS technology
- Scalable fabrication of 3ML wires and vias, αSi JJs and HZO MiMCaps have been demonstrated
- These building blocks with processing temperature budget of 420 °C open a path for NbTiN technology for several new applications
- SNSPD integrated with low loss waveguides and Josephson Junction circuits

Acknowledgements

Imec BE and US teams

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