Recent Progress in Design Automation of Superconductor Circuits

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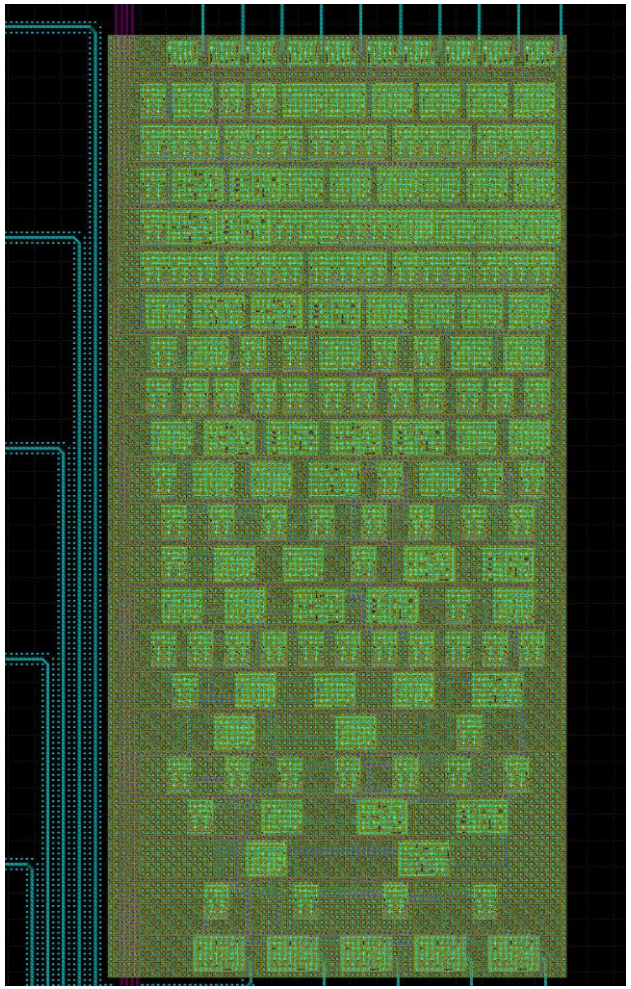
Stellenbosch University and SUN Magnetics

- QuantumEDA group at Stellenbosch University
- SUN Magnetics
  - Spin-off company from Stellenbosch University
  - InductEx, Tetrahenry and JoSIM

Introduction

- From the 1990s to around 2015, superconductor IC design tools a loose collection of in-house modules for low-level design with no application to large-scale system design.
- For many years a number of review and roadmap papers [1-3] highlighted a lack of S-EDA tools and tied that to low IC complexity.
- Unfunded academic tool development was not producing usable tools.
- Circuit complexity at around 10,000 JJs held back by manual design.



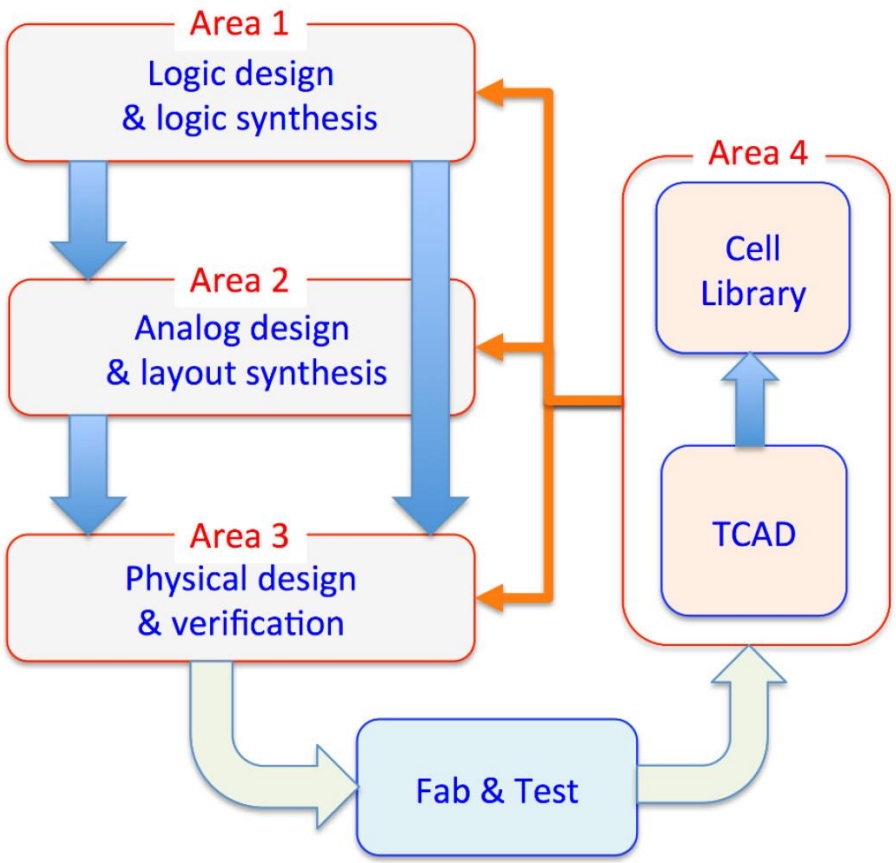
[1] K. Gaj et al., *IEEE Trans. Appl. Supercond.* 9.1, 1999, pp. 18–38
[2] H.J.M. ter Brake et al., *Phys. C* 439.1, 2006, pp. 1–41
[3] Coenrad J. Fourie and Mark H. Volkmann, *IEEE Trans. Appl. Supercond.* 23.3, June 2013.

Introduction

- In 2013, IARPA launched the Cryogenic Computing Complexity (C3) Programme to develop SFQ processors and memory.
- At this time, the state-of-the-art for S-EDA tools was little better than a decade earlier [4].
- C3 finally exposed the limitations inherent to a lack of capable S-EDA tools [5].
- IARPA launched the SuperTools programme in 2016 (after a seedling programme) to develop these tools.
  - Two teams funded:
    - ColdFlux team (USC, UStell, YNU, USMB, NEU, UFlorida) - academic.
    - Synopsys – commercial.
  - Enabled the results shown in these papers [6][7].

[4] Coenrad J. Fourie, *IEEE Trans. on Appl. Supercond.* 28.5, Aug. 2018, Art. no. 1300412
[5] Marc A Manheimer, *IEEE Trans. Appl. Supercond.* 25.3, June 2015, Art. no. 1301704
[6] Coenrad J. Fourie et al., *IEEE Trans. Appl. Supercond.* 29, Aug. 2019, Art. no. 1300407
[7] Coenrad J. Fourie et al., *IEEE Trans. Appl. Supercond.* 33.8, 2023, Art. no. 1304926

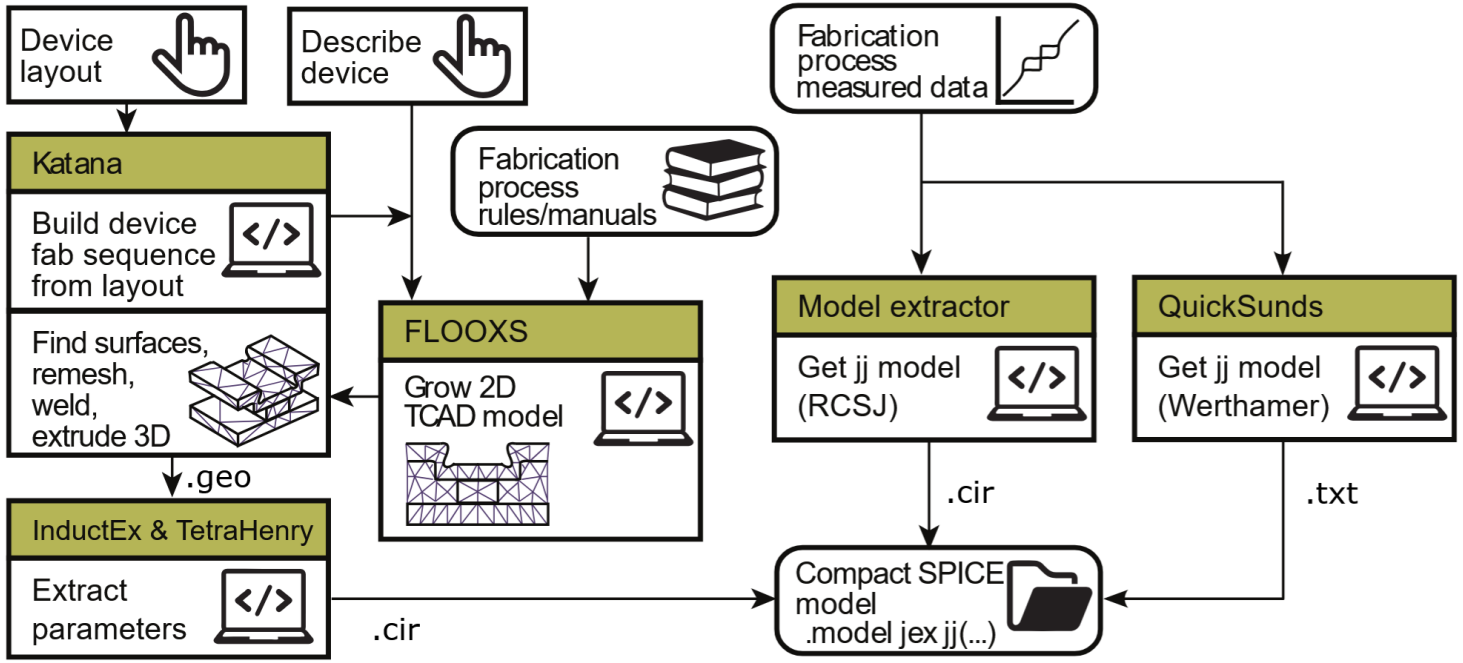
SuperTools Objectives



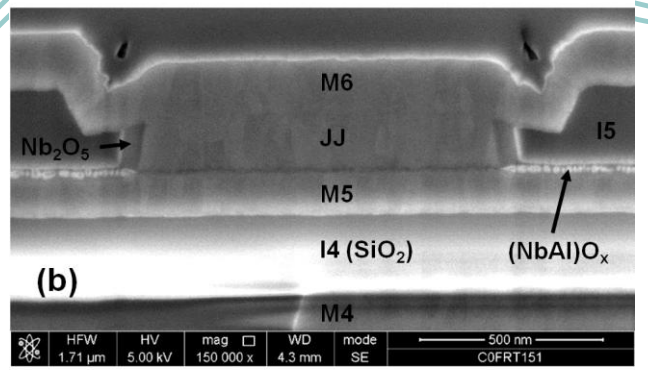
- The SuperTools objectives were spread over four areas, aided by fabrication and test feedback.
  - RTL synthesis, architectures and verification.
  - Analogue design and layout synthesis.
  - Physical design and test.
  - Technology CAD and cell library design.
- Project goals, starting from a baseline of 10,000 JJs or 1,000 gates that could be synthesized, verified and laid out with existing tools, were ambitious:
  - Phase 1: 100,000 JJs; 10,000 gates.
  - Phase 2: 1M JJs, 100k gates.
  - Phase 3: 10M JJs, 1M gates; with 64-bit RISC processor synthesis and simulation possible, and tight margins on clock skew and simulation error (later amended to 1M JJs, 100k gates).

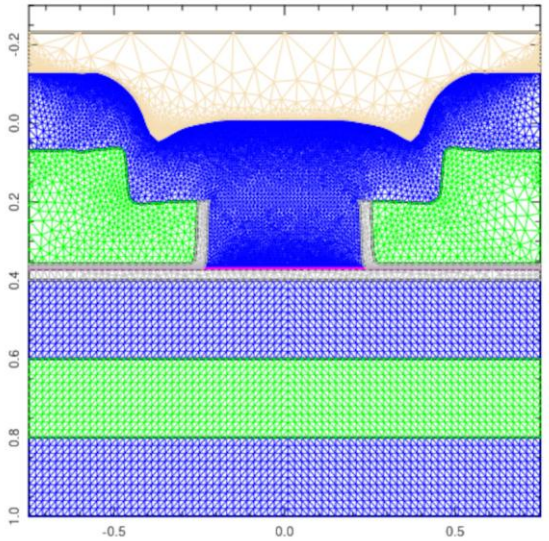
ColdFlux - Technology CAD

- FLOOXS/FLOOSS simulates 8 fabrication processes in 2D.
- Extrusion of 2D TCAD slices to create quasi-3D (2.5D) models of devices and circuit components.



[8]



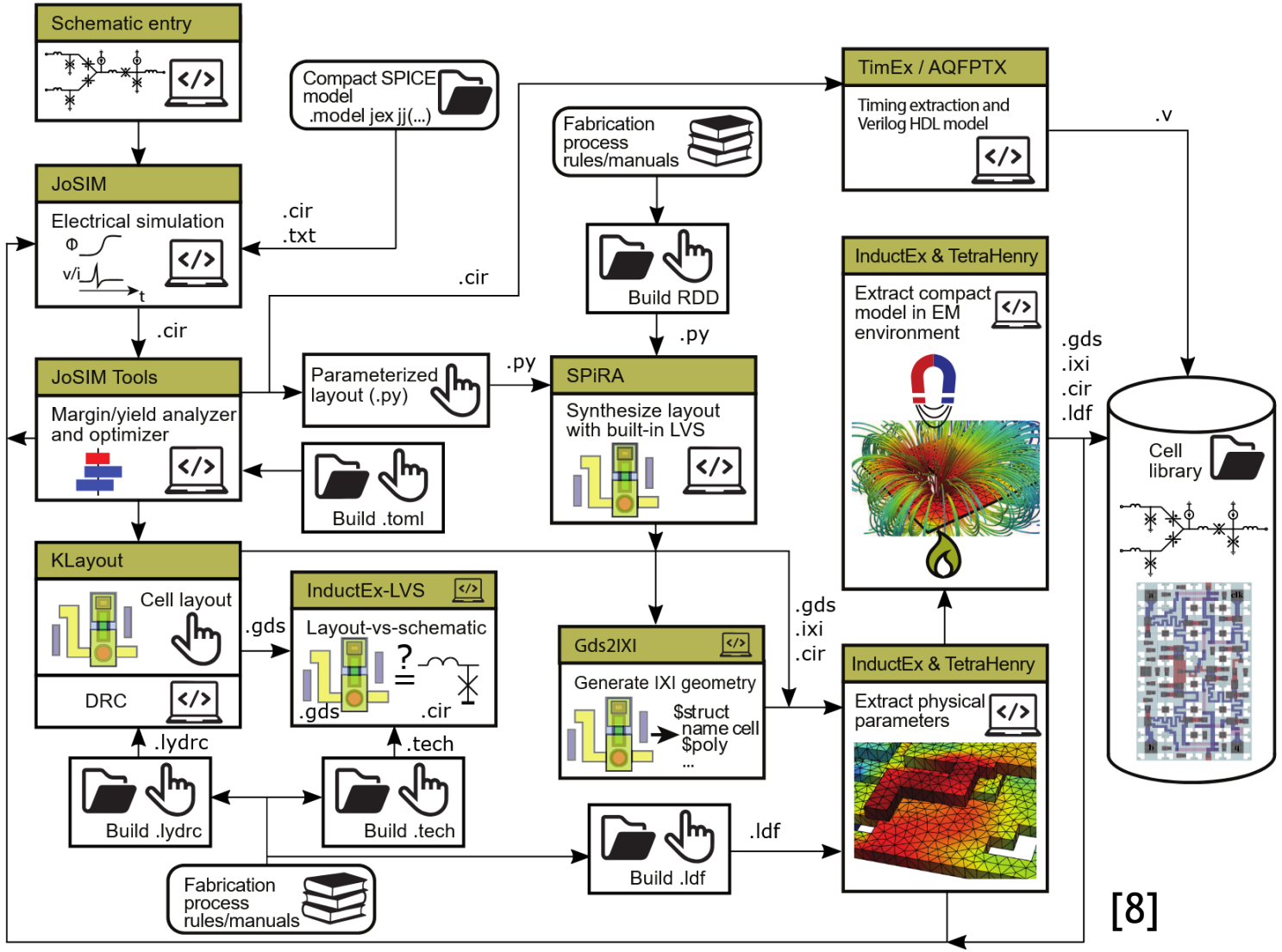


MITLL SFQ5ee process Josephson junction[9] (top) cross-section and (bottom) FLOOSS TCAD result.

[8] Coenrad J Fourie 2020 J. Phys.: Conf. Ser. 1590 012040
[9] Sergey K. Tolpygo et al., IEEE Trans. on Appl. Supercond., 26.3, Apr. 2016, Art. no. 1100110

ColdFlux – Physical (Back-end) Tools

- Tools developed:
  - JoSIM
  - JoSIM Tools
  - InductEx-LVS
  - TimEx/AQFPTX
  - SPiRA
- Tools expanded:
  - InductEx
  - TetraHenry

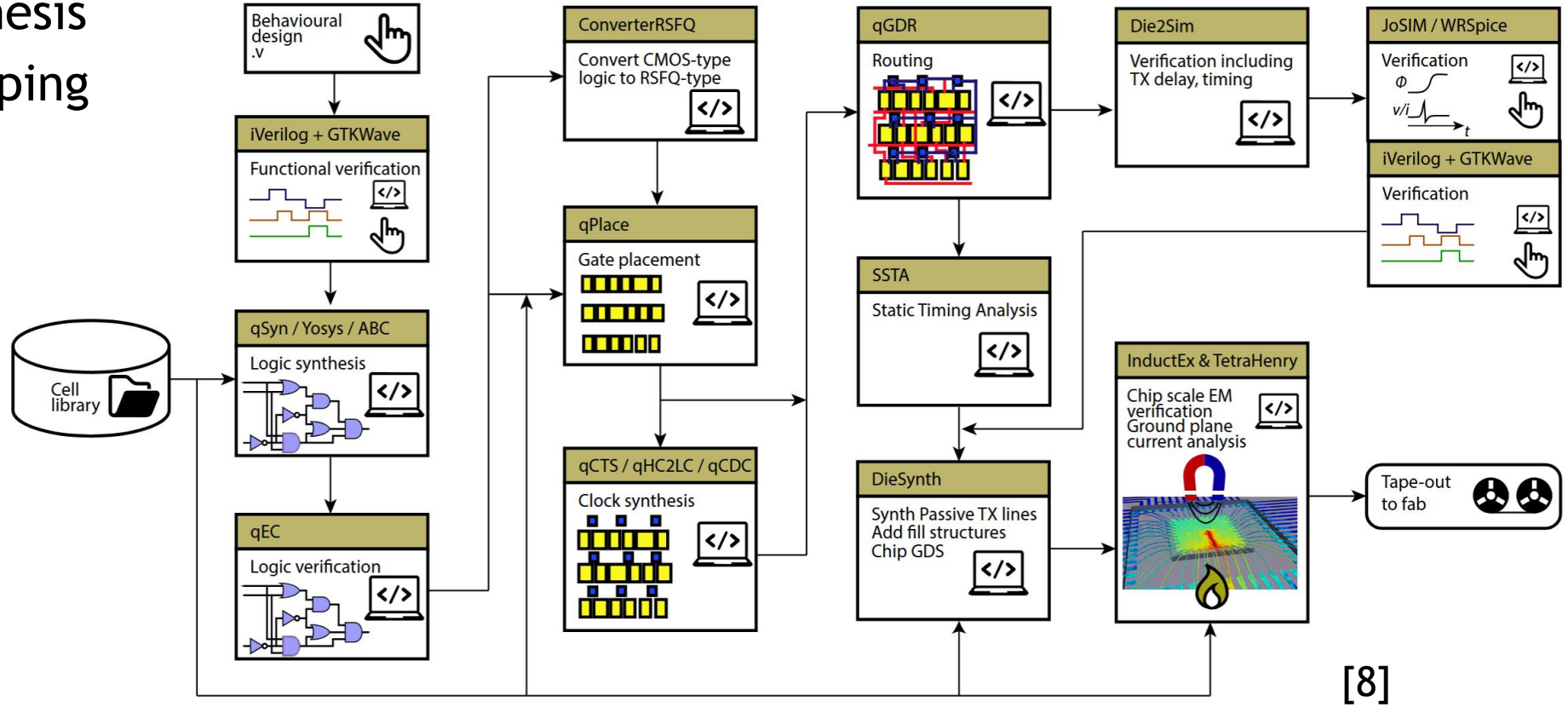


[8]

[8] Coenrad J Fourie 2020 J. Phys.: Conf. Ser. 1590 012040

ColdFlux – Digital Systems (Front-end Tools)

- qPALACE suite that includes
  - RSFQ logic synthesis
  - Technology mapping
  - Clock synthesis
  - Placement, and
  - Routing tools.

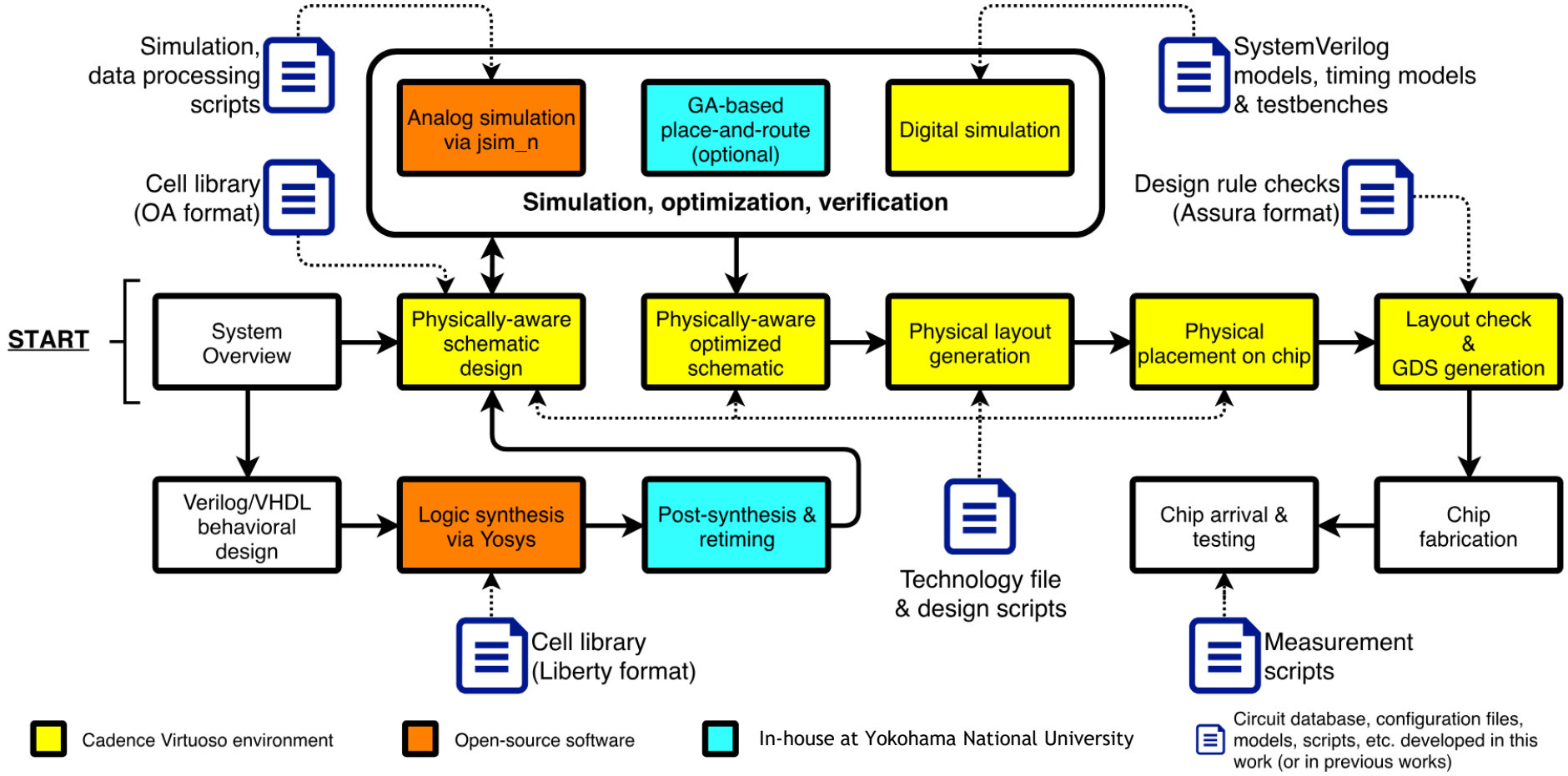


[8]

[8] Coenrad J Fourie 2020 J. Phys.: Conf. Ser. 1590 012040

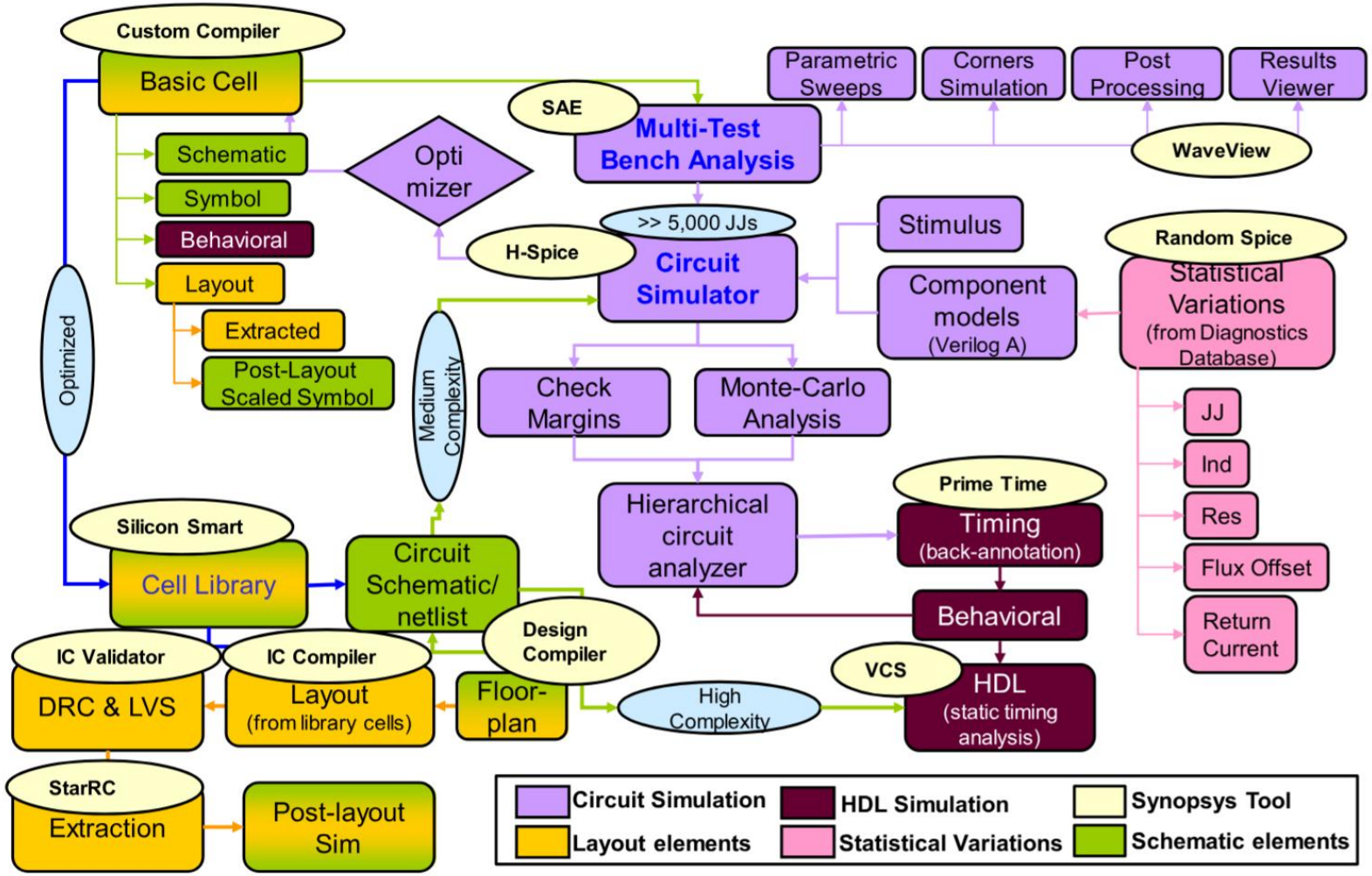
AQFP example workflow

- Semi-custom design flow and environment using established cell library.



[10] Christopher L Ayala *et al., Supercond. Sci. Technol.*, **33,** 054006, 2020

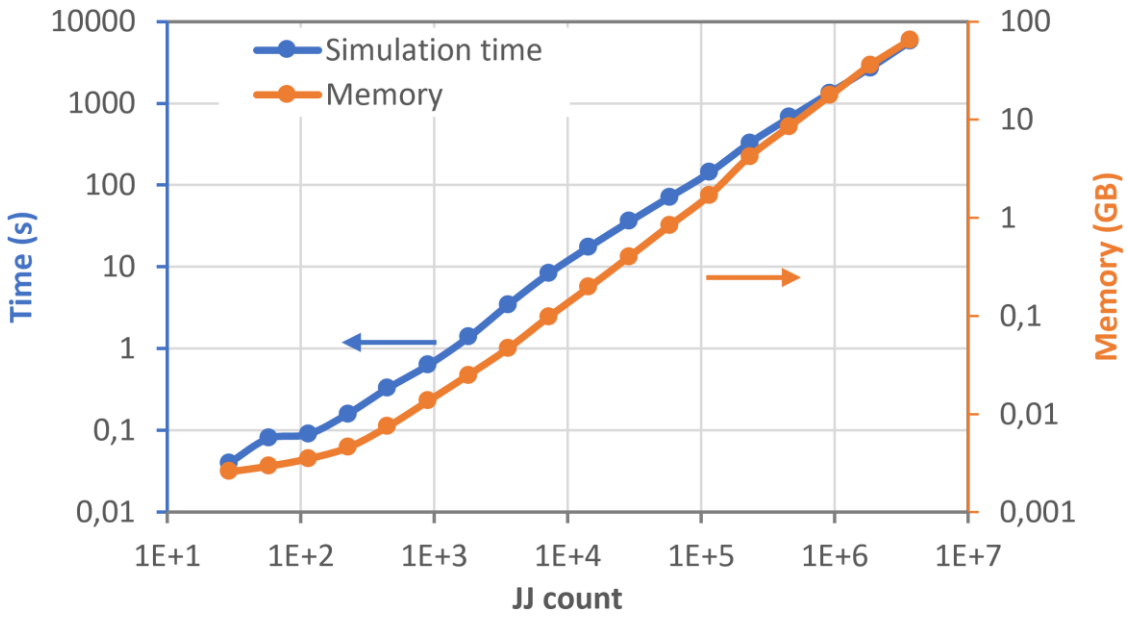
Example workflow with Synopsys Tools



[11] A. Inamdar *et al*,. *IEEE Trans. on Appl. Supercond.*, vol. 31.5, Aug. 2021, Art no. 1301907

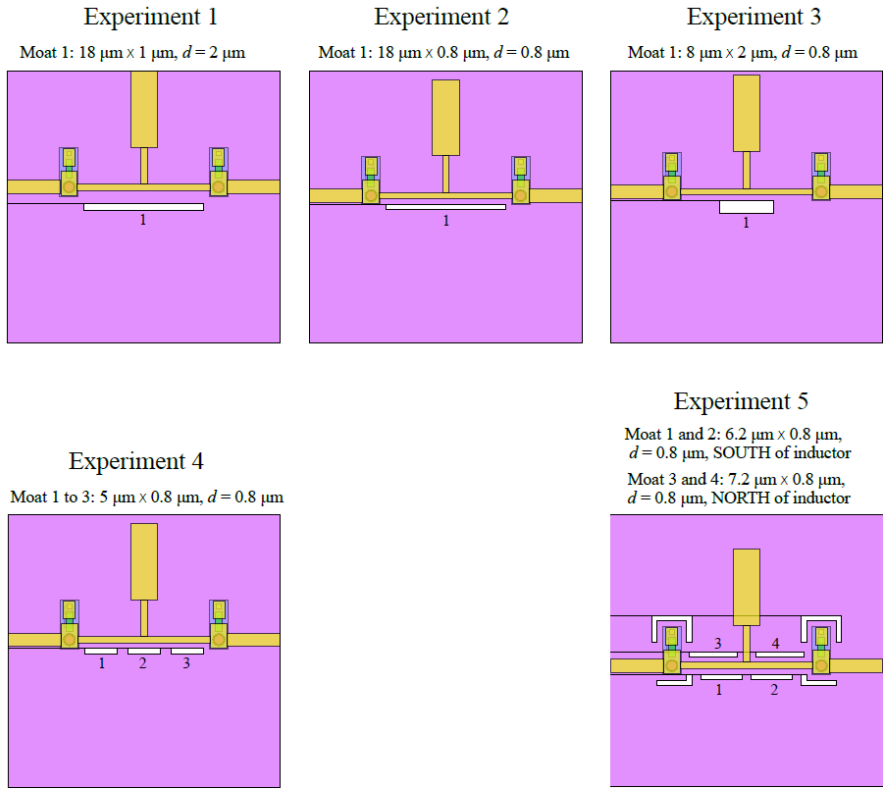
SuperTools Results - JoSIM

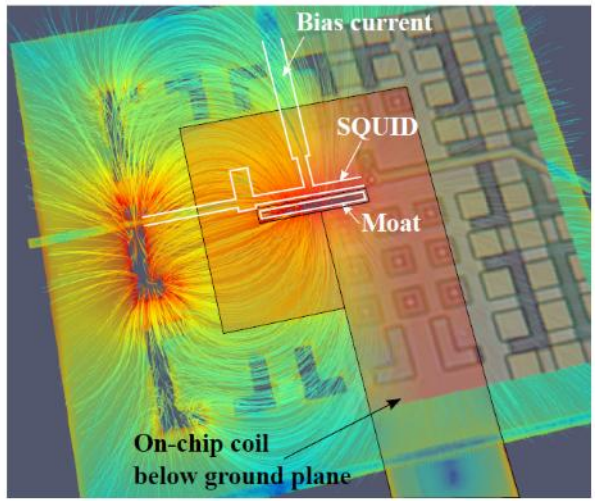
- Design complexity demonstration:
  - Large clock distribution network:
    - Subcircuit count: 41
    - Component count: 23,592,967
    - JJ count: **3,670,017**
    - Inductor count: 14,680,070
    - Resistor count: 5,242,880
    - Current source count: 2,097,154
    - Time: 5697.73 s
    - Memory: 64,821,724 kB
  - Clock frequency demonstration:
    - Input pulse train provided to a 8-bit shift register at **100 GHz** demonstrating successful throughput in transient simulation.

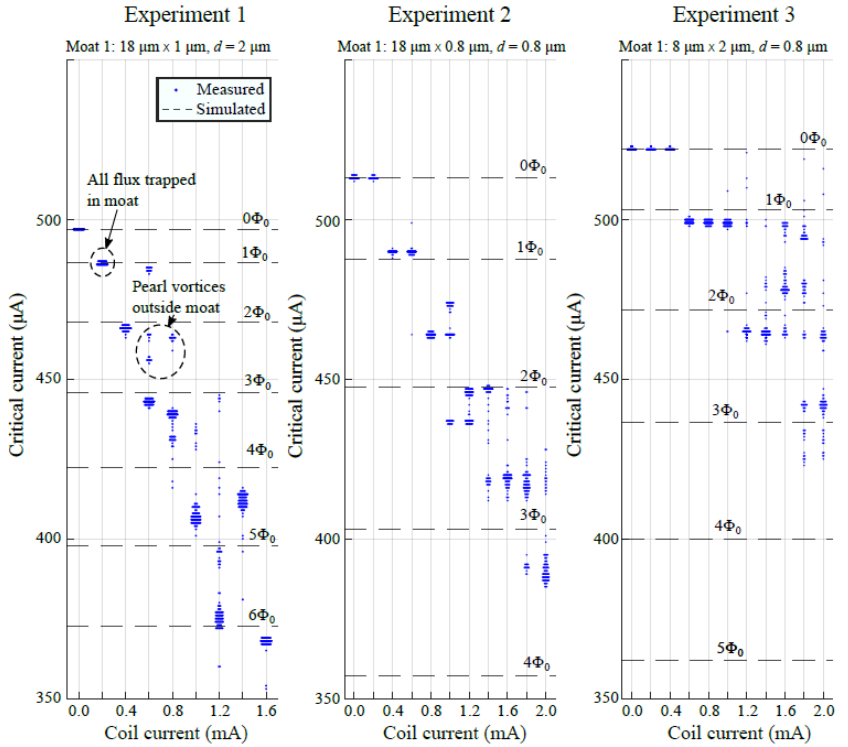


SuperTools Results: Flux Trapping Analysis

- Experimentally confirmed. Predicted (simulation) and measured discrete jumps in I_C for a SQUID agree [12][13].

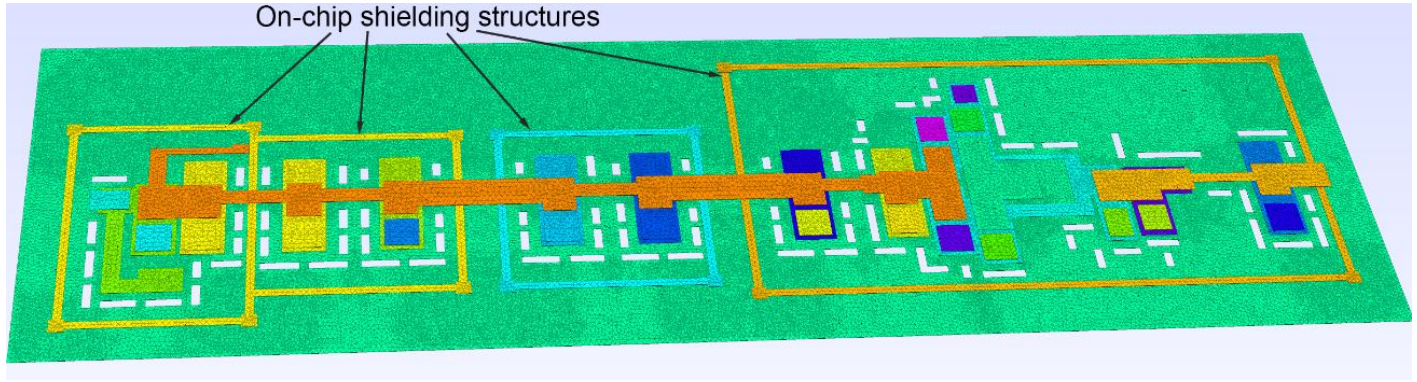


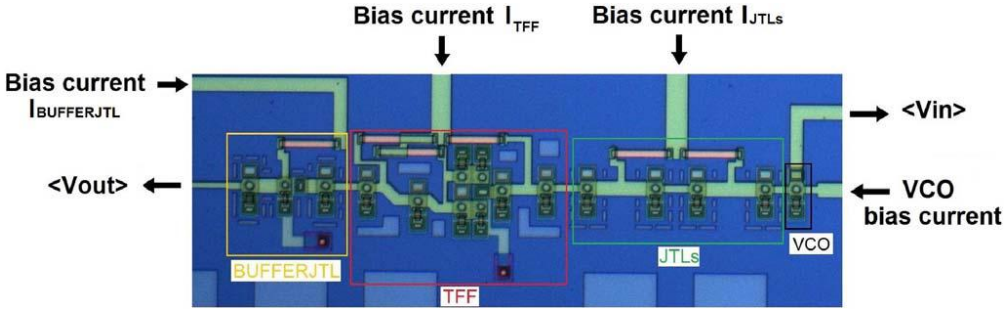


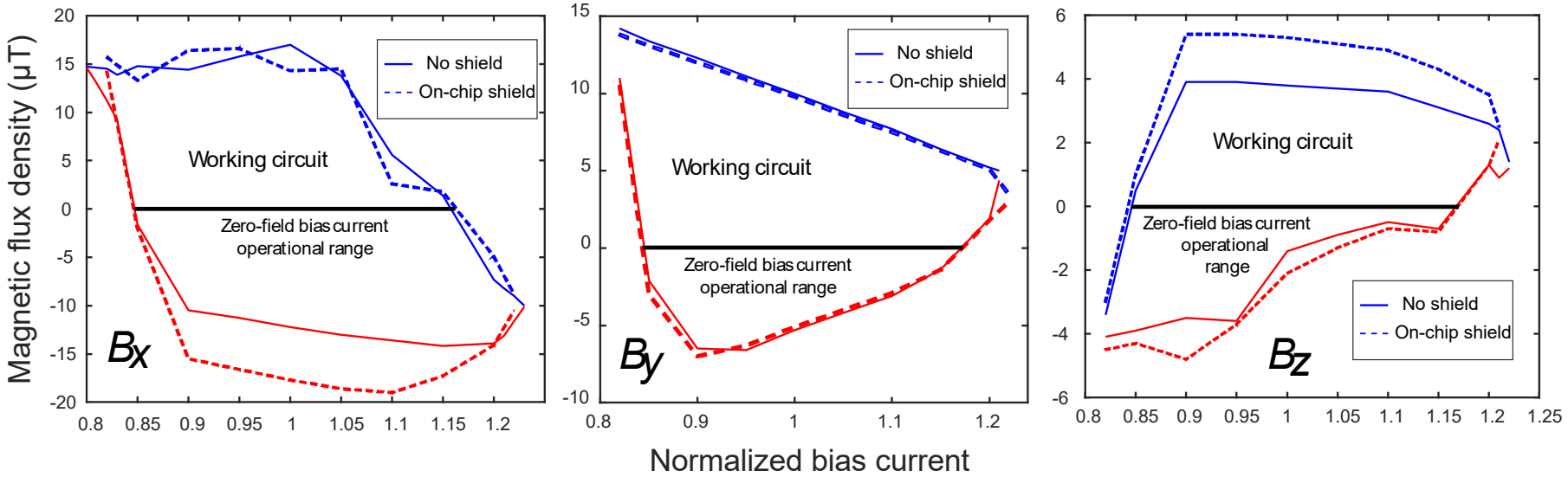


[12] K. Jackman, C. J. Fourie, *Supercond. Sci. Technol.*, vol. 33, 105001, 2020
[13] C. J. Fourie and K. Jackman, *IEEE Trans. Appl. Supercond*, 31, no. 5, 2021

SuperTools Results: Compact Models in EM Environment



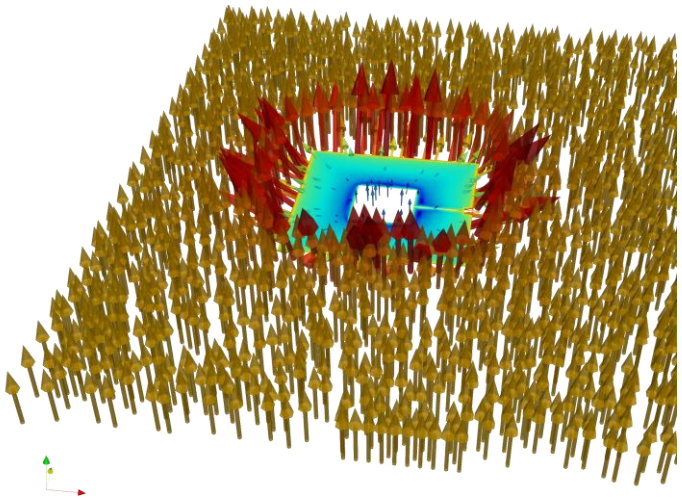


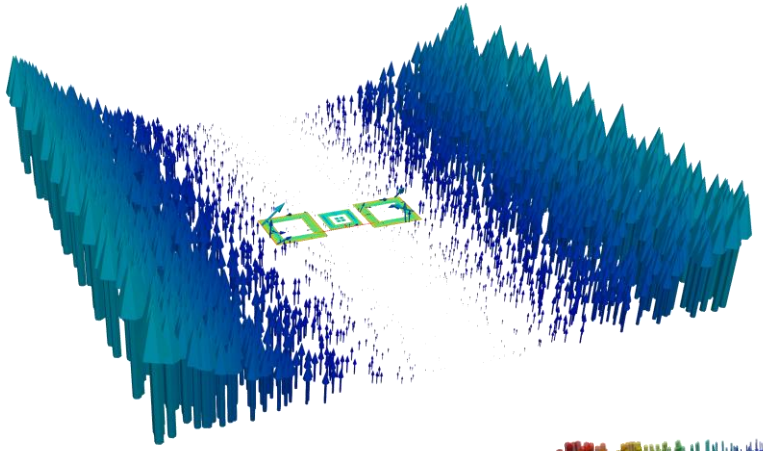


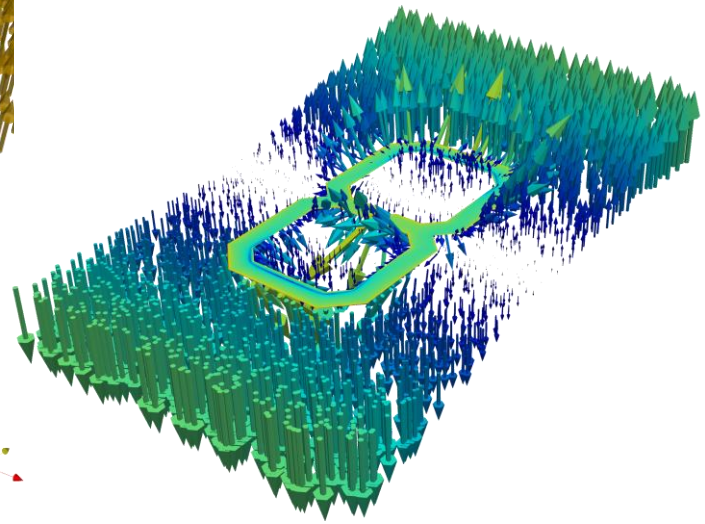
[14] C. J. Fourie, K. Jackman, *IEEE Trans. Appl. Supercond.*, vol. 29, 1301004, 2019

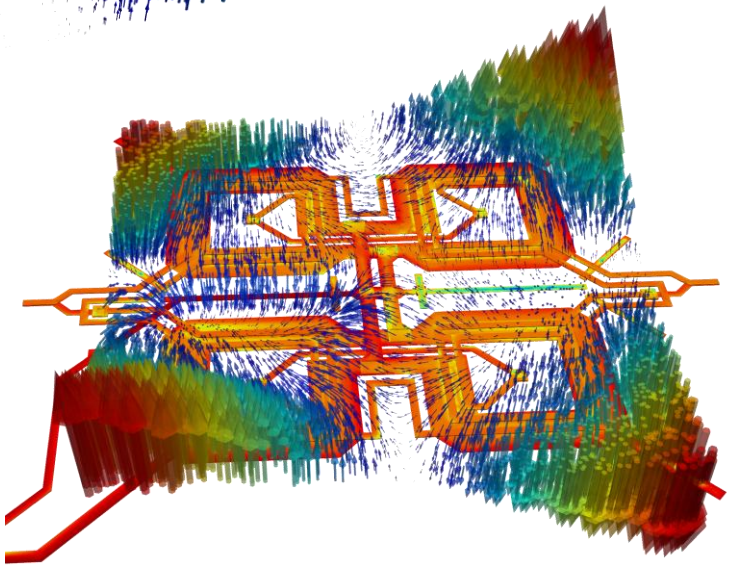
SuperTools Results: SQUIDs and Gradiometers in Field

- Uniform fields, or functions to model gradient response.



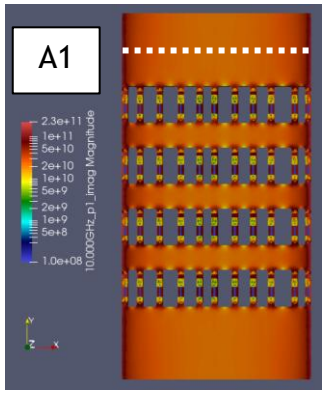


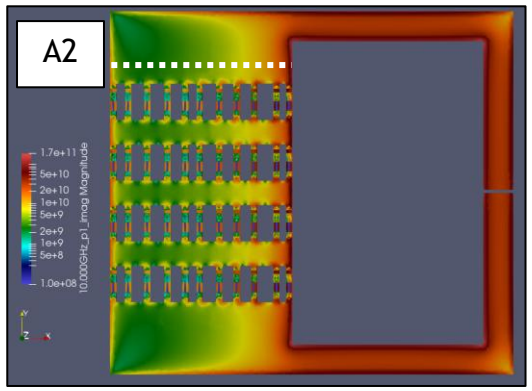


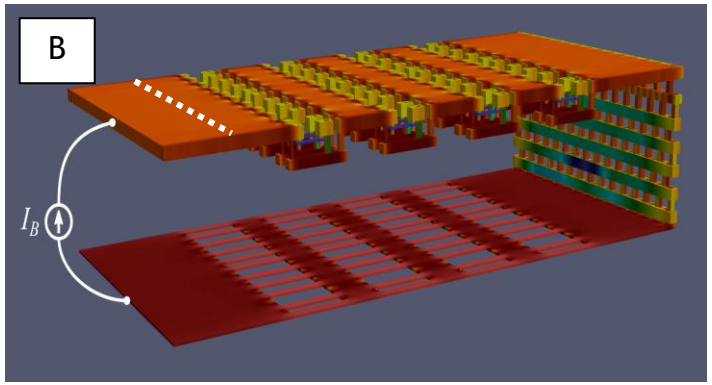


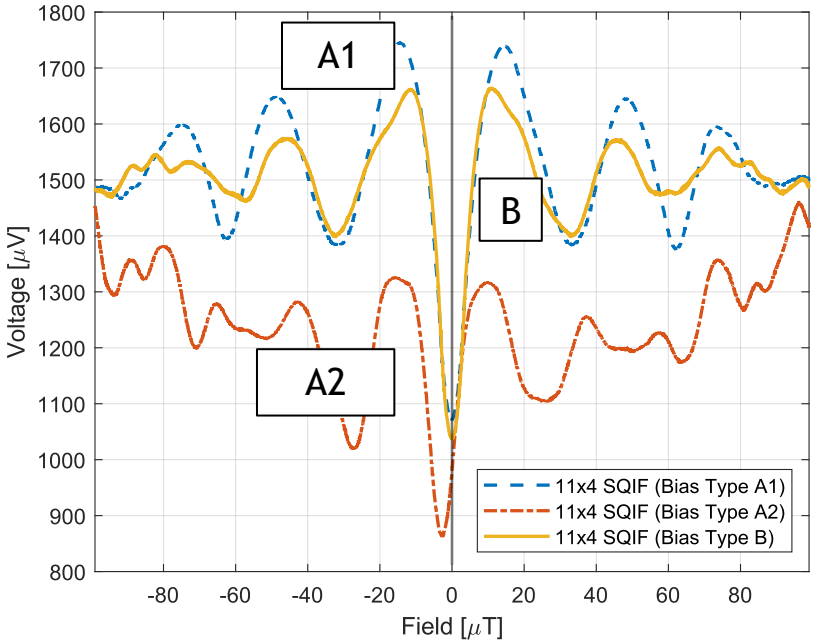
SuperTools Results: SQIF Analysis

- Developed design automation tools for extracting high-fidelity models for superconductor integrated circuits.
- **Tools can be used for compact models of 2D SQIF arrays.**
  - Compact models include all mutual inductances.
  - Support external magnetic field excitations.
  - Compatible with existing circuit simulators: JoSIM, WRspice, etc.
  - Streamlines SQIF design and evaluation process.





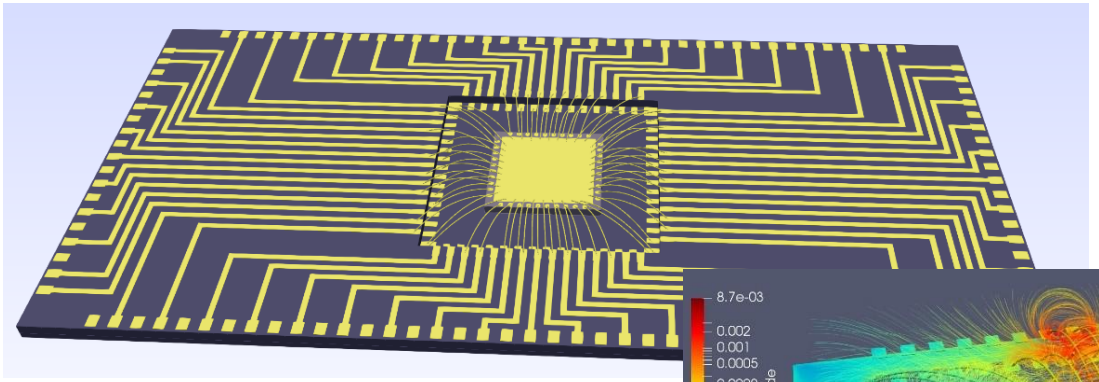


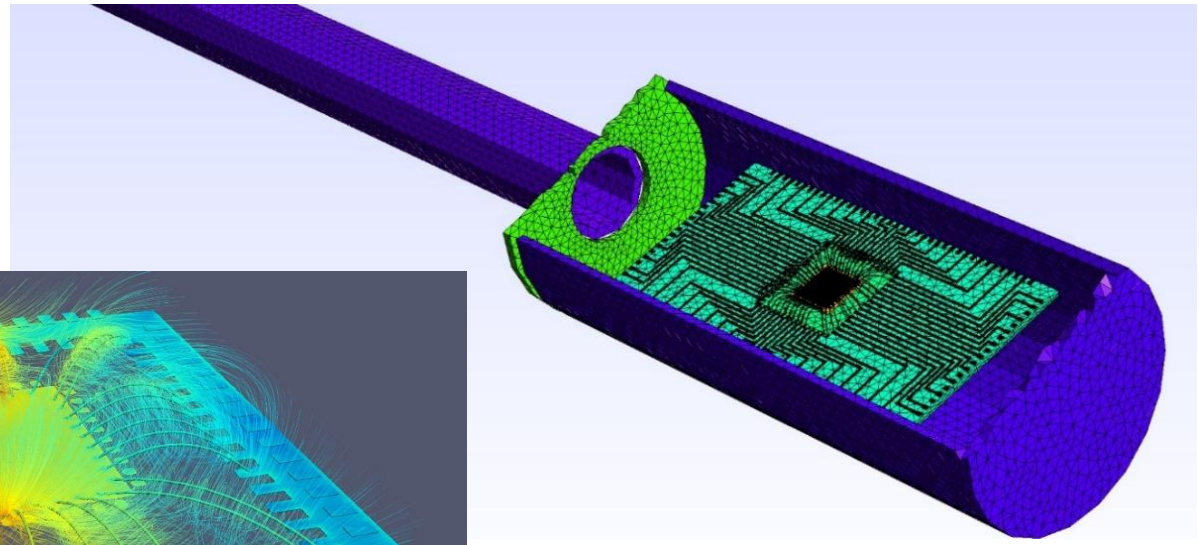


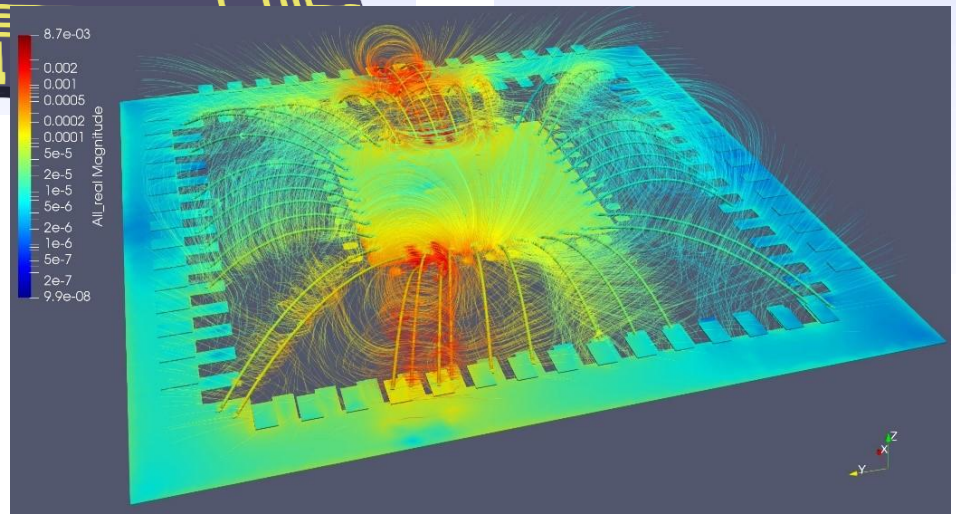
VB-response of 4x11 SQIF array with different biasing techniques.

SuperTools Results: Packaging and Shielding analysis

- Full chip-in-package with shields, wire/bump bonds
- Use IXI/mesh exports to include enclosure effects

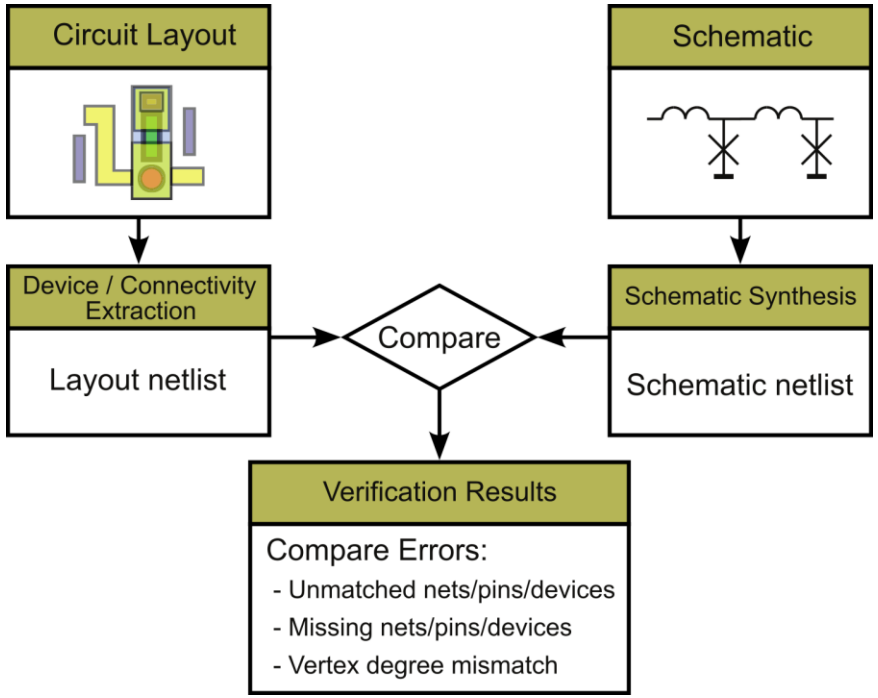


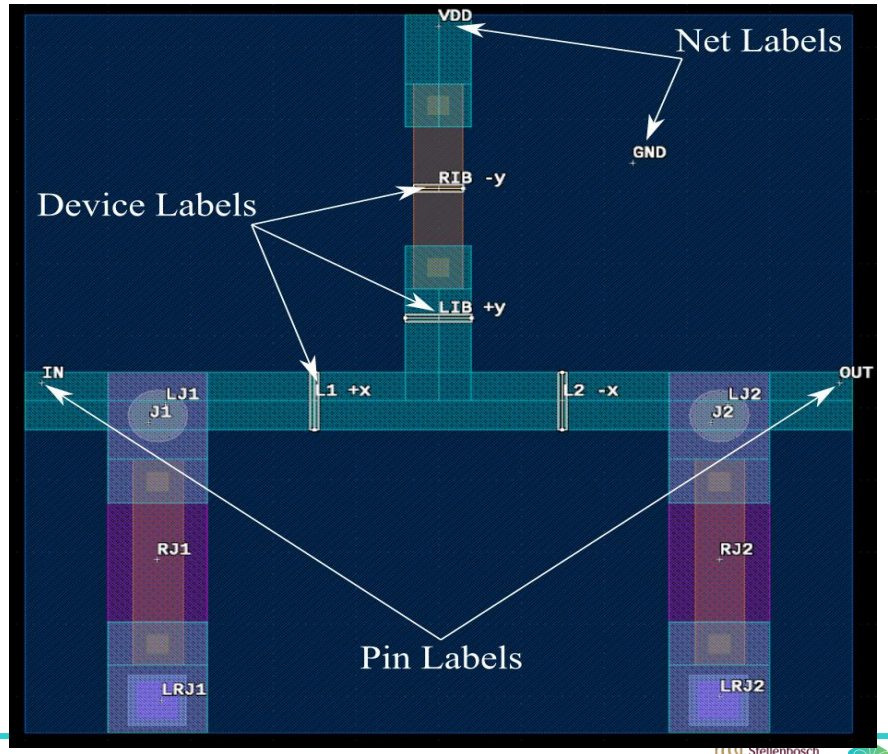




SuperTools Results: InductEx-LVS

- **LVS for superconducting layouts:**
  - Compares layout topology ↔ schematic netlist
  - Device recognition: JJs, resistors, inductors, vias, interconnect
  - Goal: catch connectivity mistakes early (especially multi-layer stacks)





Evolution of InductEx

Single inductors (10 - 30 mins)

Inductance network no M; sub-gate (1 - 30 hours)

L and M network gates (1 - 2 hours)

+ J, B/H-field ~10 gates (1 - 2 hours)

+TTH ~10 gates (20 s - 2 min)

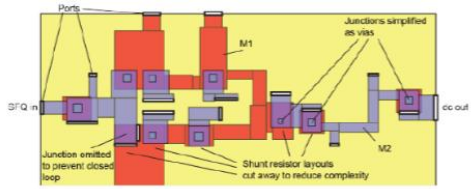
+Fluxons, external H

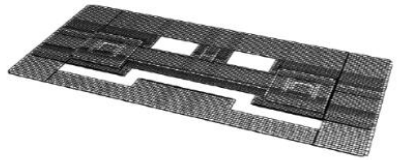
+Compact model extr.

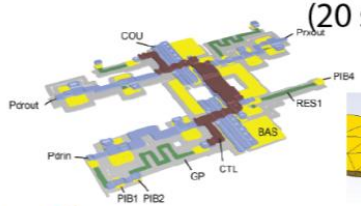
+FFH ~10 gates (20 s - 2 min)

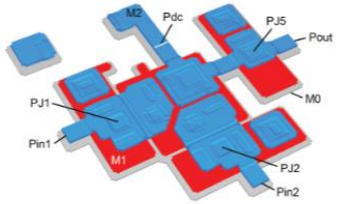
+E-fields, C, chip-scale, permability

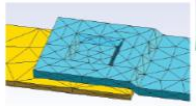
+Package modelling (5 - 10 min)

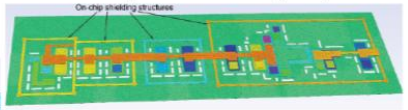


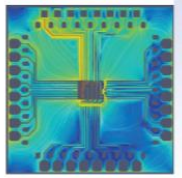


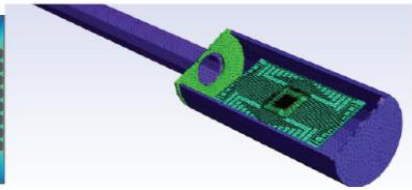












2004 2007 2010 2013 2016 2019

10K segs 20-30K segs 50-100K segs 200K segs 1M segs >10M segs

Speed 1X → 2,000X

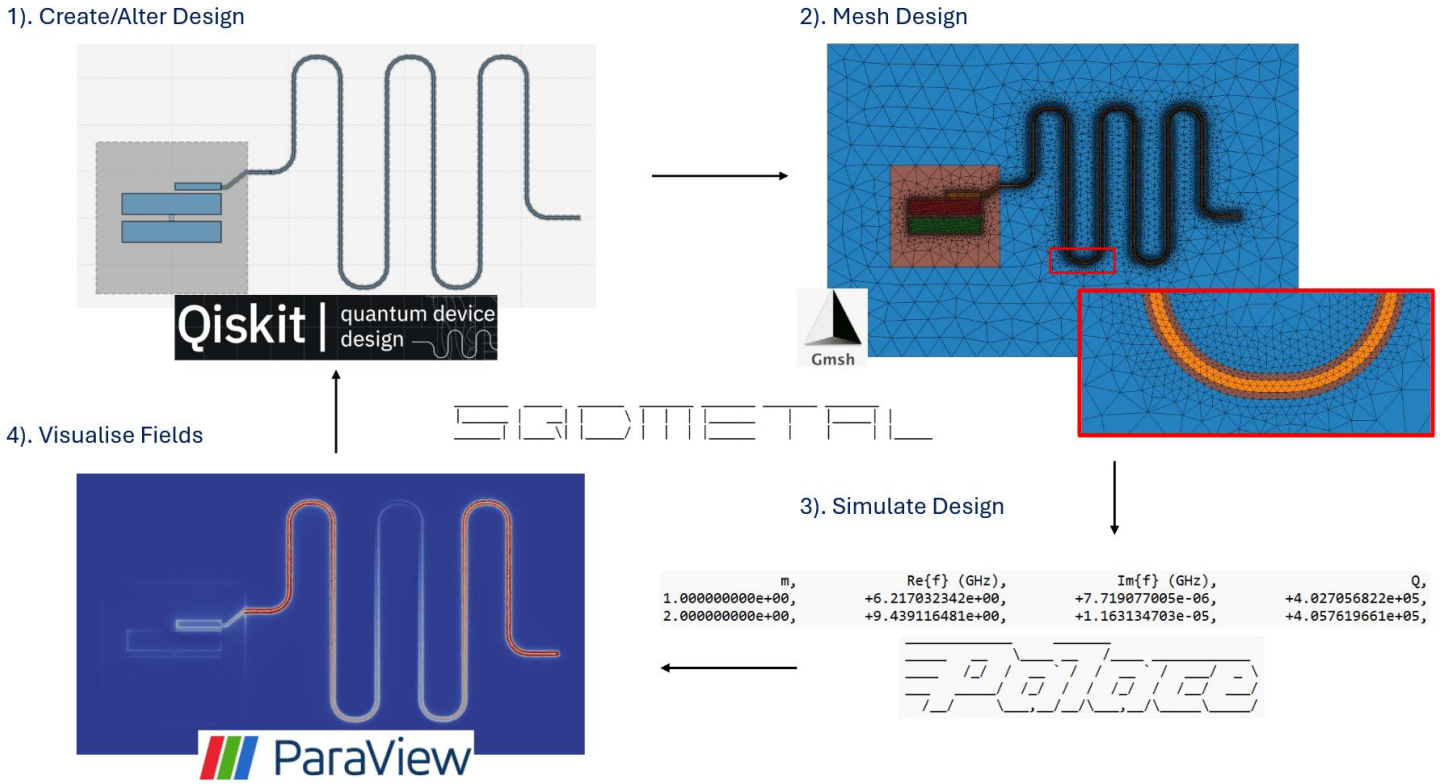
Segments 10K → 10,000K

[20] Coenrad J Fourie, *J. Phys.: Conf. Ser.*, **1590** 012040, 2020

S-EDA Tools in Quantum Computing

- Recently, a strong shift in SCE IC development from high performance or energy-efficient computing towards quantum computing applications.
- Some tools exist to design and simulate qubit systems.
  - Qiskit from IBM to design and simulate at the qubit level.
    - Abstracts away the hardware complexities.
    - Provides a high-level interface to simulate qubit systems and quantum algorithms.
- However, at the electronics level, no clear tool kit yet. For superconducting interfaces to qubits; especially to superconducting qubits (with Josephson junctions):
  - Sonnet used with SC material parameters to analyse microwave structures.
  - HFSS with Qiskit Metal can handle superconducting qubit structures (e.g. transmon qubits).
- Some of these tools approximate superconductors as PEC, neglecting kinetic inductance. Few can handle trapped flux.

Example Usage of Open-source Tools



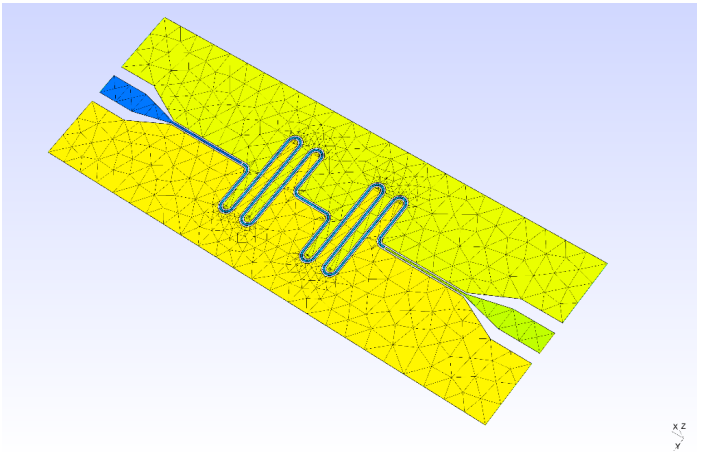
SQDMetal [15] - open-source Python API used for the design and simulation of superconducting quantum devices

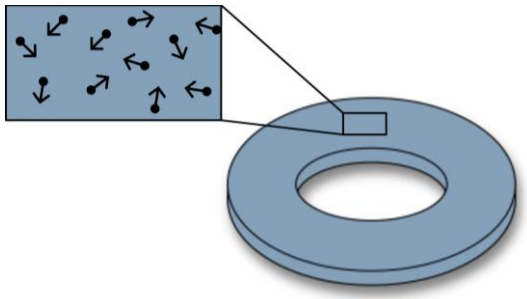
- Qiskit Metal [16] — an open-source framework for the design of superconducting quantum chips and devices.
- Gmsh [17] — an open-source finite element mesh generator for creating 3D meshes and models.
- Palace (Parallel Large-scale Computational Electromagnetics) [18] — an open-source electromagnetic solver.
- ParaView [19] — an open-source visualization and post-processing tool.

[15] David Sommers et al., Nov 2025, arXiv:2511.01220
[16] "Qiskit metal," (2025), https://github.com/qiskit-community/qiskit-metal.
[17] C. Geuzaine and J.-F. Remacle, International Journal for Numerical Methods in Engineering.
[18] "Palace," (2025), https://awslabs.github.io/palace/stable/.
[19] "Paraview," (2025), https://www.paraview.org/.

S-EDA Tools in Quantum Computing

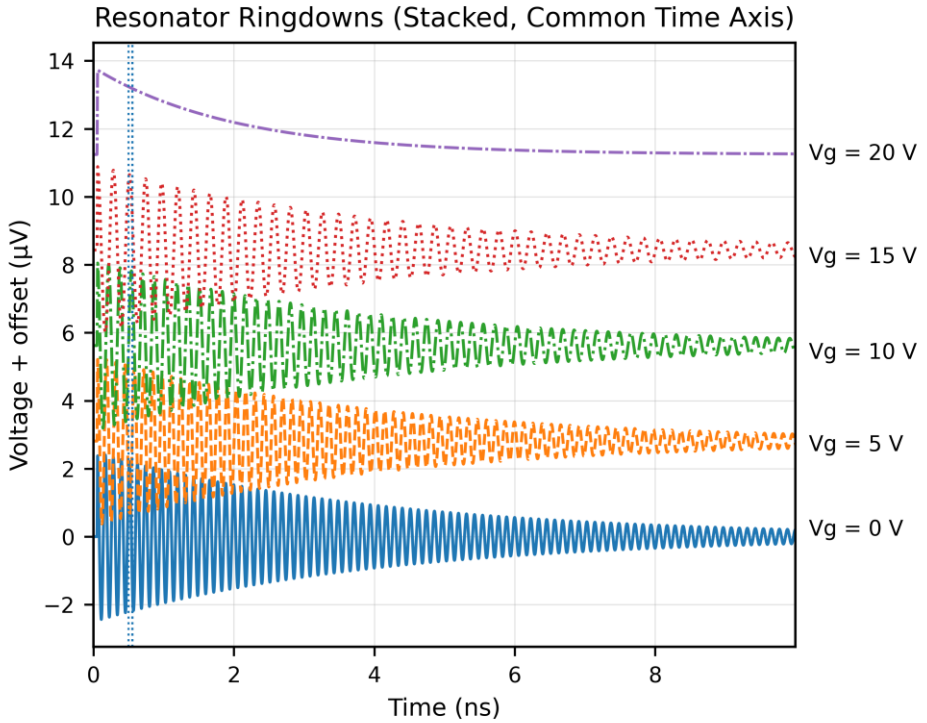
- Requirements:
  - Support for aluminium cross-type junctions in single and multilayer processes; 3D modelling.
  - High calculation precision to design, analyse and improve:
    - High-Q resonators frequency.
    - Coupling to qubits.
    - Cross-talk.
  - Numerical methods to model and calculate noise in representative IC structures (such as flux noise in inductors; spin-reversal).

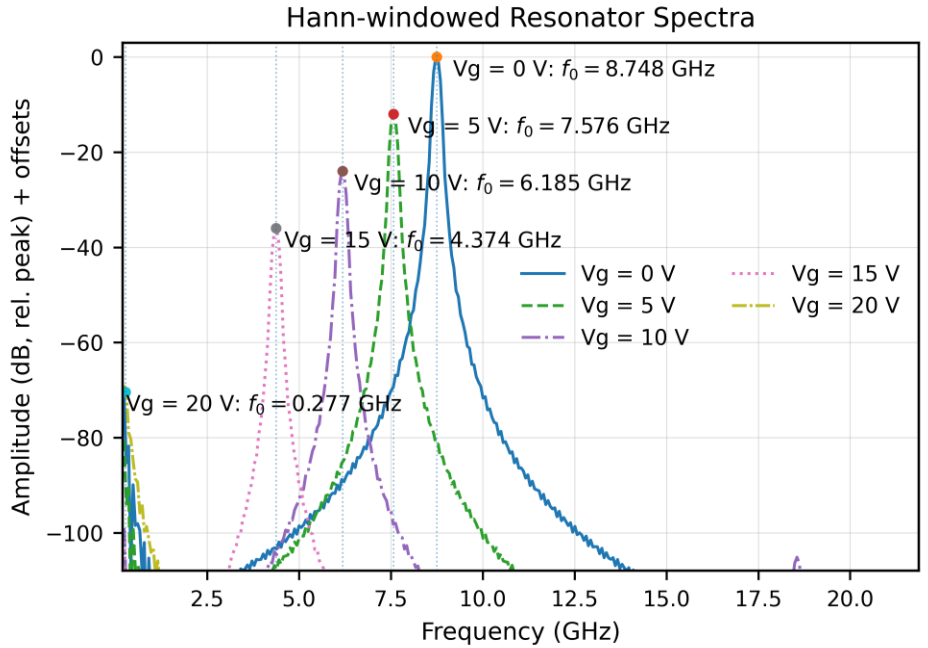




Post-SuperTools: JoSIM

- Development of JoSIM-Pro
  - Performance-tuned commercial version of JoSIM.
- Electrostatic Gate-Tunable Josephson Junctions in JoSIM (Gatemons) [20]

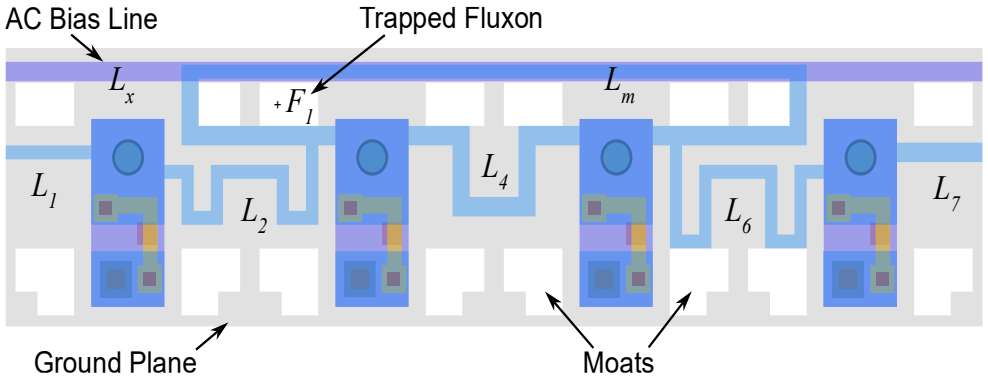




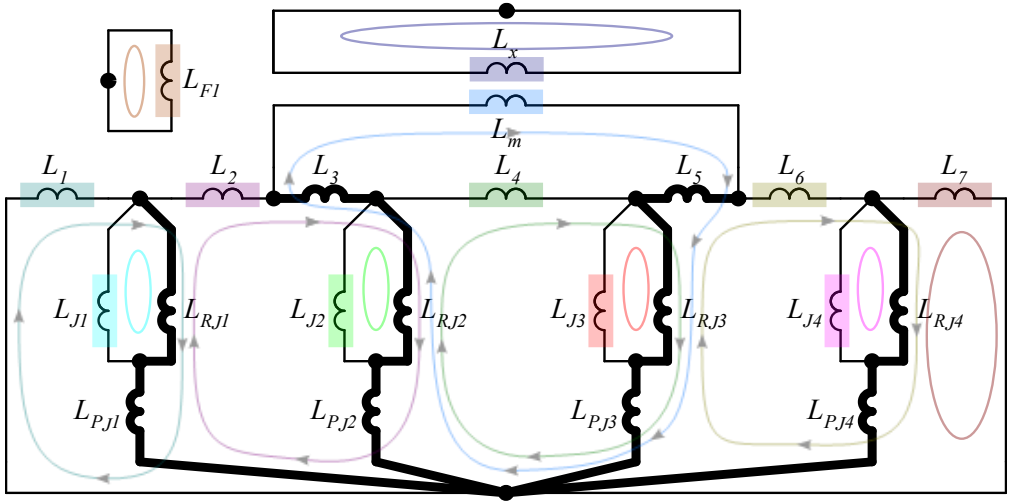
[20] J. A. Delport and O. Chen, *IEEE Trans. Appl. Supercond.*, doi: 10.1109/TASC.2025.3617516.

Post-SuperTools: CheckNet

- Compact model theory used to develop CheckNet
- Automatic Identification of Magnetic Couplings
  - Build the full inductance matrix
  - Flag missing/invalid couplings; highlight strong/weak links
  - Use graph views to spot unintended paths



Layout of AC-biased RSFQ shift register



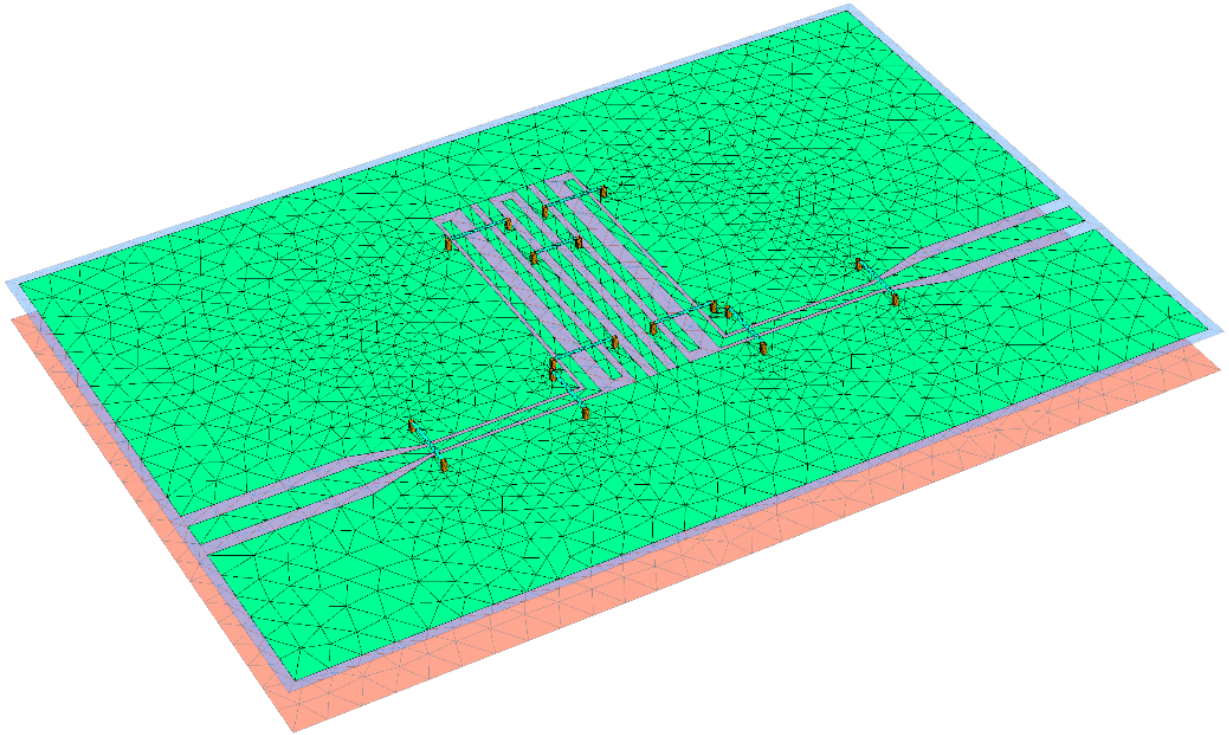
Graph representation of circuit diagram

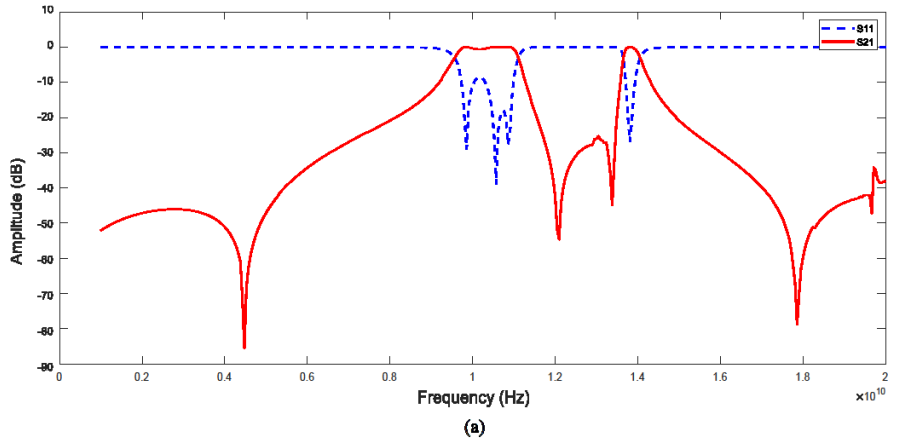
	L_1	L_2	L_4	L_6	L_7	L_{F1}	L_{J1}	L_{J2}	L_{J3}	L_{J4}	L_M	L_x
L_1	L_1	•	$M_{1,4}$	$M_{1,6}$	$M_{1,7}$	$M_{1,F1}$	$M_{1,J1}$	$M_{1,J2}$	$M_{1,J3}$	$M_{1,J4}$	$M_{1,M}$	$M_{1,x}$
L_2		L_2	•	$M_{2,6}$	$M_{2,7}$	$M_{2,F1}$	•	$M_{2,J2}$	$M_{2,J3}$	$M_{2,J4}$	•	$M_{2,x}$
L_4			L_4	$M_{4,6}$	$M_{4,7}$	$M_{4,F1}$	$M_{4,J1}$	•	$M_{4,J3}$	$M_{4,J4}$	•	$M_{4,x}$
L_6				L_6	•	$M_{6,F1}$	$M_{6,J1}$	$M_{6,J2}$	$M_{6,J3}$	$M_{6,J4}$	•	$M_{6,x}$
L_7					L_7	$M_{7,F1}$	$M_{7,J1}$	$M_{7,J2}$	$M_{7,J3}$	•	$M_{7,M}$	$M_{7,x}$
L_{F1}						L_{F1}	$M_{F1,J1}$	$M_{F1,J2}$	$M_{F1,J3}$	$M_{F1,J4}$	$M_{F1,M}$	$M_{F1,x}$
L_{J1}							L_{J1}	$M_{J1,J2}$	$M_{J1,J3}$	$M_{J1,J4}$	$M_{J1,M}$	$M_{J1,x}$
L_{J2}								L_{J2}	$M_{J2,J3}$	$M_{J2,J4}$	$M_{J2,M}$	$M_{J2,x}$
L_{J3}									L_{J3}	$M_{J3,J4}$	•	$M_{J3,x}$
L_{J4}										L_{J4}	$M_{J4,M}$	$M_{J4,x}$
L_M											L_M	$M_{M,x}$
L_x												L_x

Full inductance matrix with valid couplings (dots indicate invalid couplings)

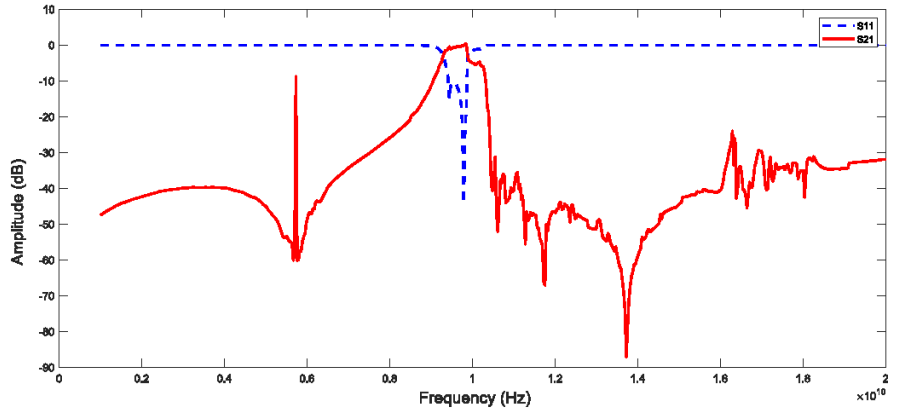
Post-SuperTools: Frequency-dependent characteristics

- Electro-magnetoquasistatic (EMQS)/Full-wave models
- S-parameter extraction of band-pass filter **with air-bridges** and **multiple dielectric layers**





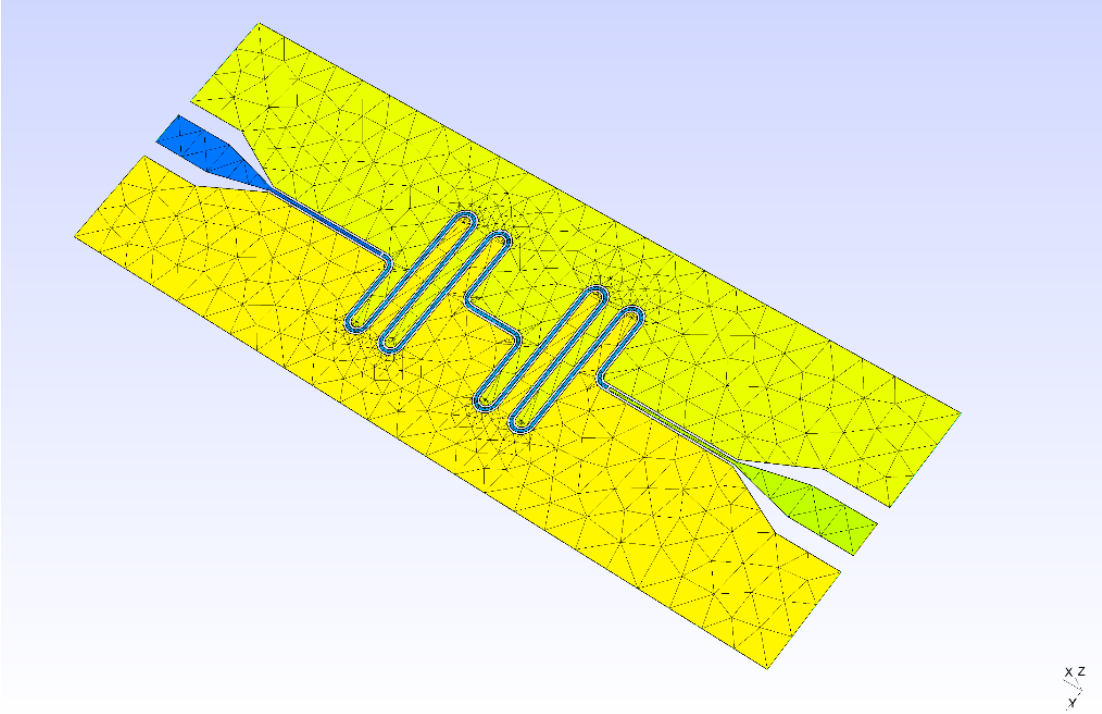
(a)

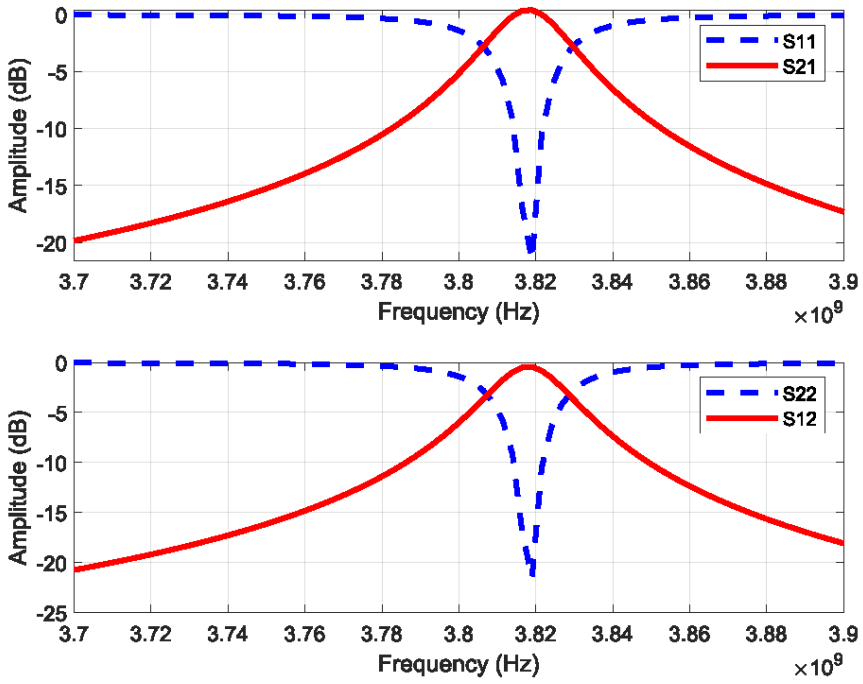


(b)

Post-SuperTools: Frequency-dependent characteristics

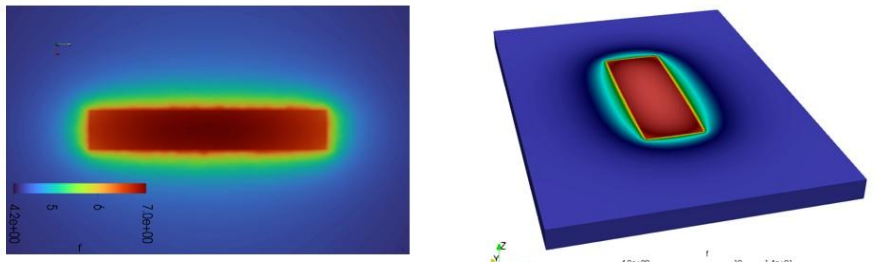
- EMQS/Full-wave: resonators
- Adaptive frequency sampling
  - high-Q resonators and superconducting transmission lines with very sharp resonances



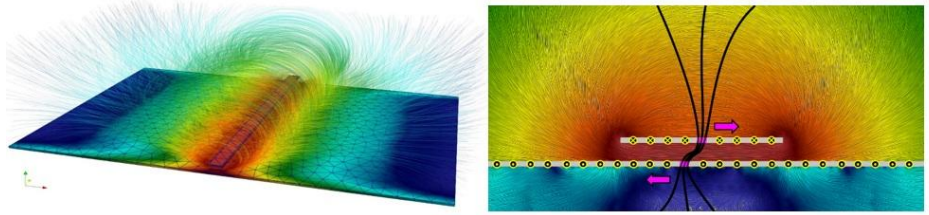


Ongoing Research

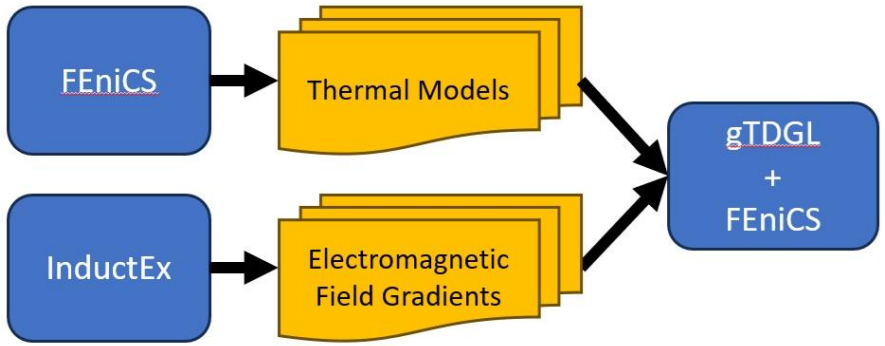
- Flux pinning and the effect on frequency response;
  - for large-scale layouts in complex 3D structures.

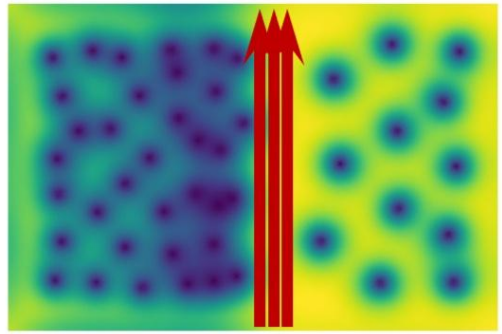


Temperature from resistor current, simulated with FEniCS.



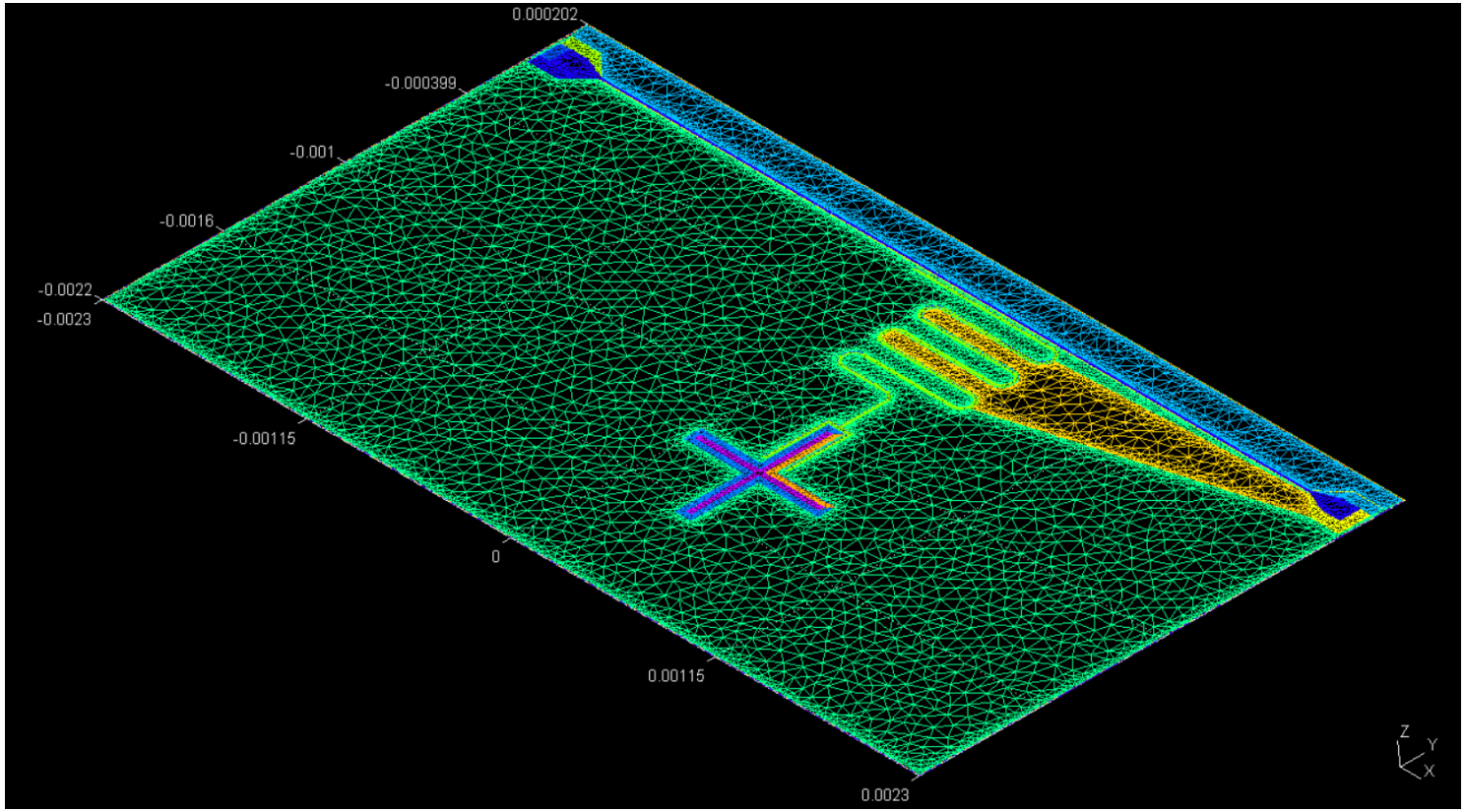
Magnetic field from microstrip current, simulated with InductEx.

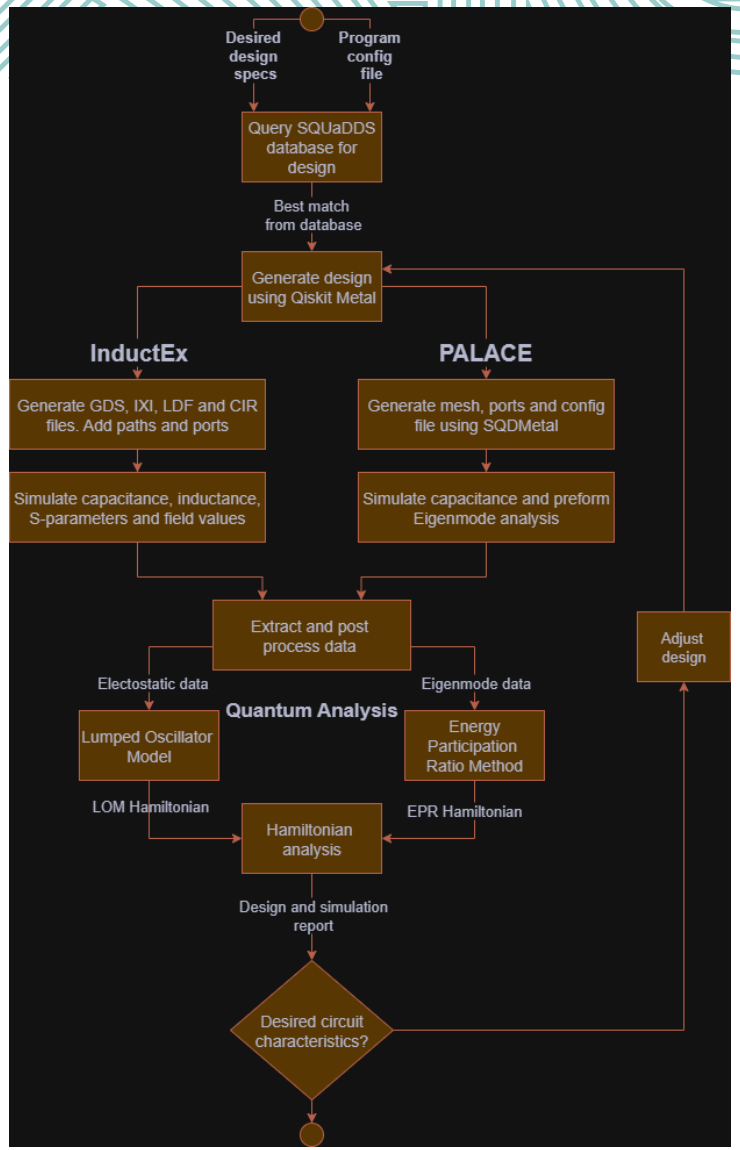




Order parameter while current is applied

Ongoing Research: Automated Hamiltonian Extraction





Summary

Domain/level	Application	Tools name	Availability
Physical	Technology CAD	FLOOXS	Academic
Physical	Parameter/compact model extraction	InductEx, TetraHenry Lmeter/3D-MLSI StarRC (Synopsys)	Commercial Academic/Free (last update 2004) Commercial
Physical	Electrical simulation	JSIM (JSIM_n) JoSIM & JoSIM-Pro WRSpice HSPICE PSCAN2	Open-source Open-source & Commercial Open-source Commercial Free
Physical	Layout-versus-schematic verification, DRC	SpiRA InductEx-LVS Cadence ASSURA	Academic Commercial Commercial
Digital system	Logic simulation	iVerilog NC Verilog	Open-source Commercial
Digital system	Synthesis, place-and-route	qPalace, Yosys In-house tools for AQFP IC Validator/Design Compiler (Synopsys)	Open-source Academic Commercial
Quantum	Qubit Design and simulation	Qiskit SQDMetal Keysight EDA EDA-Q	Open-source Open-source Commercial Open-source

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SUN Magnetics

Thank you

Photo by Stefan Els