17th European Conference on Applied Superconductivity
21-25 September 2025, Porto, Portugal

Superconducting Digital Electronics: Current Advances and the Beginning of a New Era

Nobuyuki Yoshikawa

Yokohama National University, Japan

Outline

- Background and motivation
- Introduction to superconducting digital electronics (SDE)
  - Single flux quantum (SFQ) logic
  - Adiabatic quantum flux parametron (AQFP) logic
- Recent advancements in SDE
- New research activities in SDE
- Challenge in SDE
- Conclusions

Background

Estimated power consumption to achieve 10 exa-scale computing

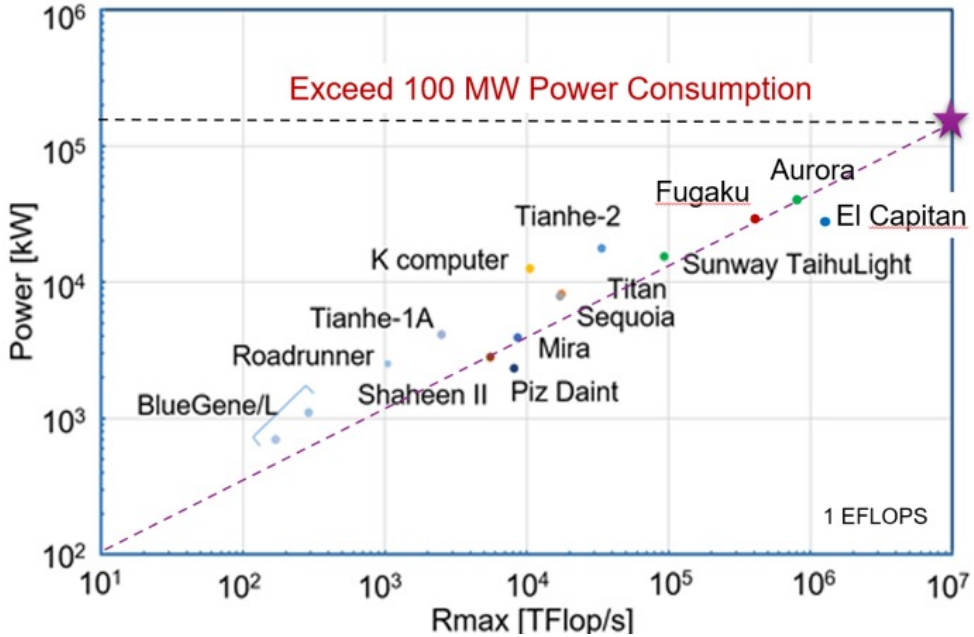
~ 100 MW ~ $100 million per year

Fugaku (Japan)

Peak performance: 513 PFLOPS

Power consumption: 28.3 MW

1st-ranked computers in recent TOP500



http://www.top500.org/

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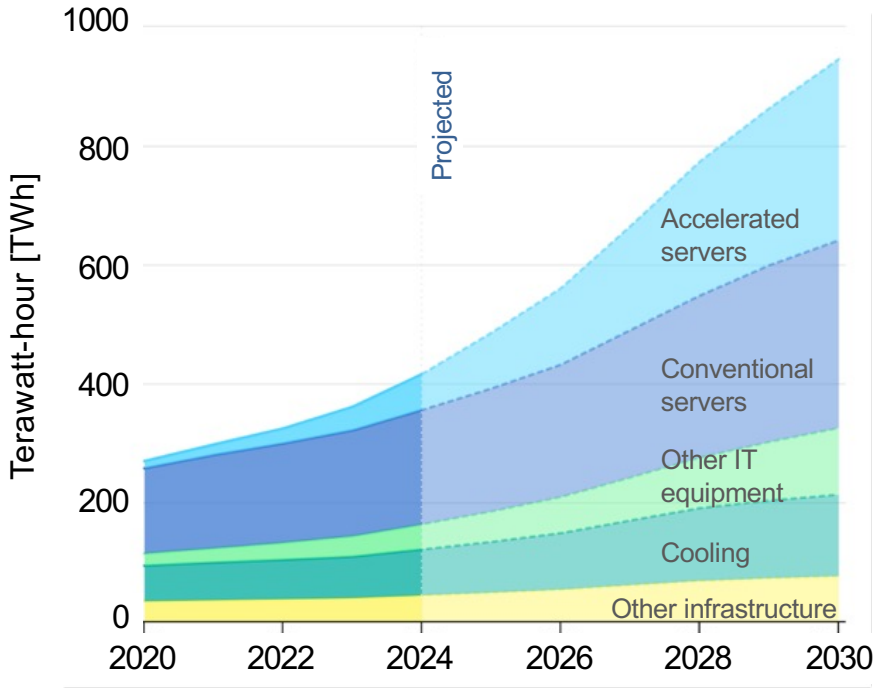
Global Data Center Electricity Consumption

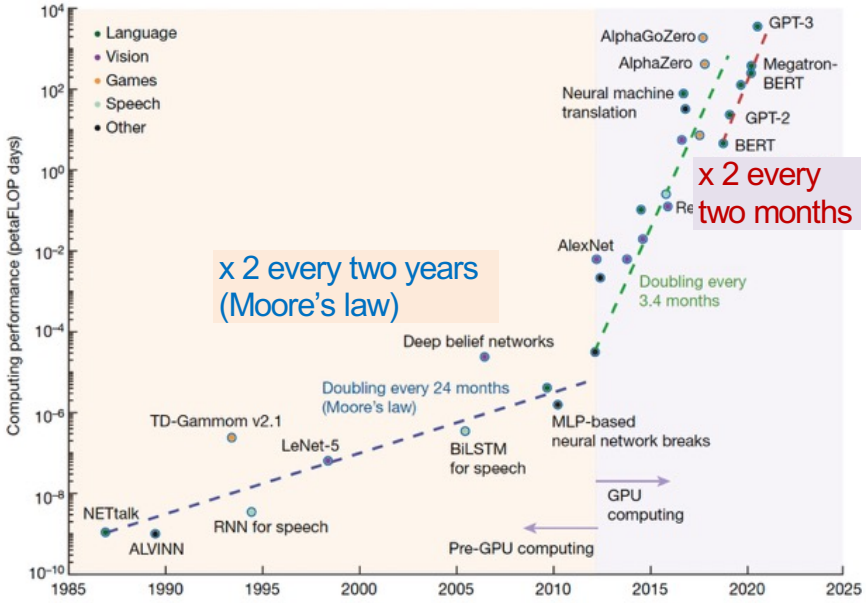


- Global electricity demand from data centers is projected to more than double by 2030, reaching ~945 TWh.
- This demand is equivalent to Japan's entire electricity consumption today.
- AI is the primary driver of this rapid growth.

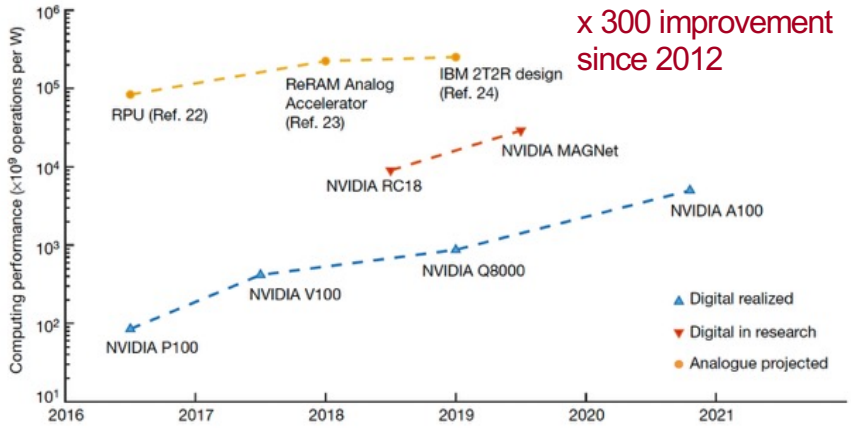
IEA Report, 2025

Computing Power Demand and Hardware Efficiency

Computing Power demand over the past 40 years



AI hardware efficiency over the past five years



Mehonic, A., Kenyon, A.J. Brain-inspired computing needs a master plan. *Nature* **604**, 255–260 (2022).

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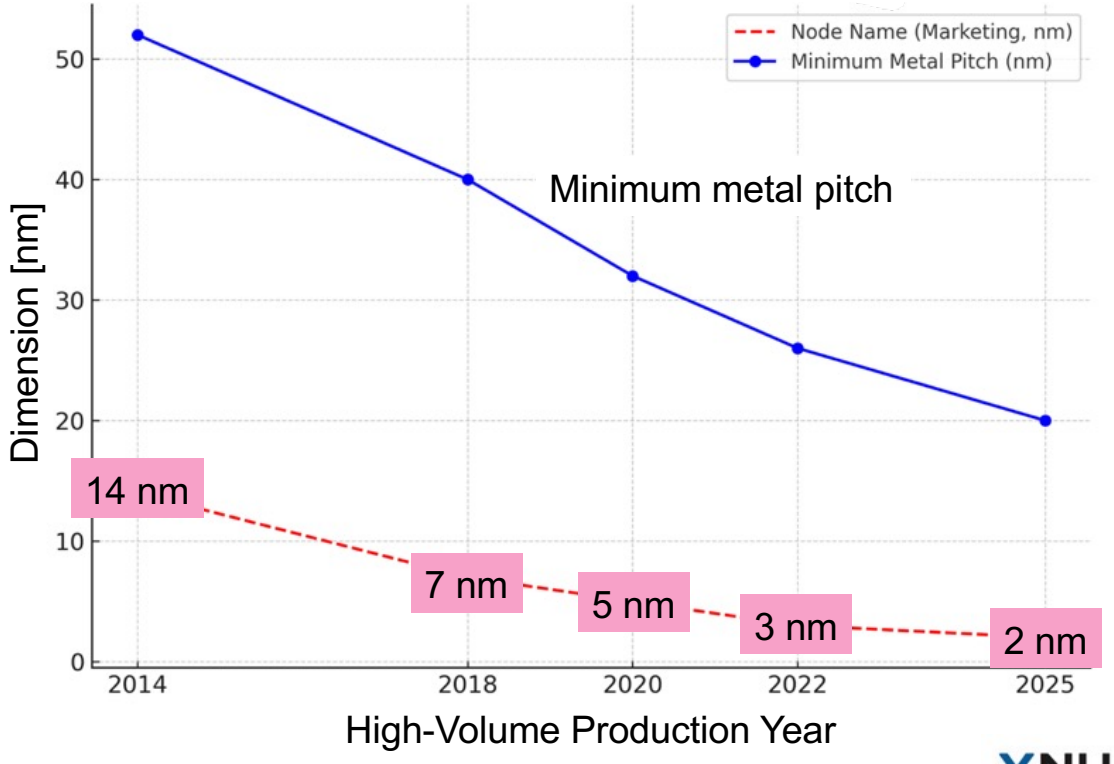
Technology Node vs. Minimum Metal Pitch



There is a large discrepancy between technology node names and the actual minimum metal pitch!

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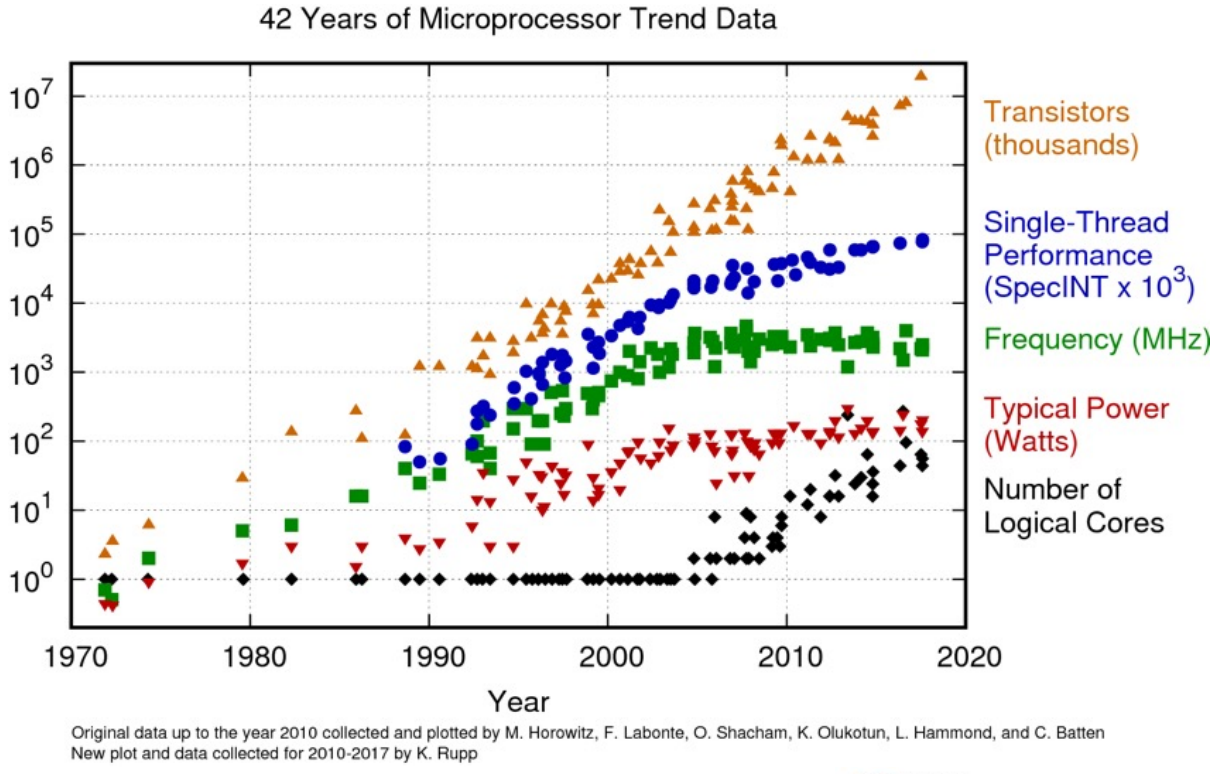
End of the Moore's Law



Rupp, K. (2018). 42 Years of Microprocessor Trend Data [Data set]. GitHub. https://github.com/karlrupp/microprocessor-trend-data

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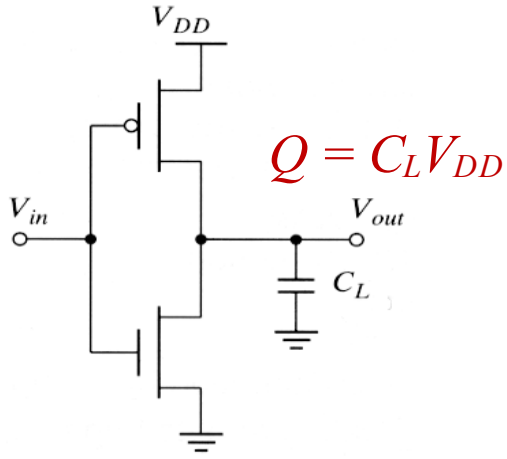
Single-Flux-Quantum (SFQ) Circuits

CMOS circuits



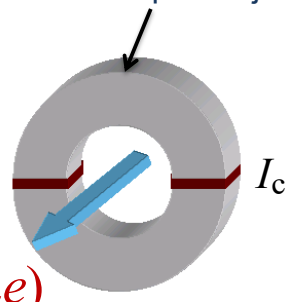
$$Q = C_L V_{DD}$$

Switching energy

$$E = QV_{\mathrm{DD}} \sim 10^{-16}\ \mathrm{J}$$

SFQ circuits

Superconducting loop
with Josephson junctions

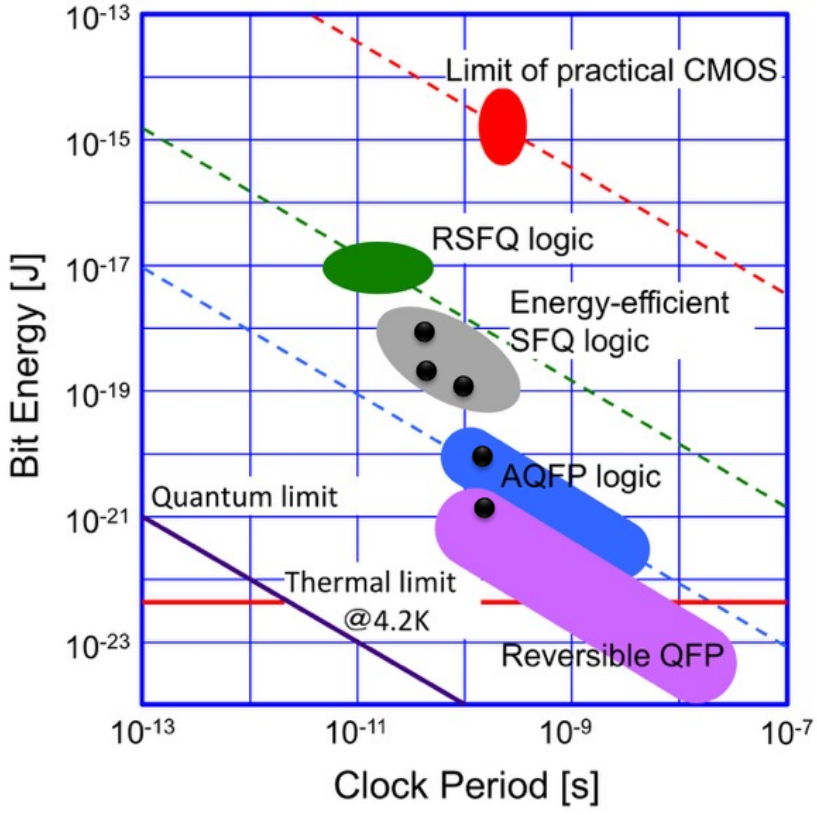


$$\Phi_0 = h/(2e)$$

Switching energy

$$E = \Phi_0 I_c \sim 10^{-19}\ \mathrm{J}$$

Energy and Delay of Superconductor Logic



Quantum limit

$\Delta E \Delta \tau \sim h$

Thermal limit (Landauer's limit)

$E \sim k_B T \ln 2$

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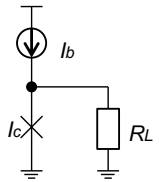
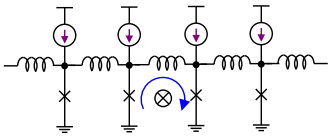
Classification of Josephson Logic

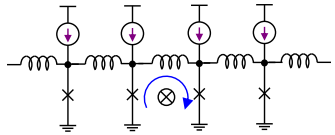
- Latching logic



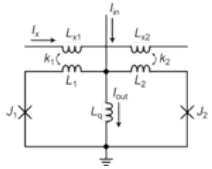
- SFQ-based logic



  - RSFQ



    - DC powered
      - RSFQ
      - LR SFQ, LV SFQ
      - ERSFQ, eSFQ
      - Dynamic SFQ
      - HFQ
      - Temporal SFQ
      - Ballistic SFQ
    - AC powered
      - AC-SFQ
      - RQL, PCL
  - QFP



    - AQFP
    - DQFP
    - RQFP
    - nSQUID

Red color: Circuits with more than 1,000 junctions have been demonstrated.

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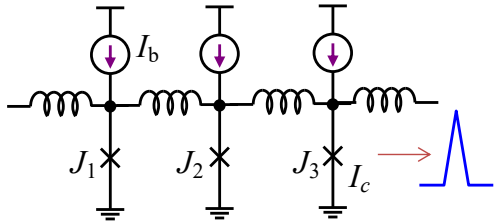
Superconducting Digital Logic

Rapid single-flux-quantum (RSFQ) logic and its energy-efficient variants



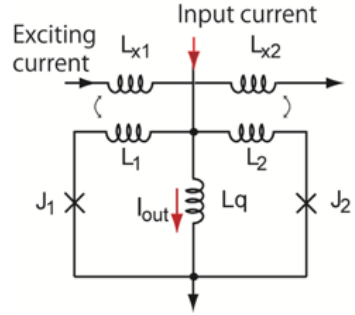
- DC Powered
- Operating speed → very fast

  $f_{clock} \sim 50$ -100 GHz
- Switching energy → small

  $E_b \sim I_c\Phi_0 \sim 100\ k_BT$

RSFQ: K. Likharev *et al*. *IEEE Trans. Appl. Supercond.* 1, 3 (1991).
ERSFQ: O. A. Mukhanov, *IEEE Trans. Appl. Supercond.* 21, 760 (2011).
eSFQ: M. Volkmann *et al.*, *Supercond. Sci. Technol.* **26**, 015002 (2013).
LVSFQ: M. Tanaka *et al., IEEE Trans. Appl. Supercond*. **23**, 1701104 (2013).

Adiabatic quantum flux parametron (AQFP) logic



- AC Powered
- Operating speed → fast

  $f_{clock} \sim 5$ - 10 GHz
- Switching energy → very small

  $E_b << I_c\Phi_0 \sim\ k_BT$

QFP: K. Loe, E. Goto, IEEE Trans. Magn. 21, 884 (1985).
AQFP: N. Takeuchi, *et. al*., *SUST*, 26, 035010 (2013).

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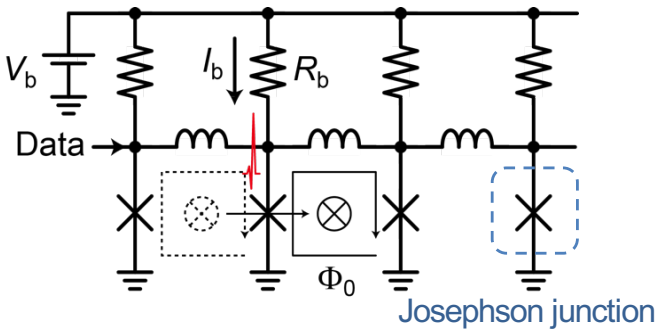
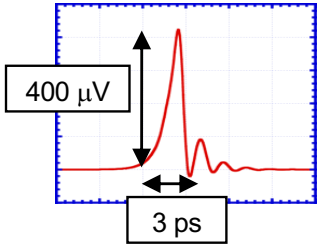
Rapid Single-Flux-Quantum (RSFQ) Logic

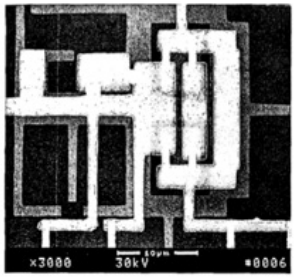




- Pulse height ~ 400 μV
- Pulse width ~ 3 ps
- Power ~ nW/gate

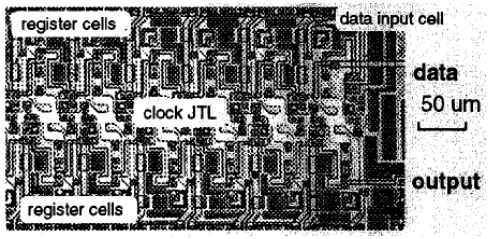
K. K. Likharev, V. K. Semenov, *IEEE Trans. Appl. Supercond.* 1, 3–28 (1991).

T Flip-flop operating at up to 770 GHz.



W. Chen *et al.*, *IEEE Trans. Appl. Supercond.* 9, 3212–3215 (1999).

256-b shift register operating at 12 GHz



O. Mukhanov *et al., IEEE Trans. Appl. Supercond 3,* 2578-2581 (1993*)*.

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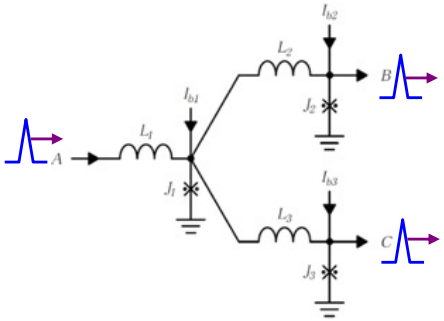
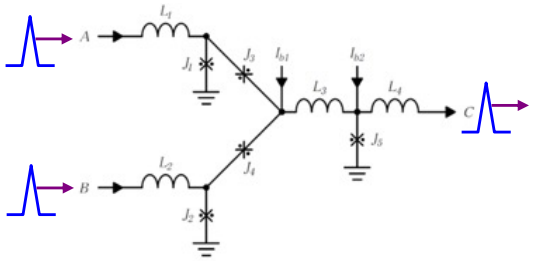
Basic Logic Components in RSFQ

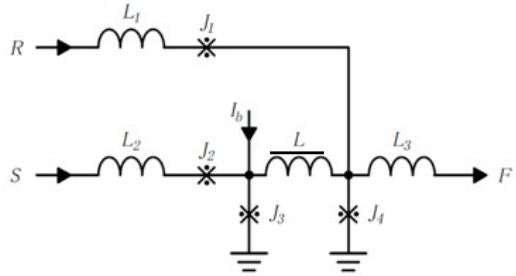
Splitter



Confluence buffer

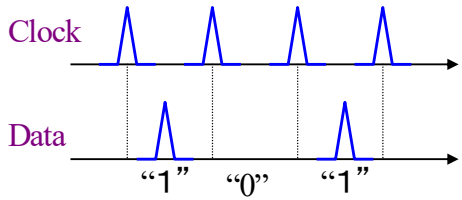


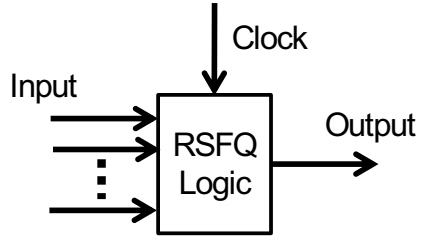
D flip-flop (DFF)



$$I_c L > \Phi_0$$

Representation of Logical States in RSFQ Logic





K. K. Likharev, V. K. Semenov, *IEEE Trans. Appl. Supercond.* 1, 3–28 (1991).

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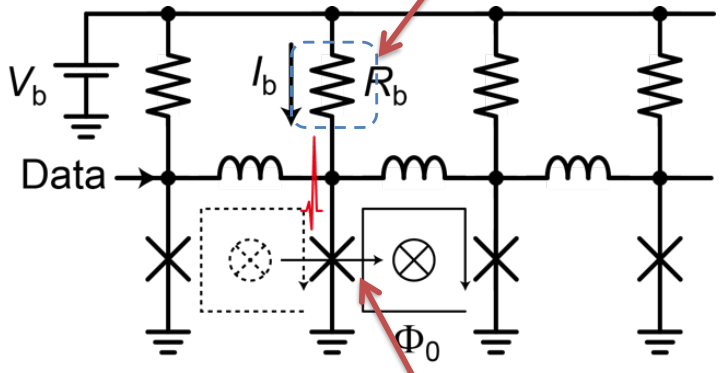
Power Consumption in RSFQ Logic

Static power dissipation:
$P_S = R_b I_b^2$



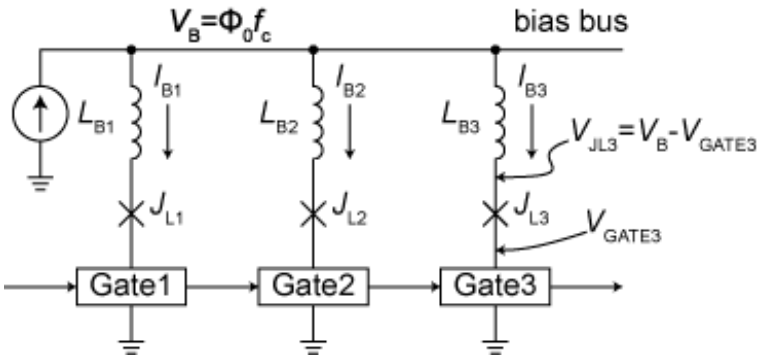
$P_D \sim P_S/20$

Dynamic power dissipation:
$P_D = \Phi_0 I_c f$

Reduction of static power is required.

Energy-Efficient RSFQ (ERSFQ) Logic

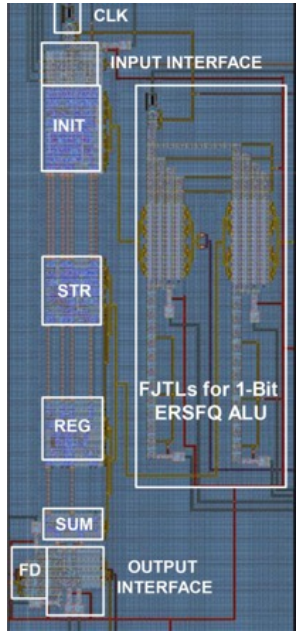
- Bias resistors are replaced with inductors and Josephson junctions.
- A feeding JTL is required, which introduces additional switching energy.



$$P_S \sim P_D \sim I_c \Phi_0 f$$

Hypres O. A. Mukhanov, *IEEE Trans. Appl. Supercond.* **21**, 760 (2011).

Demonstration of ERSFQ Arithmetic Logic Unit



- Fabrication process: MIT-LL 100 μA/μm^2 SFQ5ee
- Maximum operating speed: 30 GHz
- Total bias current: ~400 mA

A. Inamdar *et al.*, *IEEE Trans. Appl. Supercond.* **33**, 1300908 (2023).

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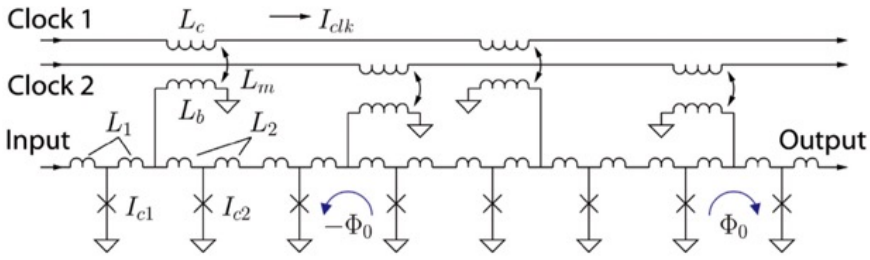
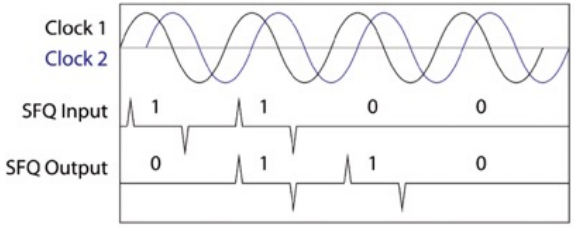
Reciprocal Quantum Logic (RQL)

- A 4-phase AC bias current propagates digital "1" as pairs of SFQ pulses with opposite polarity.
- Gates can be biased in series.

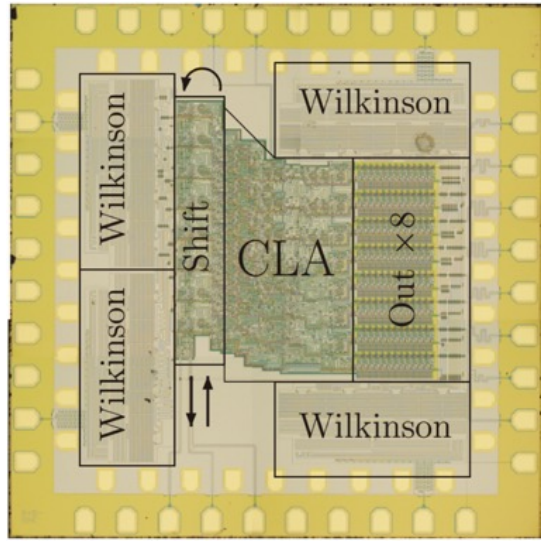




$P_S \sim 0$,
$P_D \sim I_c \Phi_0 f$

Northrop Grumman Q. P. Herr *et al., J. Appl. Phys.* **109**, 103903 (2011).

Demonstration of 8-bit carry look-ahead adder at 10 GHz



- Fabrication process: Hypres 2 um Nb process
- Power dissipation: 510 nW at 6.2 GHz

A. P. Herr *et al., J. Appl. Phys.* **113**, 033911 (2013).

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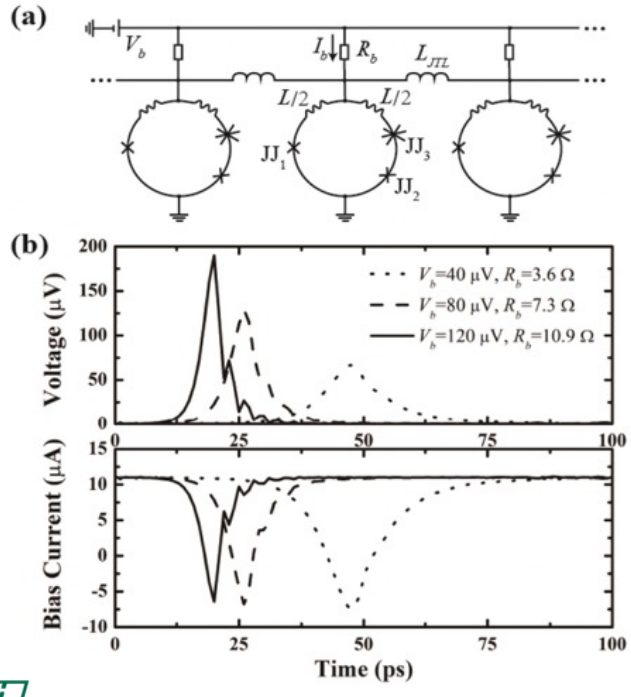
Half Flux Quantum (HFQ) Logic

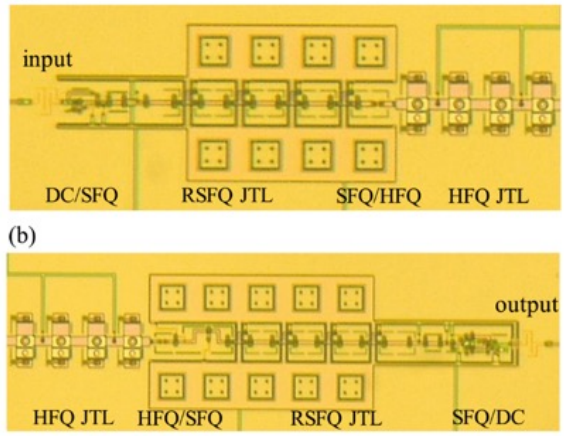
HFQ JTL



F. Li, *et al., Supercond. Sci. Technol.* 34, 025013, 2021.

- A SQUID with a π junction is used to reduce the effective critical current.
- A half flux quantum propagates in the HFQ JTL.
- Reduced energy consumption is expected.

Demonstration of HFQ JTL



D. Hasegawa *et al., IEEE Trans. Appl. Supercond.* 31, 1101504, 2021.

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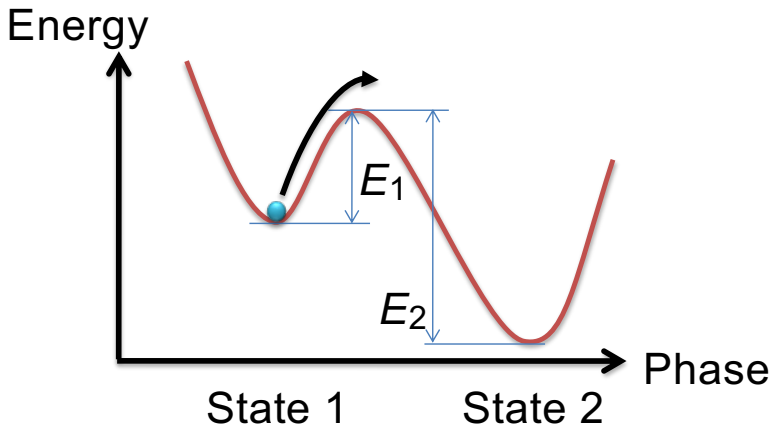
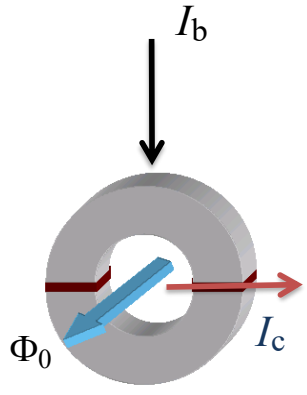
Energy Potential of RSFQ Logic





$E_2 \sim \Phi_0 I_c \sim 10^{-19}$ J

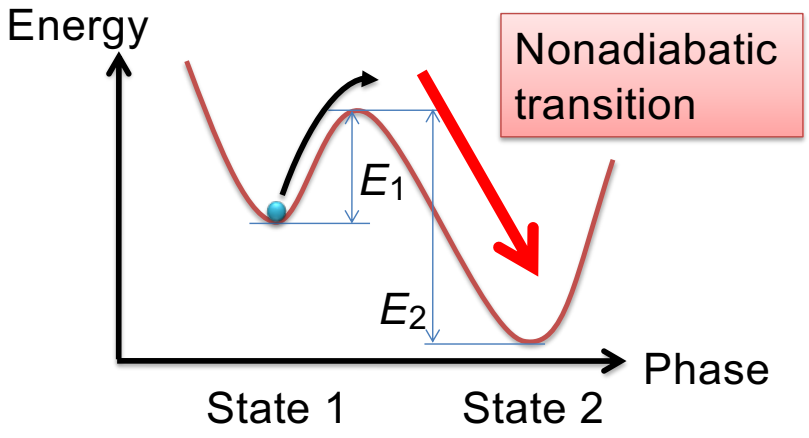
Input energy: E_1
Output energy: E_2

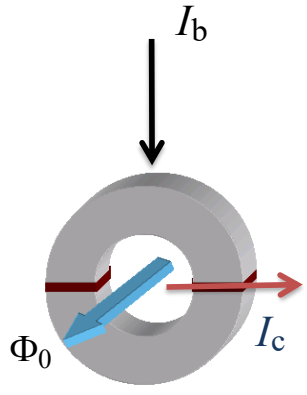
Energy dissipation: E_2

Requirement for the reduction of switching errors

$E_1 > 100\ k_B T$

Energy Potential of RSFQ Logic





$E_2 \sim \Phi_0 I_c \sim 10^{-19}$ J

Input energy: E_1
Output energy: E_2

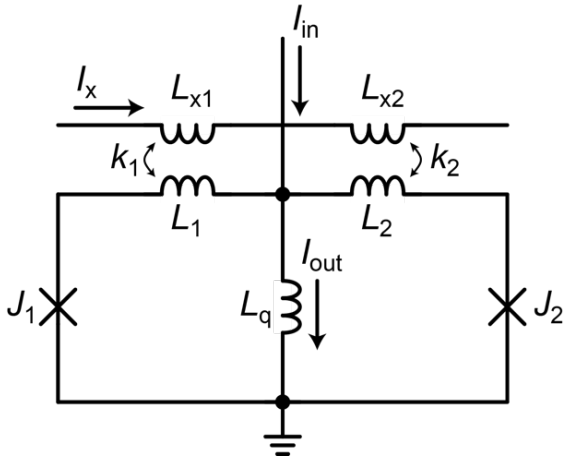
Energy dissipation: E_2

Requirement for the reduction of switching errors

$E_1 > 100\ k_B T$

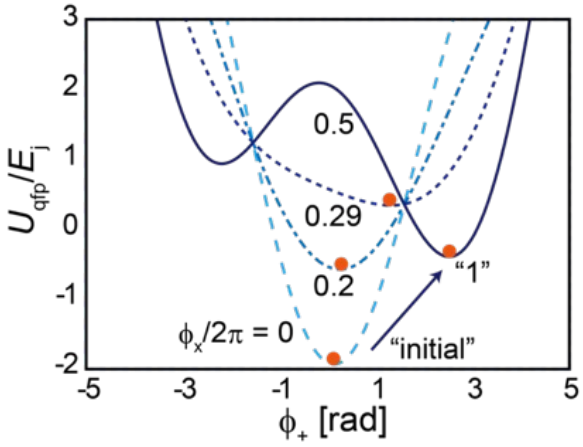
Adiabatic Quantum Flux Parametron (AQFP) Logic

AQFP gate



An SFQ is stored in the right or left loop depending on I_{in}.

Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984*.

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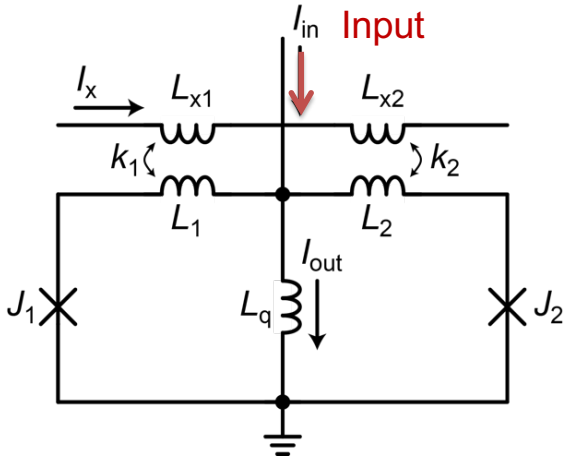
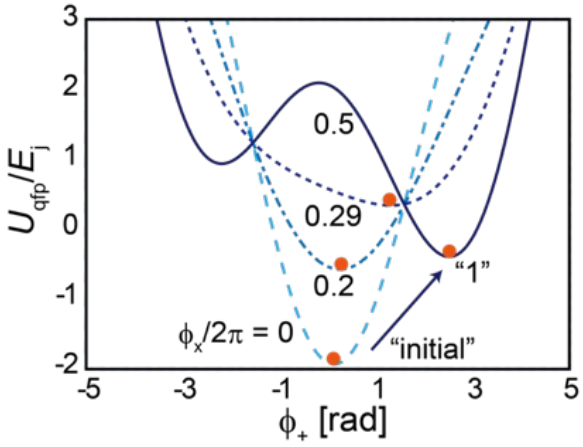
Operation Principle of AQFP Logic

AQFP gate



Potential energy of the gate



Potential energy changes adiabatically during switching.

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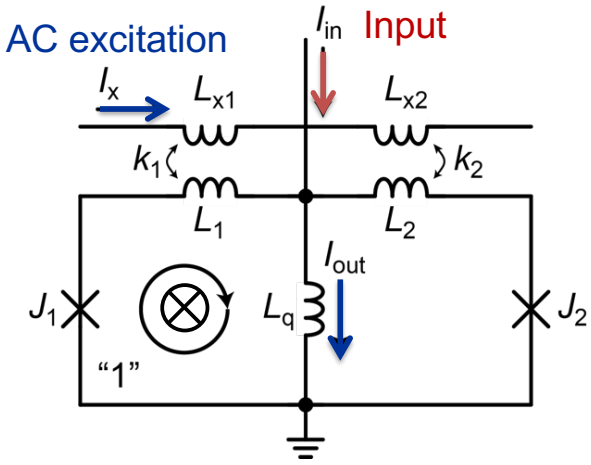
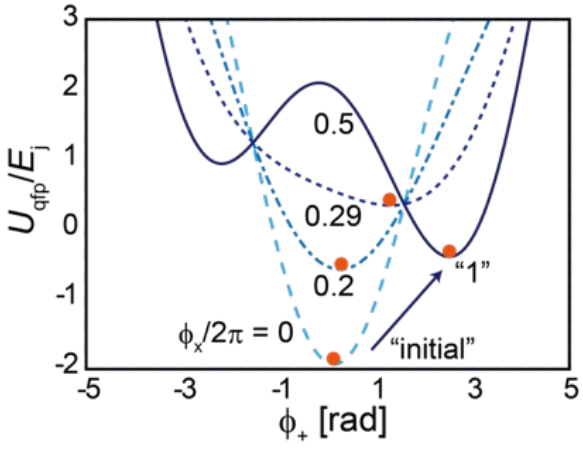
Operation Principle of AQFP Logic

AQFP gate



I_{out} flows downward.

Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984.*

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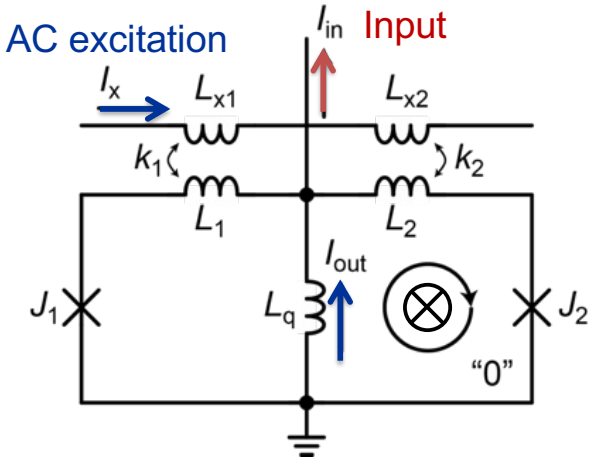
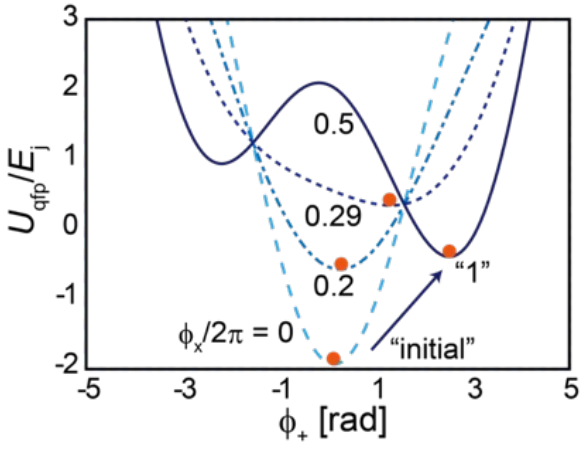
Operation Principle of AQFP Logic

AQFP gate



I_{out} flows upward.

Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984*.

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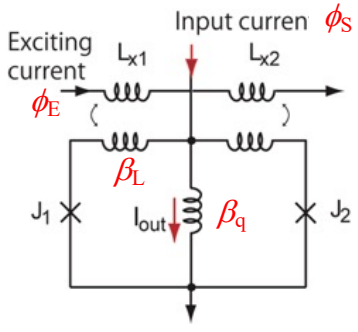
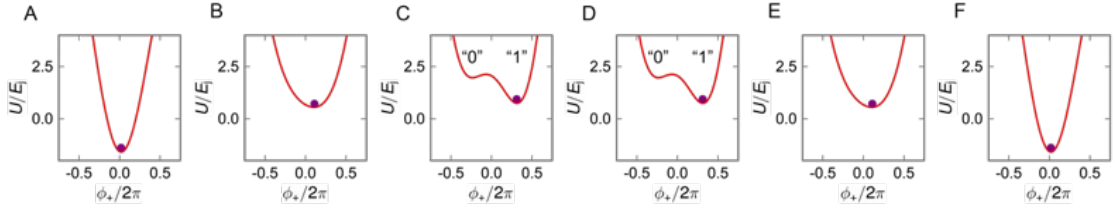
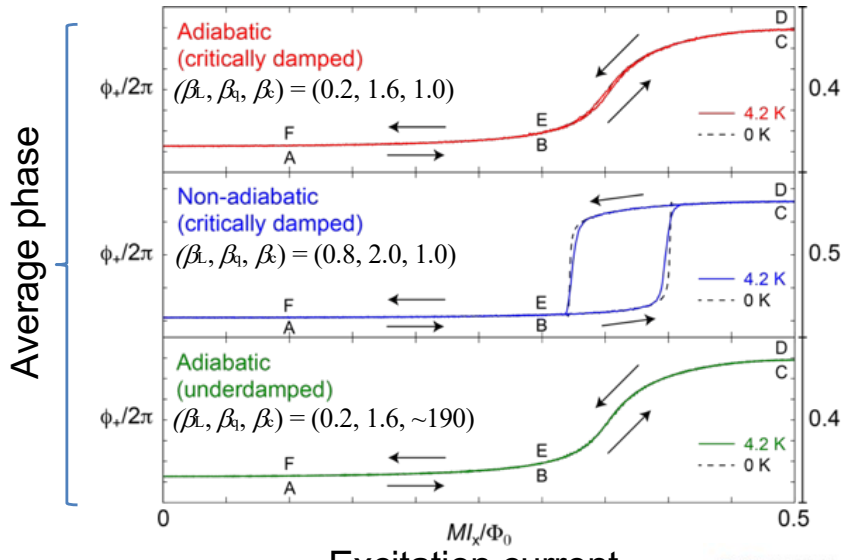
Junction Phase vs. Excitation Current of QFP



- β_c: McCumber parameter

$$\beta_c = \frac{\omega_c C}{G}$$





Junction phase of adiabatic QFP (AQFP) changes adiabatically.

Takeuchi *et al.*, Phys. Rev. Appl. 4, 034007 (2015).

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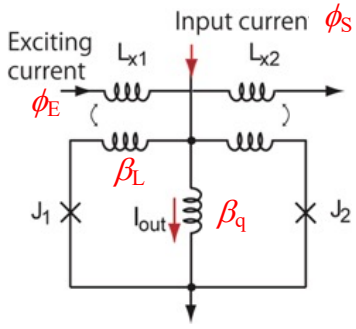
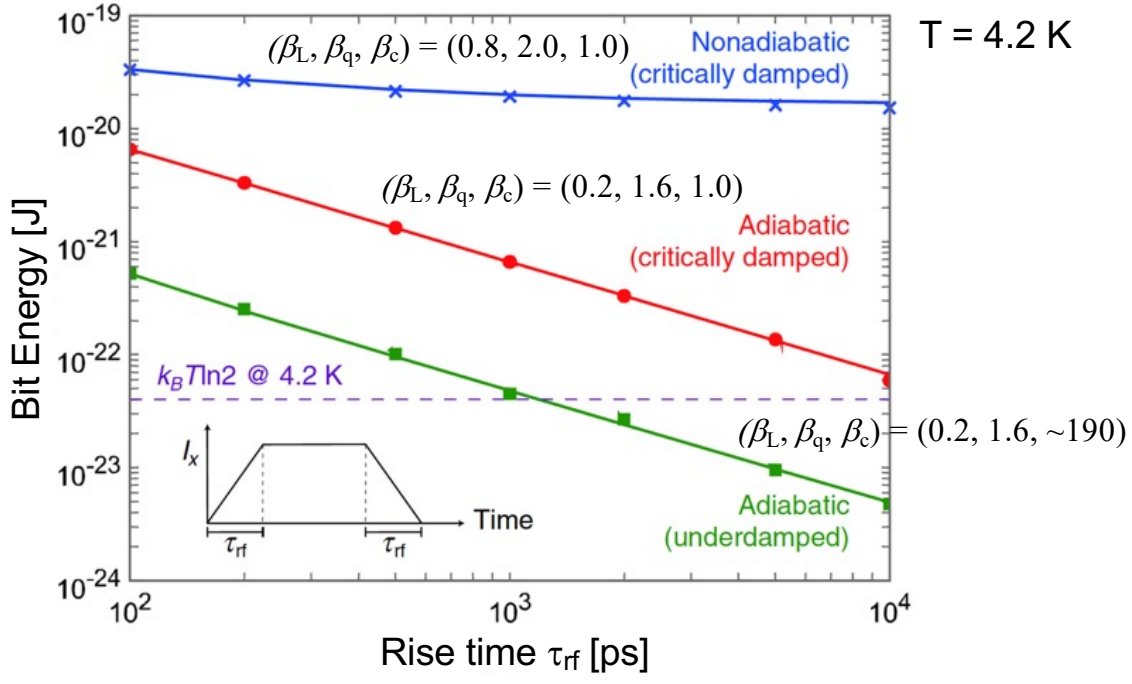
Bit Energy vs. Rise Time of Excitation Current of AQFP



- β_c: McCumber parameter

$$\beta_c = \frac{\omega_c C}{G}$$



T = 4.2 K

E_{bit} ~ 0.05 zJ ($\sim k_B T$) when rise time = 1000 ps

Takeuchi *et al.,* Phys. Rev. Appl. 4, 034007 (2015).

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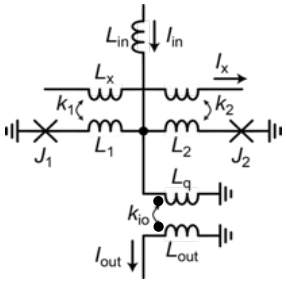
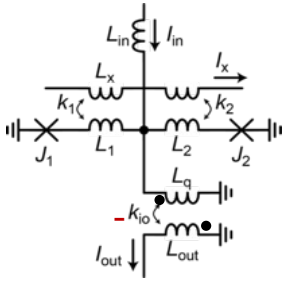
Design of AQFP Logic

- NOT gate is cost free.
- Majority gate is a basic logic gate.

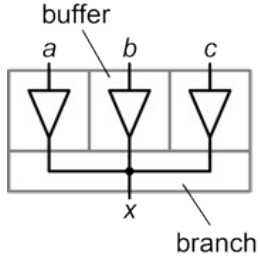
Buffer



NOT

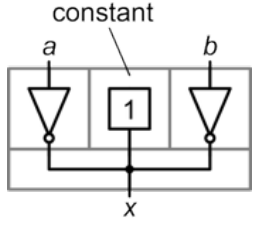


Majority



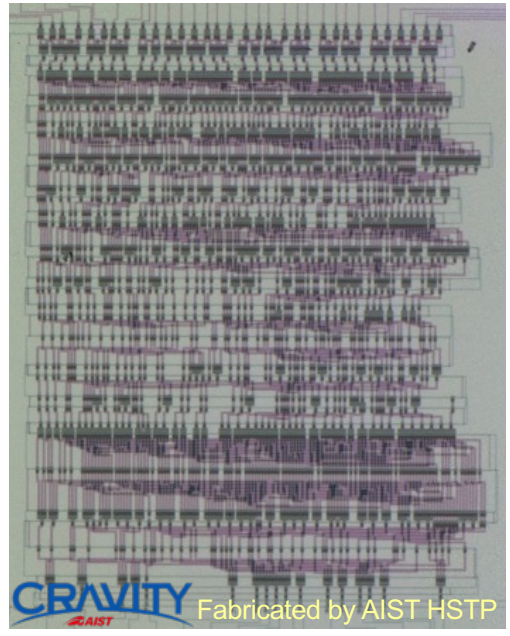
$x = \mathrm{MAJ}(a, b, c)$
$= ab+bc+ca$

NAND



$x = \mathrm{MAJ}(\bar{a}, 1, \bar{b})$
$= \overline{ab}$

Demonstration of AQFP 16b Carry Look-Ahead Adder



K. Inoue, *et al*. IEEE Trans. Appl. Supercond., **23**, 1301105 (2013).

T. Tanaka *et al*., IEICE 105-C, 2022

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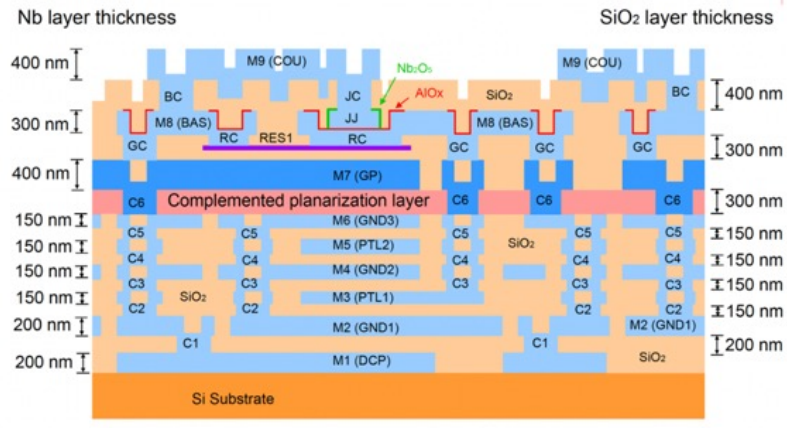
Outline

- Background and motivation
- Introduction to superconducting digital electronics (SDE)
  - Single flux quantum (SFQ) logic
  - Adiabatic quantum flux parametron (AQFP) logic
- Recent advancements in SDE
- New research activities in SDE
- Challenge in SDE
- Conclusions

Development of Process Technologies

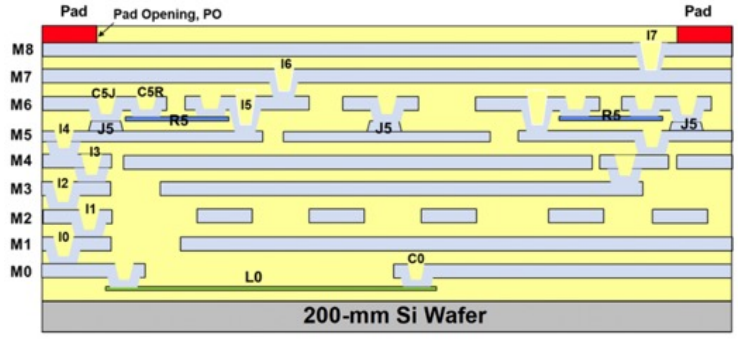
- Multilayer Nb-based Josephson IC processes have been developed worldwide, including in Japan, the United States, Germany, and China.
- Most use Nb/Al-AlOx/Nb junctions with J_c ranging 1-10k A/cm^2.

AIST-Qufab Nb 9-layer Advanced Process



MIT LL SFQ5ee+ Josephson Process

8-metal-layer Nb/AlOx/Nb 10-kA/cm^2 Josephson process



Josephson circuits with ~10k-scale are available in these processes.

S. Nagasawa and M. Hidaka, J. Physics: Conf. Series 871, 012065, 2017. S. K. Tolpygo *et al.*, *IEEE TAS*, 35, 1300806, 2025.

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Development of Design Technologies

ColdFlux project (2017-2022)

- Developed a complete chain of **digital and analog S-EDA tools** (front-end to back-end), supported by the IARPA SuperTools program.

Performers:

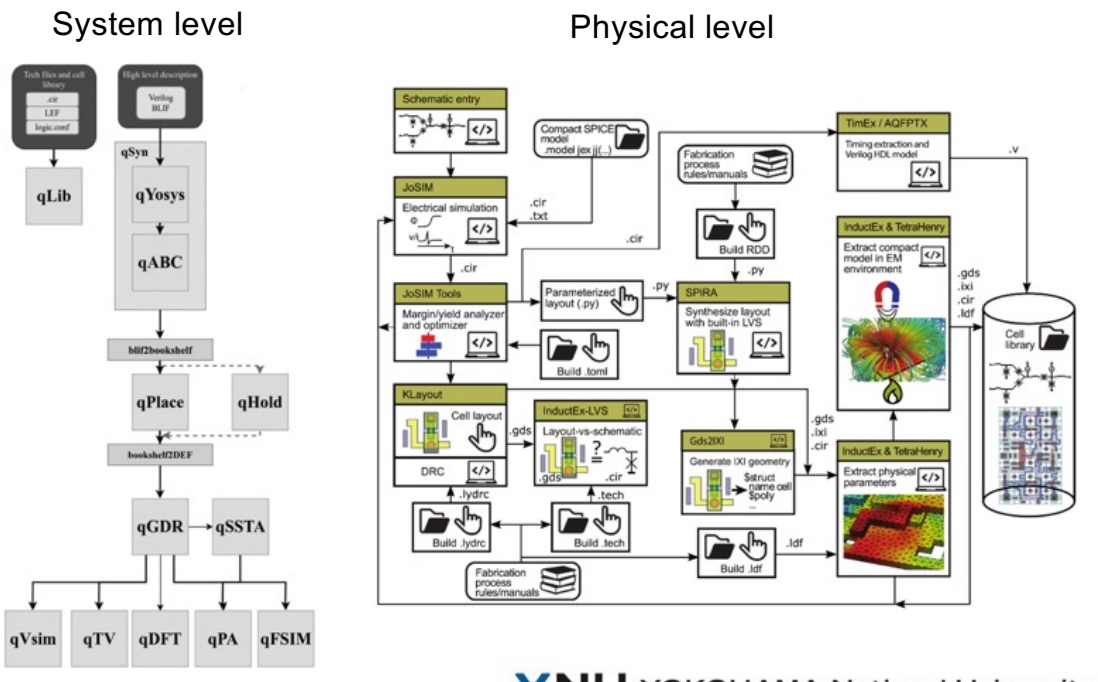
- University of Southern California
- Northeastern University
- Stellenbosch University
- University of Florida
- University of Savoie Mont Blanc
- Yokohama National University

Parallel effort

- A **Synopsys** project developed a **commercial EDA toolchain** in parallel.

C. Fourie, *et al., IEEE TAS,* 33, 1304926, 2023

ColdFlux tool flow



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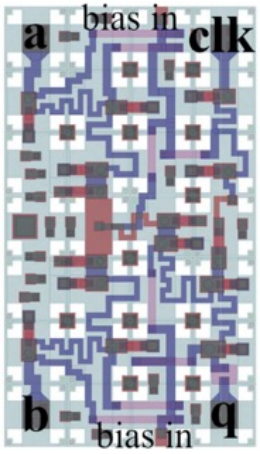
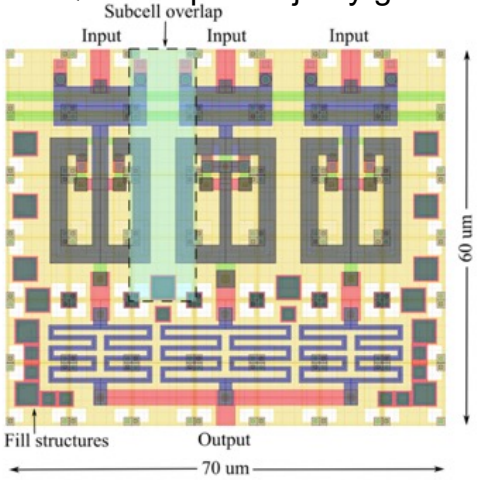
Results from the ColdFlux Project

Cell layouts using MIT LL SFQ5ee process

RSFQ 2-input OR gate

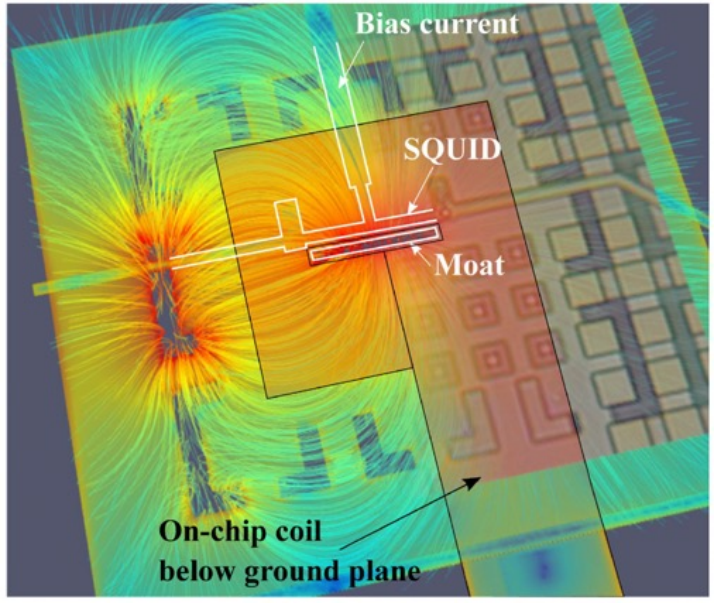


AQFP 3-input majority gate



- A parameterized cell design approach is employed.
- Layouts use a 10 x 10 μm track block, enabling SFQ-AQFP hybrid systems.

Magnetic field created by a trapped fluxon



Simulated by InductEX

C. Fourie, *et al., IEEE TAS,* 33, 1304926, 2023

L. Schindler, *et al., IEEE TAS,* 33, 1304905, 2023

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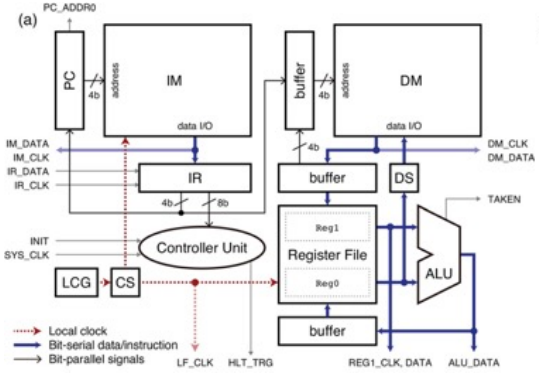
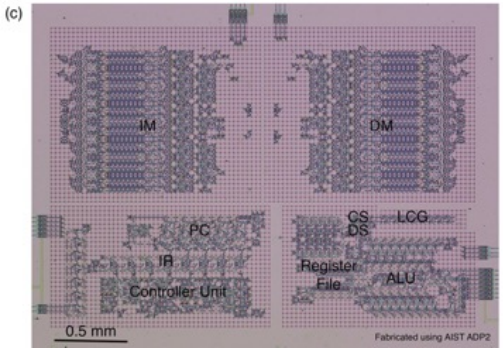
Demonstration of an RSFQ Microprocessor

An RSFQ bit-serial 8-bit microprocessor with SFQ memories is operated at 60 GHz.

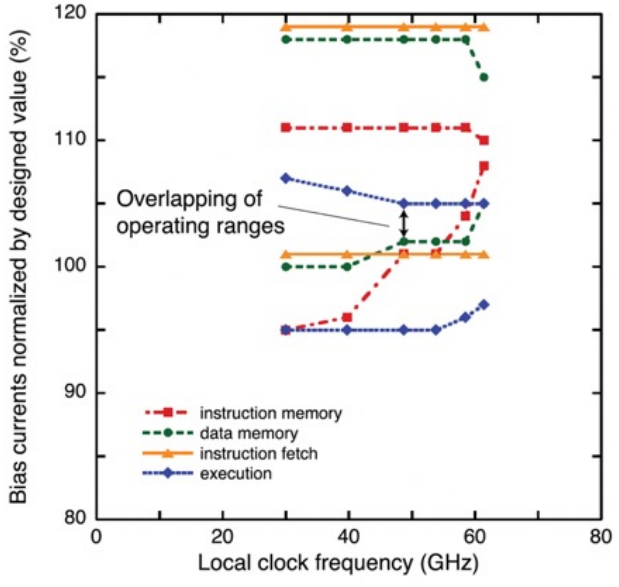
Block diagram



Die photo



Bias margins vs. clock frequencies



- Fabrication process: AIST 10-kA/cm^2 9-Nb-layer process (ADP)
- Total junctions: 11,000 JJ
- Memory size: 256 bits, Instructions: 13
- Maximum clock frequency: 60 GHz
- Power consumption: 2.5 mW

NAGOYA UNIVERSITY

M. Tanaka *et al., Appl. Phys. Lett.* 122, 192601 (2023).

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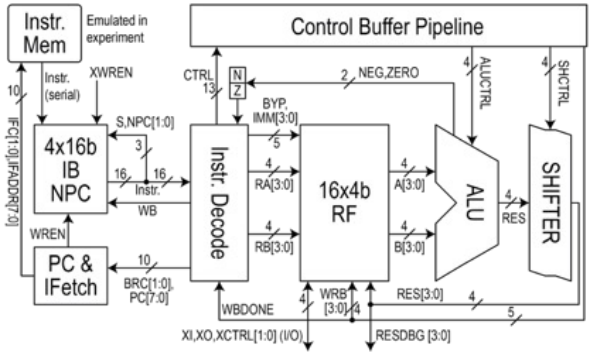
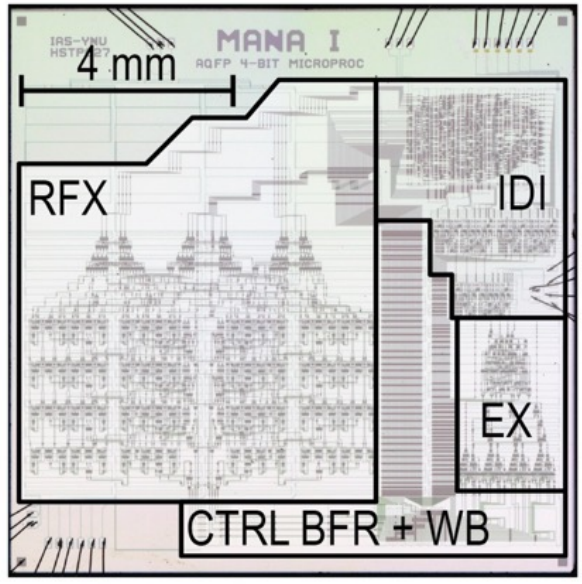
Demonstration of AQFP 4b RISC Microprocessor

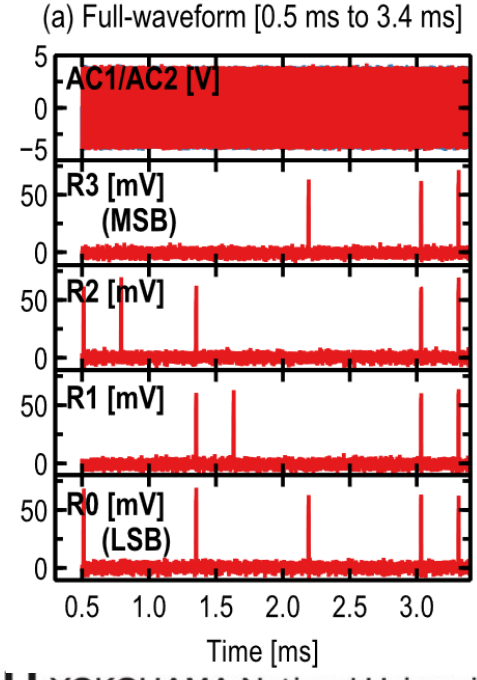
MANA – Monolithic Adiabatic iNtegration Architecture





- RISC + dataflow (4-bit data, 16-bit instruction)
- 15 aJ/op @ 5GHz
- 27 cycles/operation (5.4ns @ 5GHz)
- Nb/AlOx/Nb 10 kA/cm^2 AIST HSTP process
- 21,460 JJs on 1 x 1 cm^2 chip

Execution of Test Program: add/sub + branch



CRAVITY AIST Fabricated by AIST HSTP

C. Ayala *et al.*, IEEE Journal of Solid-State Circuits, 2020

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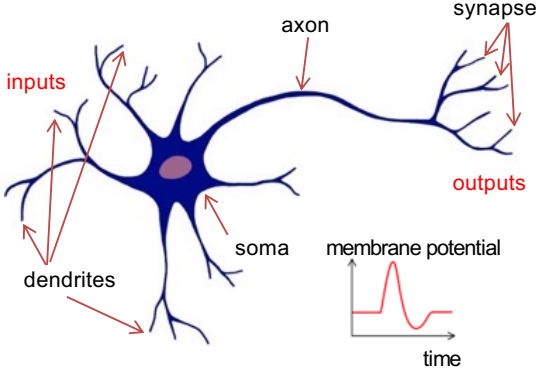
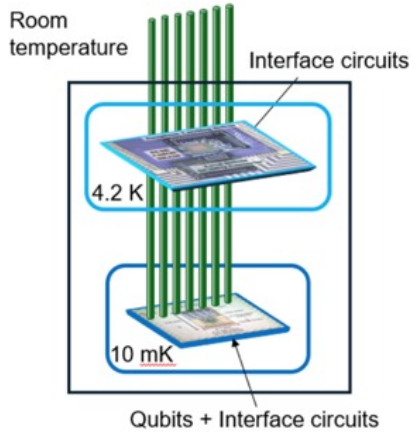
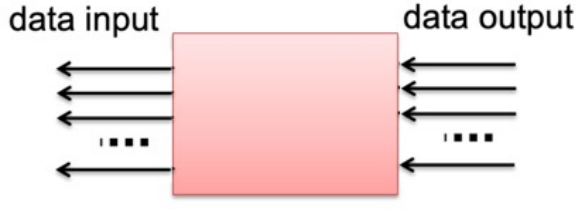
- Challenge in SDE
- Conclusions

New Research Activities in SDE

- Neuromorphic computing
- Interface with quantum computers
- Reversible computing







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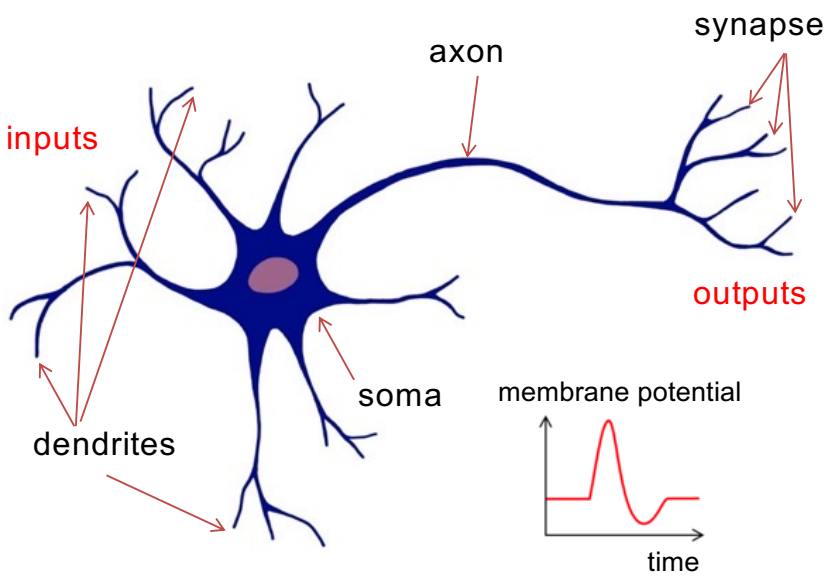
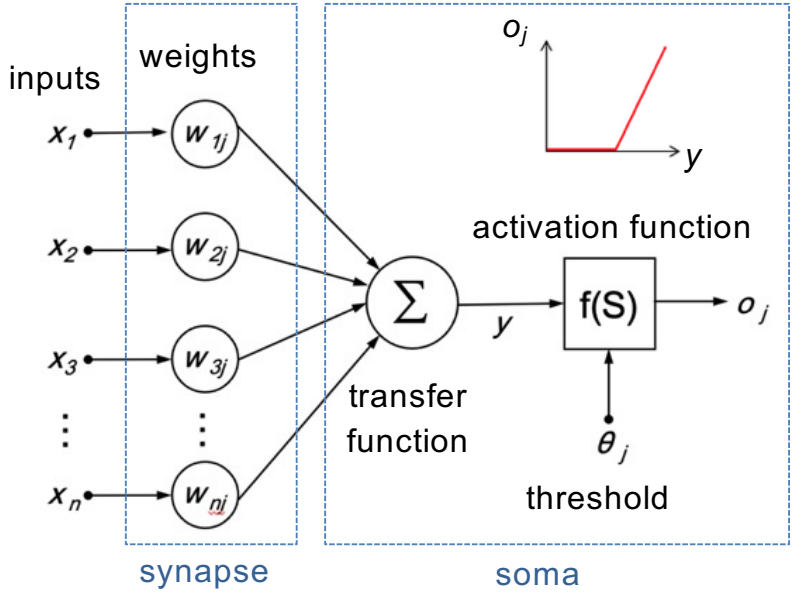
Neuromorphic Computing



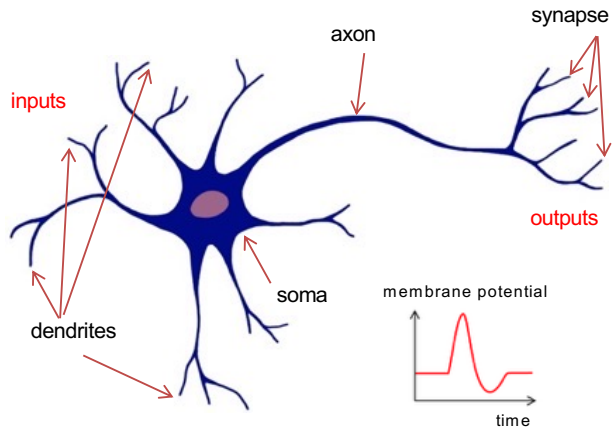
Biological neuron



Artificial neuron model

Advantages of Neuromorphic Computing

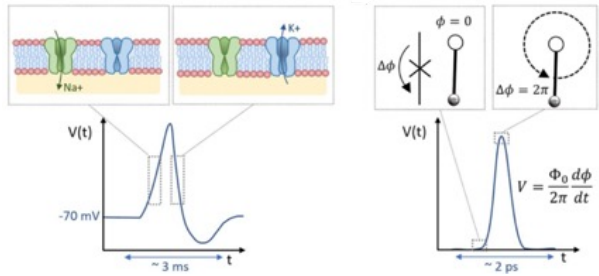
- **Massive Parallelism**
  Enables efficient large-scale data processing.
- **Memory–Computation Integration**
  Synapses combine storage and processing, eliminating the von Neumann bottleneck.
- **Event-Driven Operation**
  Circuits are activated only when spikes occur, reducing power consumption.
- **Scalability**
  System performance improves simply by adding more neurons and synapses.



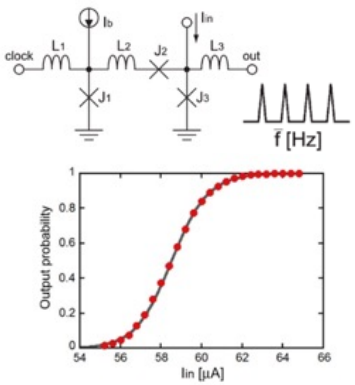
Josephson-Based Spiking Neurons

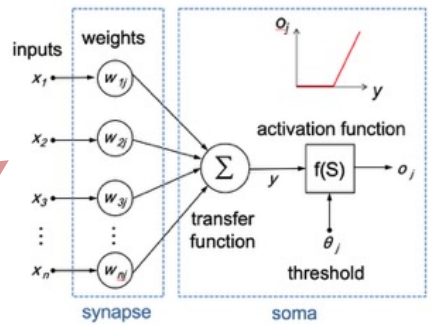
- Intrinsic spiking behavior (compact circuits)
- Ultra-fast operation (~10-100 GHz firing rates)
- Ultra-low energy consumption (~aJ per spike)

Biological action potential **SFQ pulse**

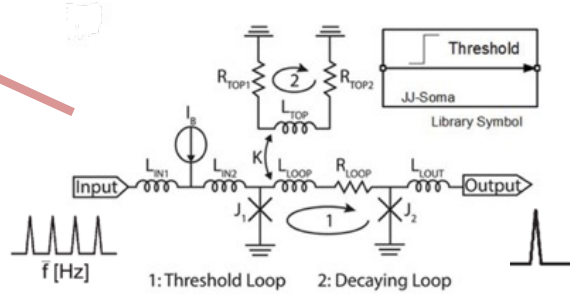


Superconducting synapse





Superconducting soma



M. Schneider *et al. Supercond. Sci. Technol.* **35** 053001,2022.
Y. Yamanashi, *et al.*, *IEEE TAS* 23, 17010042013, 2013.

A. Bozbey *et al.*, arXiv:1812.10354, 2018

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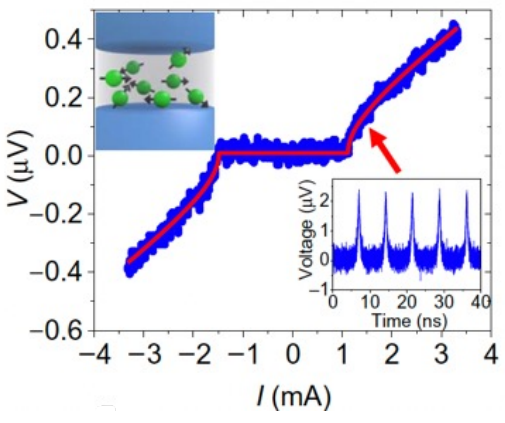
Artificial Synapses with Magnetic JJs

NIST

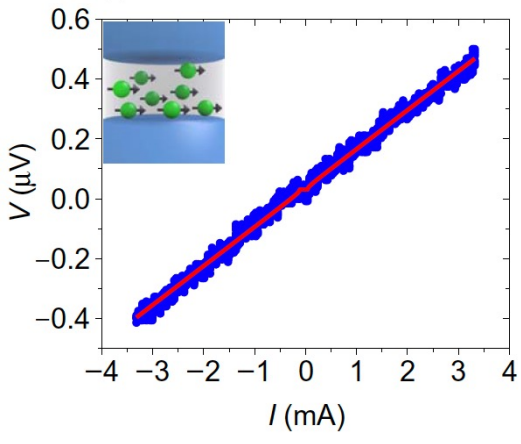
- Using Josephson junctions with magnetic nanoclusters
  - **Ultra-low energy**: spiking energy ~1 aJ (vs. ~10 fJ in human brain)
  - **Ultra-high density**: JJ size down to ~100 nm.

I-V characteristic of a 10-μm JJ synapse at 4 K

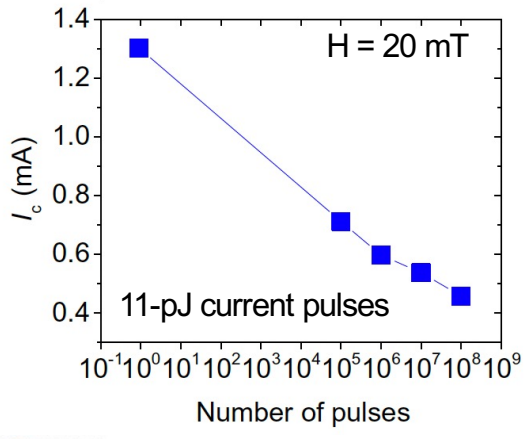
Disordered state



Ordered state



I_c as a function of ordering pulses



M. L. Schneider *et al.*, Sci. Adv. 4, e1701329 (2018).

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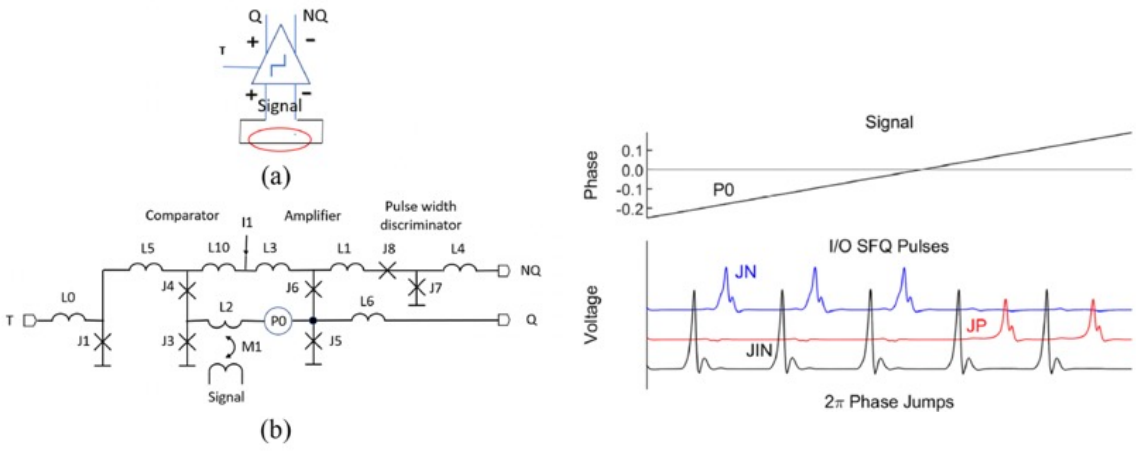
BioSFQ Circuits

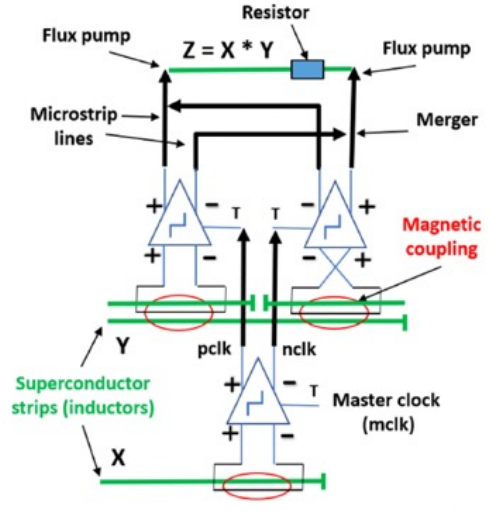
Stony Brook University, MIT Lincoln Laboratory

- Mixture of analog and digital circuits.
- Information is stored in a SC loop and transferred as a rate of SFQ pulses.

Analog comparator with complementary outputs



Bipolar analog multiplier



V. Semenov, E. Golden, S. Tolpygo, IEEE TAS, 33, 1400308, 2023.

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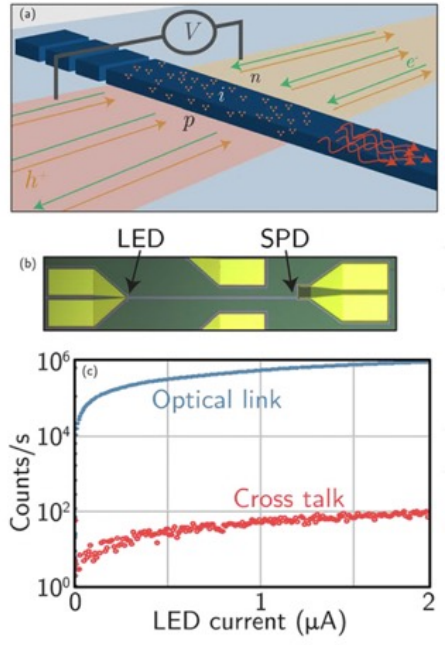
Superconducting Optoelectronic Neurons

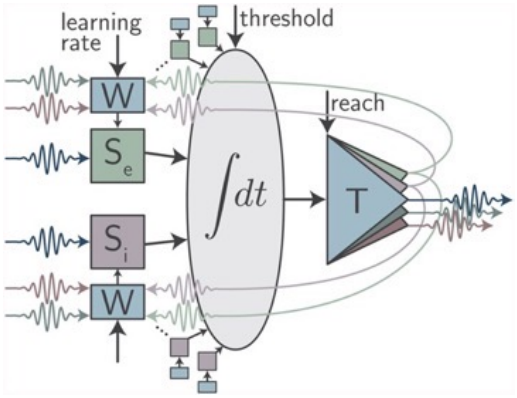
NIST

- **Communication:** Optical waveguides with LEDs and single-photon detectors (SPDs).
- **Computation:** Josephson circuits.

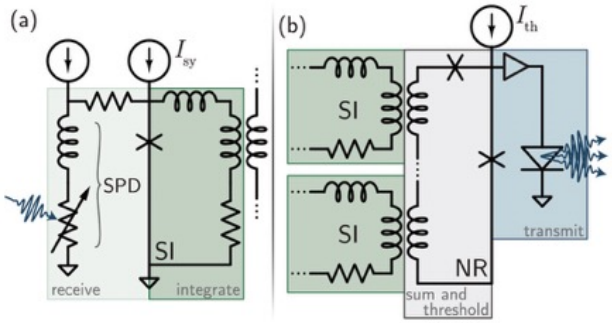
A silicon LED and waveguide coupled to a SPD



Optoelectronic neuron



Superconducting synapse and neuron cell body



J. M. Shainline *et al.,* J. Appl. Phys. 126, 044902 (2019)

J. M. Shainline *et al.,* J. Appl. Phys. Lett. 118, 160501 (2021)

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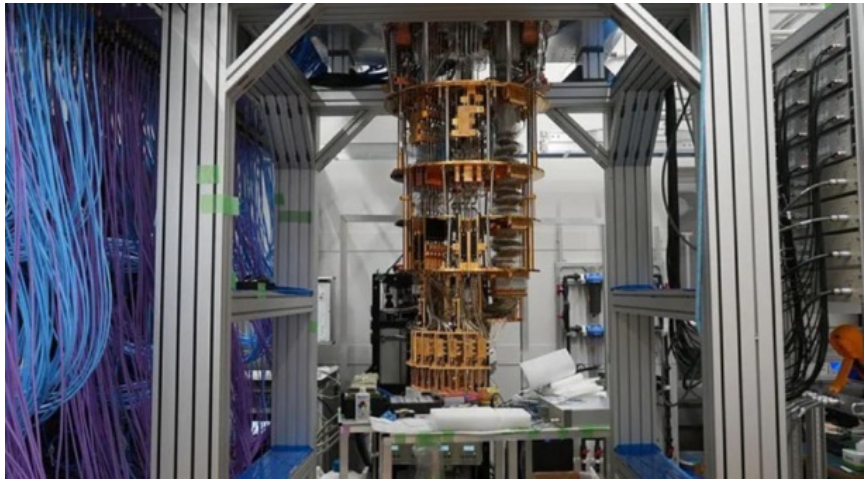
Comparison of Neuromorphic Circuits

	Biological (Brain)	Semiconductor (CMOS, memristor)	Superconductor (JJ, MJJ, SFQ)
Speed	~1 - 100s Hz (1 – 10 ms delay)	~1 – 100s MHz (~ 10 ns delay)	~10 – 100 GHz (~ 10 ps delay)
Energy/synapse	~ 10 fJ/synapse (20 W/brain)	~ pJ – 10s pJ	~ aJ or lower
Advantage	High density Massive parallelism High energy efficiency	room temp. operation Energy efficient than software Matured fab	Ultra fast Ultra low energy
Limitation	Slow	Power hungry	Cryogenic operation

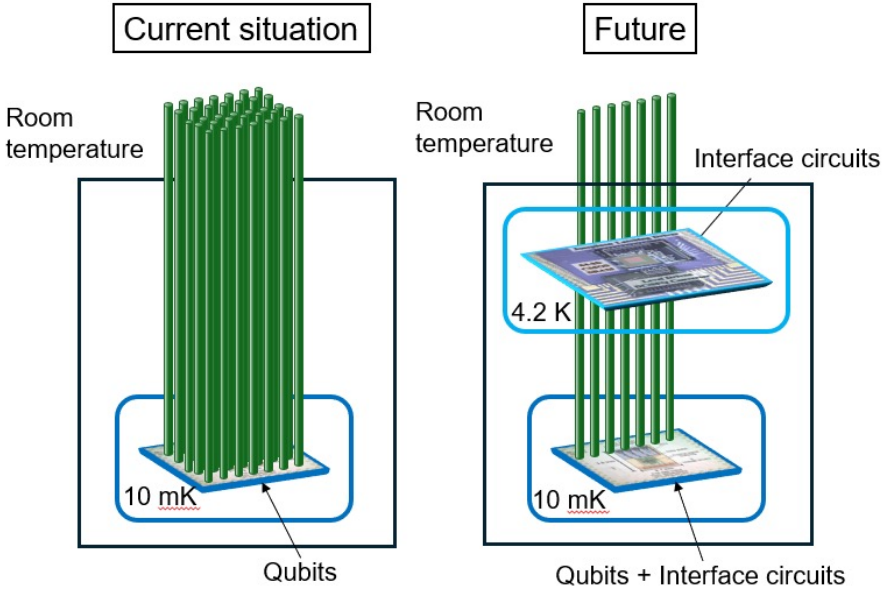
Current Issue in SC Quantum Computers

Each qubit requires 2-3 microwave lines between the mK stage and room temperature.

1000 qubits → ~2500 microwave lines



https://orient.tm/en/post/86805/Japan-launches-worlds-largest-256-qubit-quantum-computer



- Reduced wiring to room temperature
- High-speed qubit control

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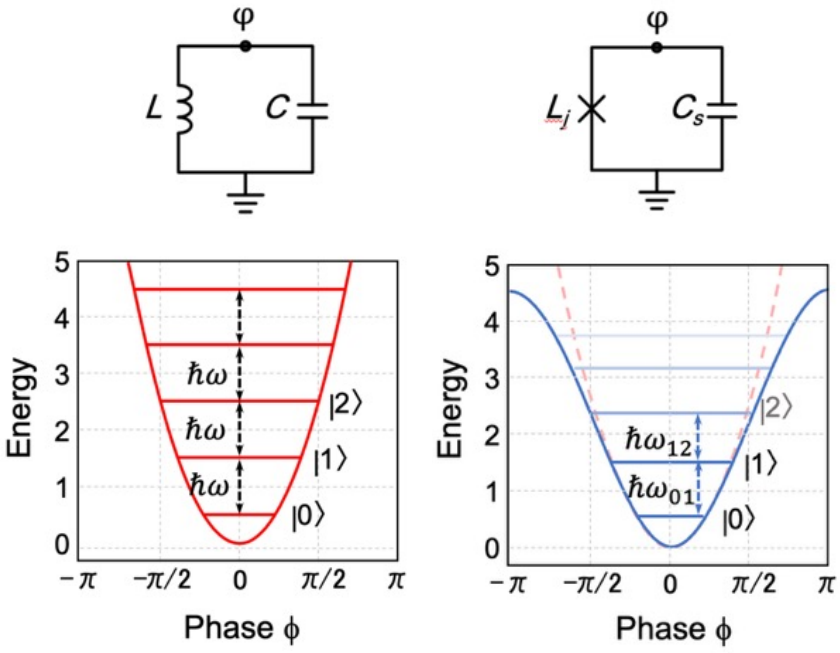
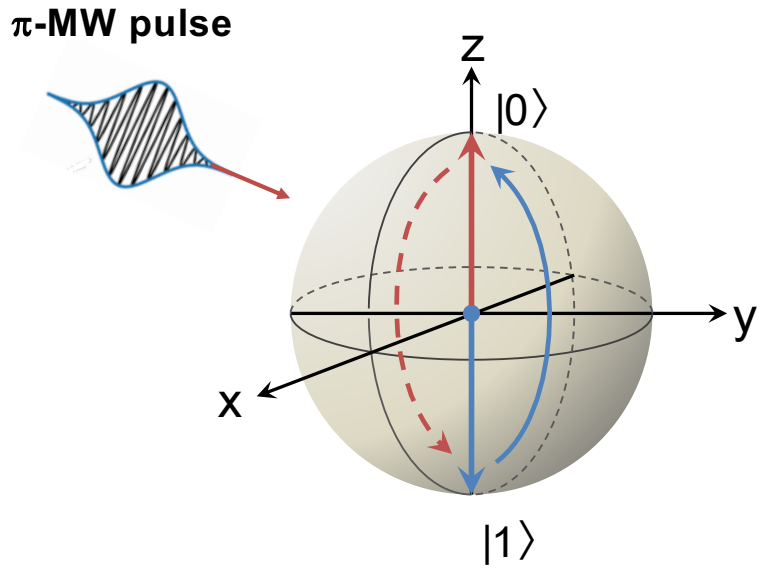
Superconducting Qubit



Quantum harmonic oscillator

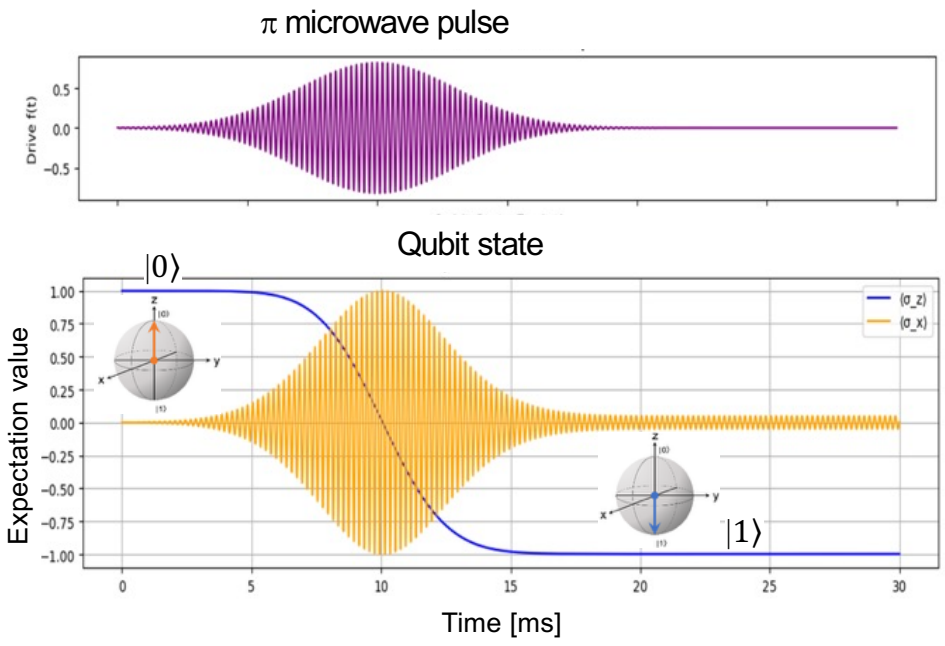
Josephson qubit



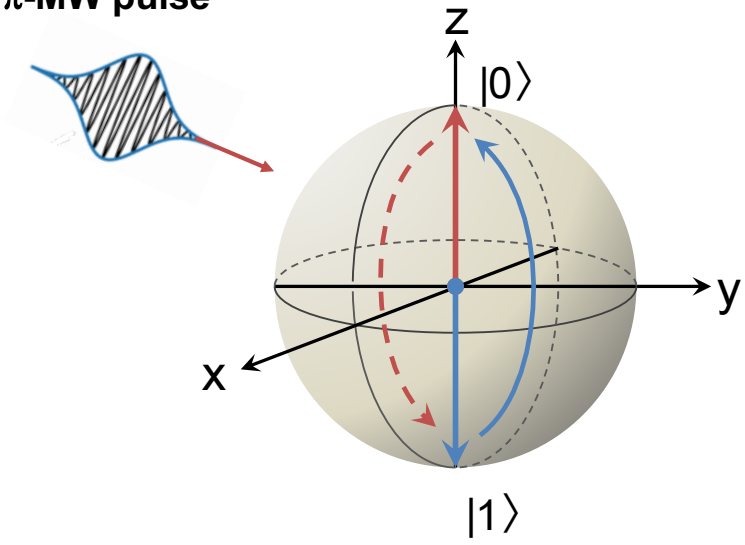
Bloch sphere and qubit states

Superconducting Qubit Irradiated with a π-MW Pulse

Qubit state control using a microwave pulse



π-MW pulse



Bloch sphere and qubit states

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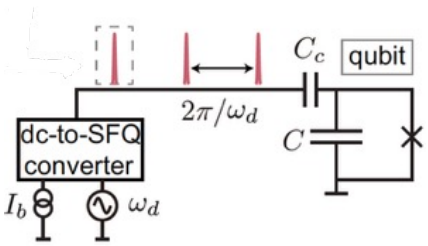
Digital Coherent Control of a Superconducting Qubit

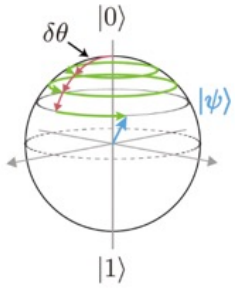
University of Wisconsin-Madison, Syracuse University

- An on-chip SFQ pulse driver integrated with a transmon qubit
- Average gate fidelity: ~95%
- Coherence limited by quasiparticle (QP) poisoning

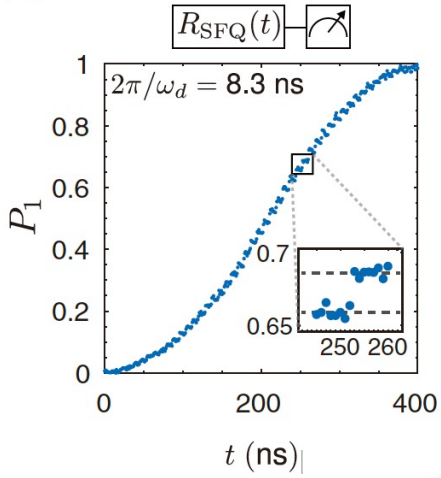
SFQ pulse driver



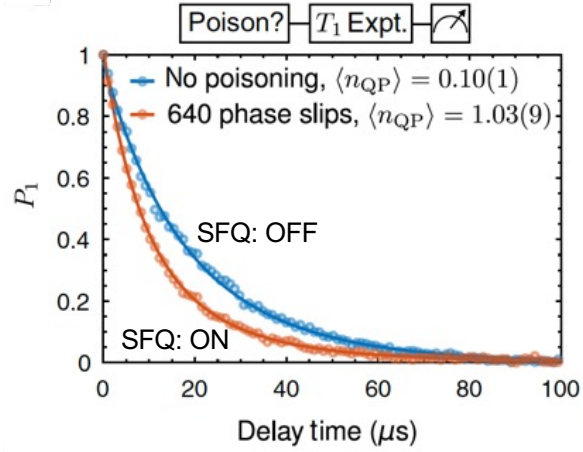
Trajectory of qubit state



Qubit-state change driven by SFQ pulses



Energy decay curve w/wo SFQ pulses



E. Leonard Jr, *et al., Phys. Rev. Applied* 11, 014009, 2019

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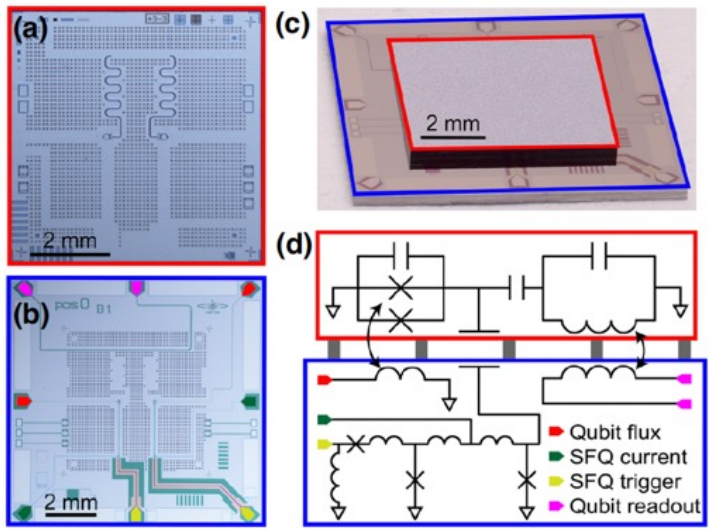
SFQ-Based Digital Qubit Control in an MCM

University of Wisconsin-Madison, Syracuse University, NIST, University of Colorado, LLNL

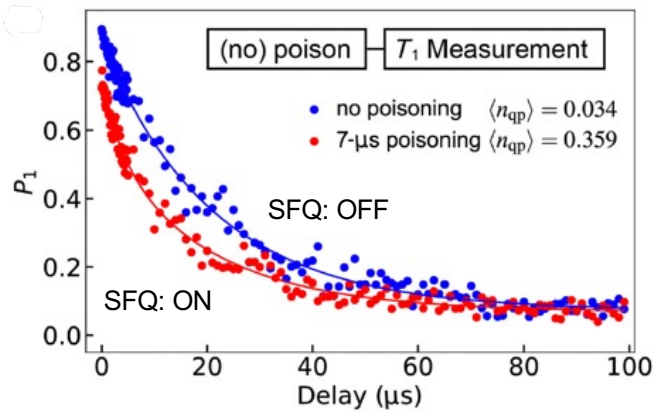
- SFQ driver and qubit on separate chips in a multichip module (MCM).
- Average gate fidelity: 98.8 % (10 x improvement).
- Residual error arising from photon-induced QP poisoning.

Quantum-classical multichip module



C. H. Liu, *et al., PRX Quantum* 4, 030310, 2023.

Energy decay curve w/wo SFQ pulses



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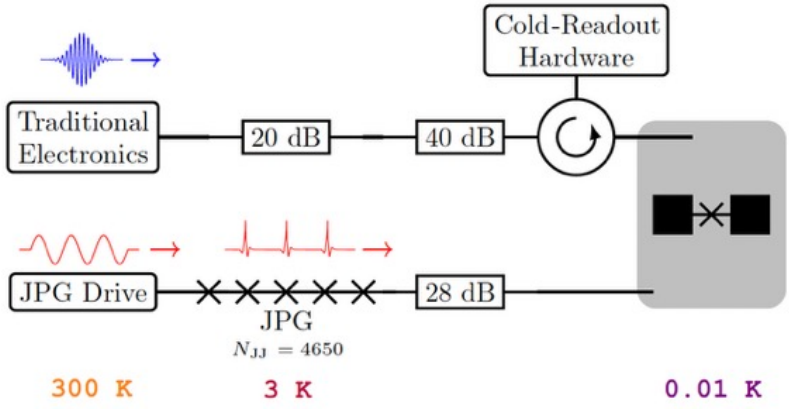
Qubit Control using a JJ Pulse Generator at 3 K

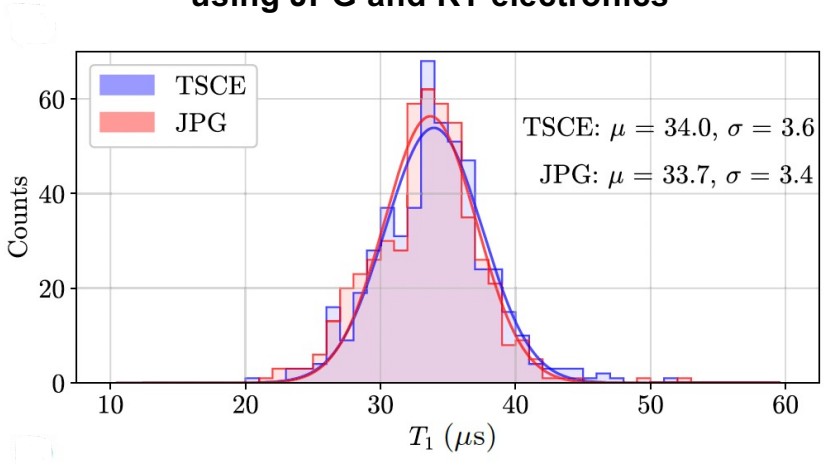
NIST, University of Colorado

- Transmon qubit controlled by Josephson pulse generator (JPG) at 3 K stage.
- Qubit lifetime T_1 comparable to room-temperature electronics.

Experimental setup



Histograms of qubit lifetime T_1 measured using JPG and RT electronics



L. Howe, *et al., PRX Quantum 3*, 010350, 2022.

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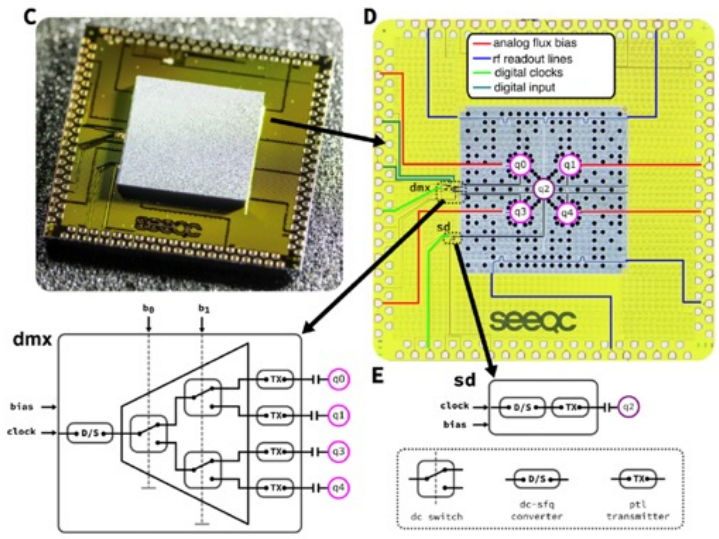
Multi-Qubit Control with SC Electronics at mK

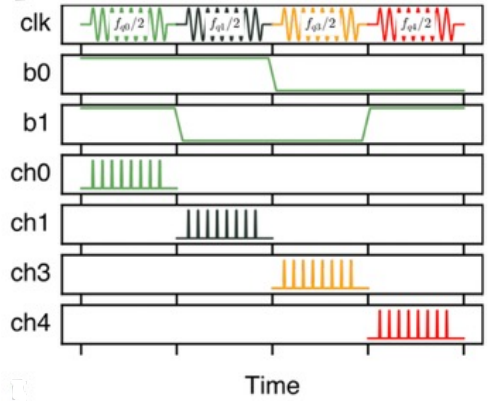
Seeqc, Inc.

- Implement digital SFQ demultiplexer with a multi-qubit system.
- Average gate fidelities: ~ 99.5%
- Power dissipation for 1-4 DMX: 9 nW

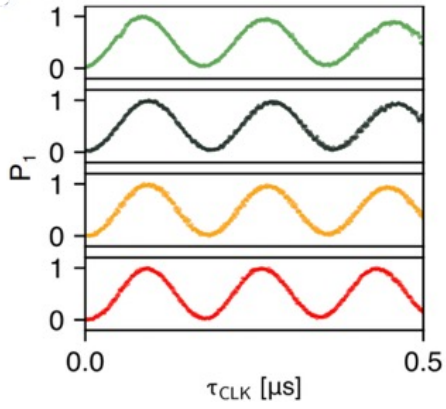
MCM composed of quantum & SFQ chips



Timing diagram of time-multiplexed qubit control



Time-multiplexed Rabi oscillations of the 4 qubits



J. Bernhardt et al., arXiv:2503.09879

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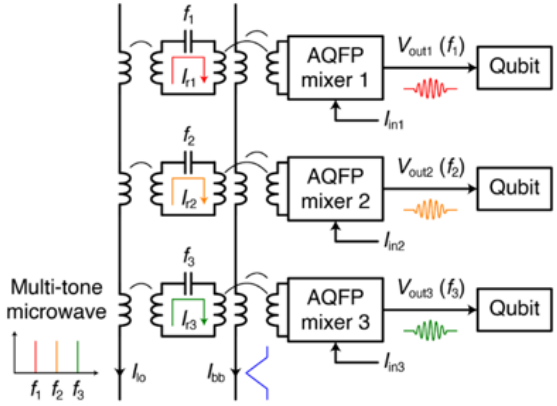
AQFP-Multiplexer for Qubit Control

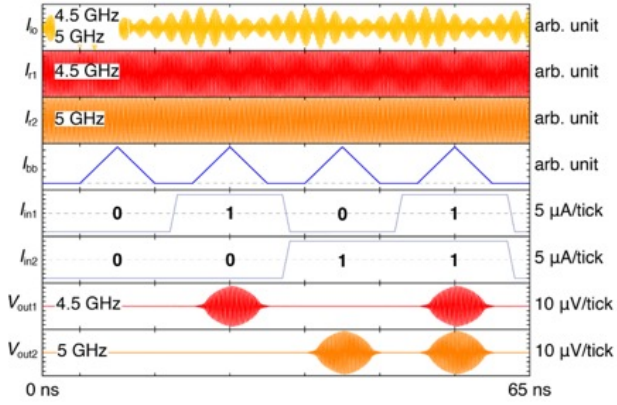
AIST, Tohoku University, NEC, Yokohama National University

- Multi-tone microwaves are multiplexed using AQFP gates
- Ultra-low-power qubit control: 81.8 pW per qubit

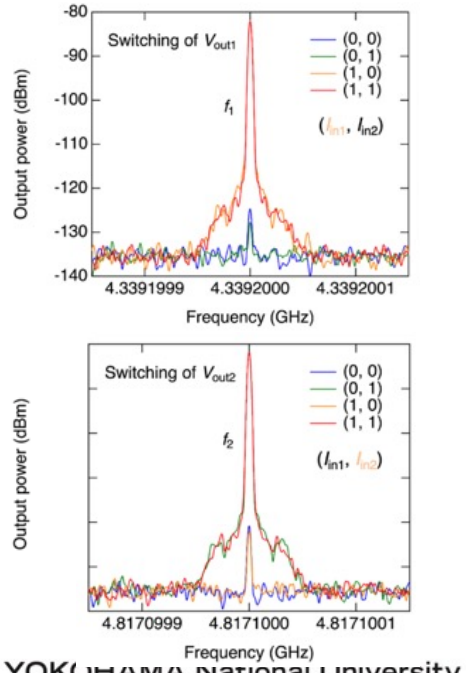
Block diagram of AQFP multiplexer



Simulated waveforms of AQFP multiplexer



Measured results at 4.2K



N. Takeuchi, *et al. npj Quantum Inf* **10**, 53 (2024).

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Comparison of Control Schemes for SC Qubits

	Room-Temp. Electronics	Cryo-CMOS	Superconducting Digital
Operating temp.	~ 300 K	3 – 4 K	10 -20 mK
Latency	High (cable delay) ~ 100 ns	Medium ~ 10 ns	Ultra-low ~ 100 ps
Power dissipation pre qubit	~10 mW – ~100 mW	~1 μW – ~10 mW	~10 pW – ~10 nW
Thermal load	Heat from many cables and attenuators	~100 mW at 4 K	~10 μW at 20 mK
Scalability	Limited by wiring	Reduce wires between 300K-4K	High scalability
Advantages	Mature & flexible	Fewer cables	Ultra-fast, ultra-low energy
Challenges	Latency & wiring bottlenecks	Power dissipation at low temp.	Integration density

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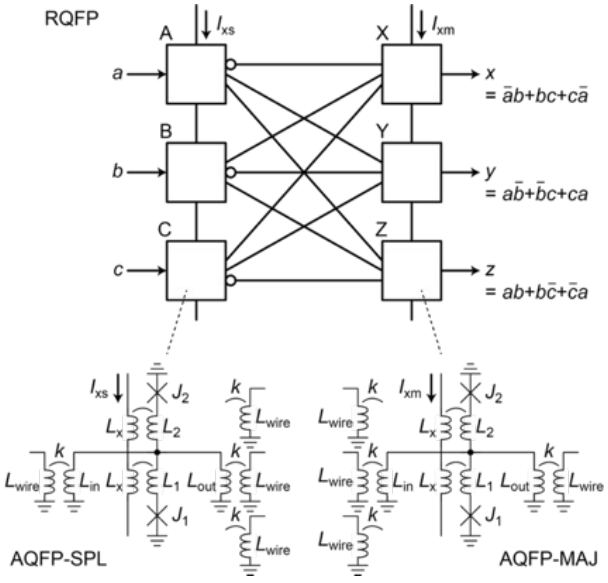
Reversible Computing

- In computation that conserve information entropy, there is no fundamental lower limit on the energy per bit.
- Landauer's principle sets a ($k_B T$ ln2) limit only when information is erased.
- Requirement to conserve information entropy :
  - Logical reversibility
  - Physical (thermodynamical) reversibility

R. Landauer, *IBM Journal of Research and Development* 5, 183 (1961).
C. H. Bennett, *IBM Journal of Research and Development* 17, 525 (1973).

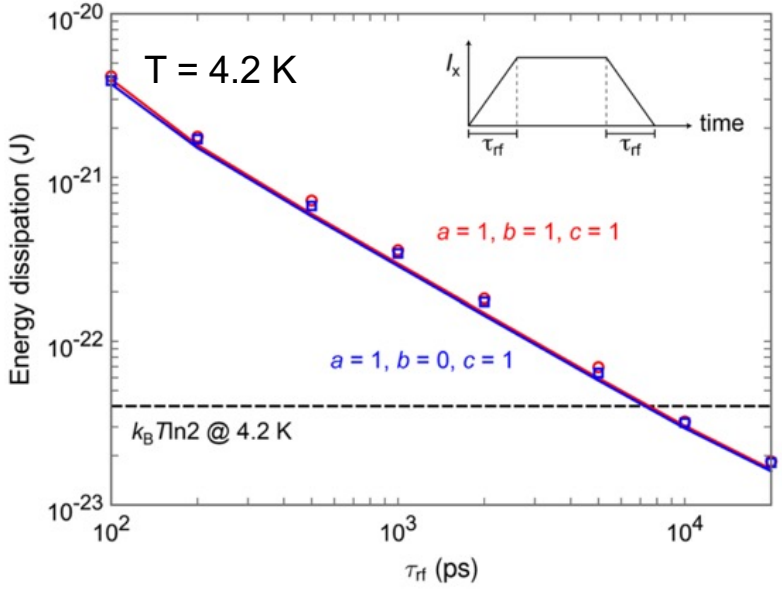
Reversible AQFP (RQFP) Logic

Reversible majority AQFP gate



A logically and physically reversible gate can be realized by AQFP.

Simulated energy dissipation vs. rise time



N. Takeuchi, *et. al*., *Scientific Reports* 4, 6354 (2014).

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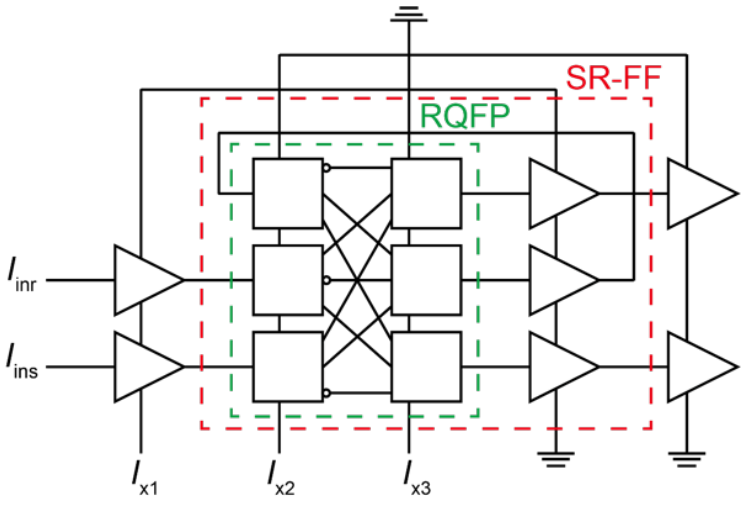
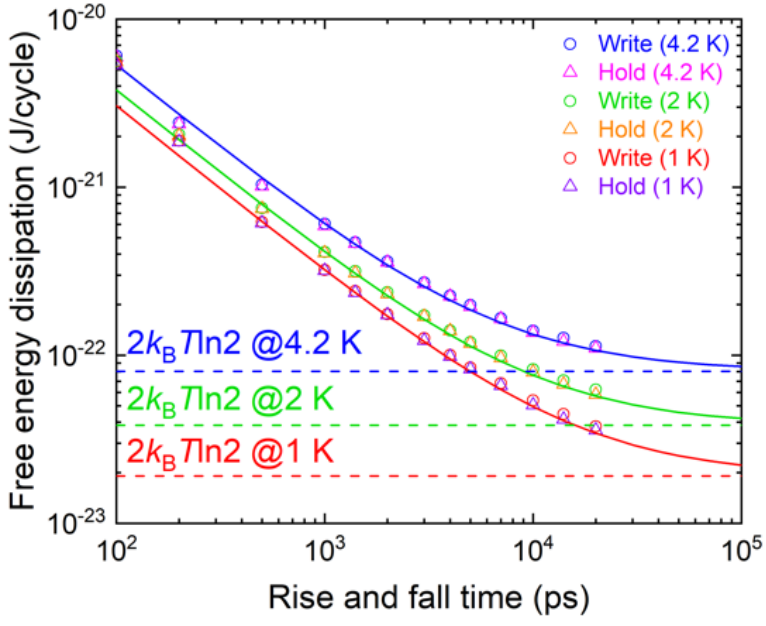
Energy Dissipation of an RQFP Flip-Flop





The energy dissipation of a reversible flip-flop approaches $2k_BT\ln2$.
⇒ The energy dissipation is determined by data erasure.

T. Yamae *et al*., J. Appl. Phys. 135, 063902 (2024).

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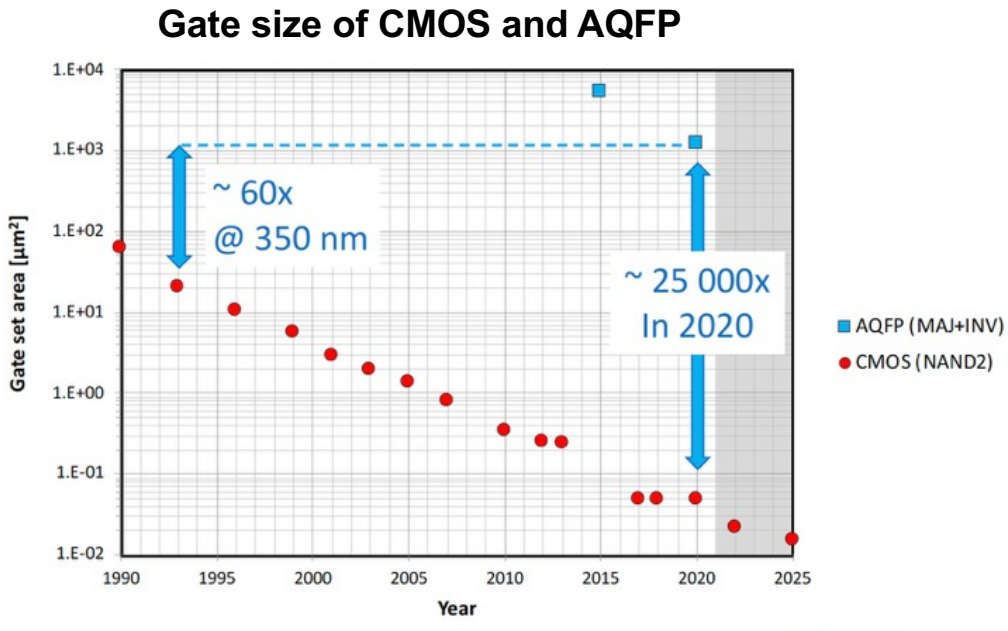
Challenge in Superconducting Digital Electronics

- Higher-density circuits and memories are needed



IRDS 2023 Update, Cryogenic Electronics and Quantum Information Processing.

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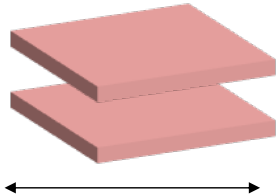
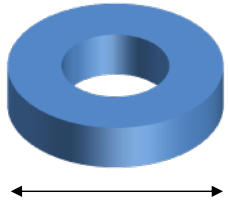
Fundamental Size of Charge- and Flux-Based Devices

Charge-based



Flux-based



Energy to store one electron $U_e = \frac{e^2}{2C} = \frac{e^2}{2\varepsilon_0\lambda_e}$

Energy to store one SFQ $U_F = \frac{\Phi_0^2}{2L} = \frac{\Phi_0^2}{2\mu_0\lambda_F}$

Equating energies ($U_e = U_F$), gives: $\frac{\lambda_F}{\lambda_e} = \left(\frac{\varepsilon_0}{\mu_0}\right)\left(\frac{\Phi_0}{e}\right)^2 = 4\left[\frac{h}{(2e)^2}\right]^2 / Z_0^2 = 4\times\left(\frac{6.45\text{k}\Omega}{377\Omega}\right)^2 \sim 1000$

Quantum resistance

Space impedance

Flux-based devices are 1000 times larger than charge-based devices since quantum resistance is much larger than the space impedance.

→ Use kinetic inductance to shrink flux-based devices.

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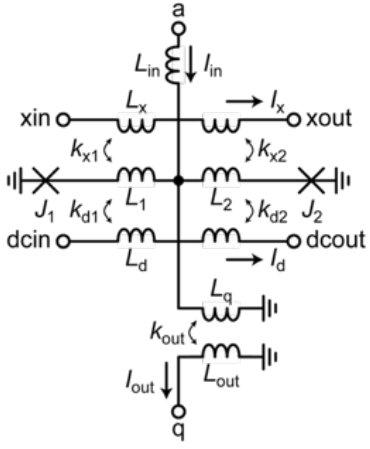
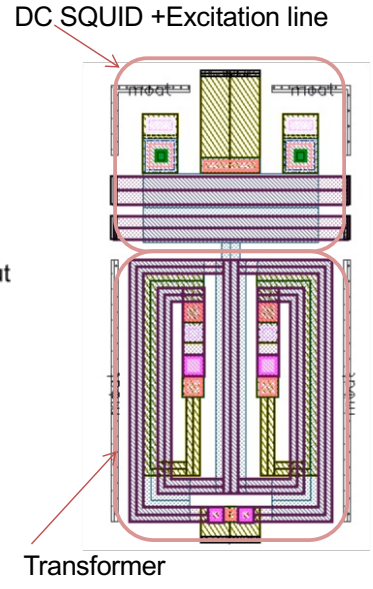
Elimination of SC Transformer from AQFP

Schematic of AQFP buffer



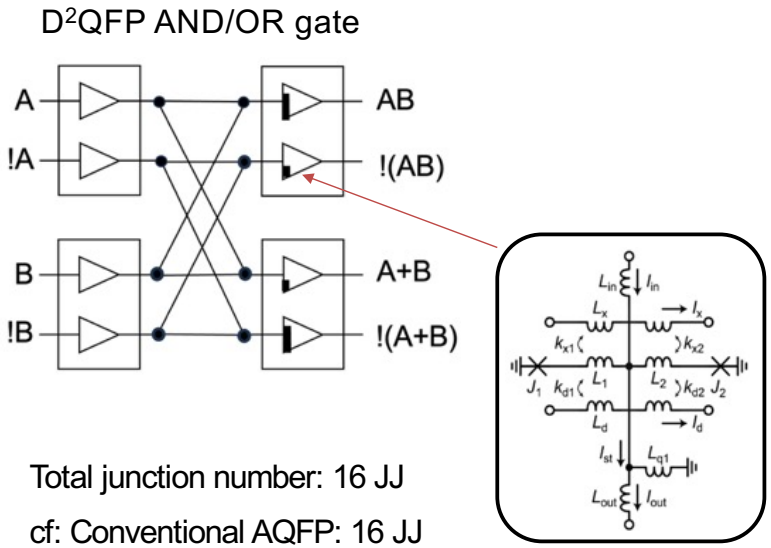
Layout of AQFP buffer



Cell size for HSTP: 20 μm x 40 μm

Designed using AIST HSTP

Dual-rail direct coupled AQFP (D²QFP) logic



Total junction number: 16 JJ

cf: Conventional AQFP: 16 JJ

N. Yoshikawa *et al., ASC2024.*

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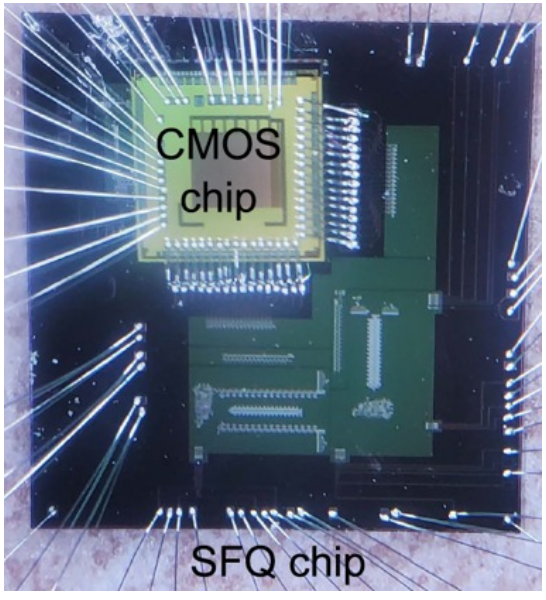
Other Activities for High-Density SC Digital Circuits

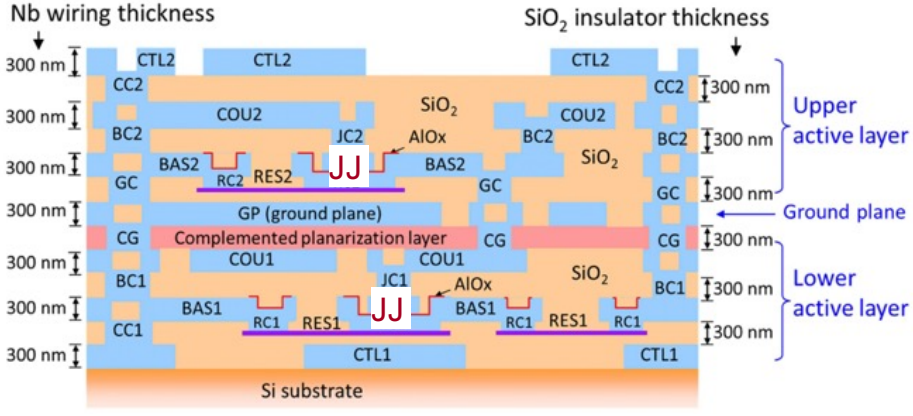
Josephson–CMOS Hybrid Memory



Readout operation at 38.4 Gb/s per channel was demonstrated.

Y. Hironaka *et al., IEEE TAS* 35, 1300109, 2025

Double-Gate-Layered Niobium Process (DGP)



3D integration will be possible to implement.

T. Ando *et al., Supercond. Sci. Technol.* 30, 075003, 2017.

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Beginning of a New Era in SDE

- **Ultra-efficient AI**
  - Zero static loss and ultra-low switching energy
  - Adiabatic and event-driven logic → much lower-power training and inference
- **Large-scale quantum computing**
  - Cryogenic control/readout with minimal heat near qubits
  - Picosecond timing and low-noise amplifiers → high-fidelity quantum gates
- **Green computing**
  - Lower energy consumption and cooling loads
  - "Cold accelerator" modules co-packaged with CMOS and photonics
- **What is needed next**
  - Higher-density circuits and memories
  - Standardized PDKs and EDA workflows