# NioCAD - Brief History and Current Activities

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***Abstract*— We introduce NioCAD, a company based in Stellenbosch, South Africa. NioCAD develops an EDA suite, called NioPulse, which is specifically designed for the superconductive electronics industry. We provide a brief history of the organisation, as well as an overview of the purpose and capabilities of NioPulse.**

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## I. INTRODUCTION

It may come as a surprise to some that there are research and development activities in the field of Superconductive Electronics (SCE) in South Africa. The number of active individuals is low and budgets are small compared with that of the rest of the developed world, but we are intent on making a positive contribution to the field.

There are primarily two SCE groups in South Africa: the Superconductivity, Advanced materials and Nano Devices (SAND) group [1] and NioCAD (Pty) Ltd [2]. SAND, which forms part of the Electrical and Electronic Engineering Faculty [3] of Stellenbosch University [4], focuses on Rapid Single Flux Quantum (RSFQ) [5][6], Complementary Output Switching Logic (COSL) [7] and hybrid digital circuits, as well as 3D parameter extraction of superconductive structures. NioCAD develops and commercialises NioPulse, an integrated suite of Electronic Design Automation (EDA) tools specifically designed for SCE integrated circuit design. NioCAD was established by researchers from Stellenbosch University, with the aim of commercialising their research.

We provide a brief history of the arrival of SCE research in South Africa and how NioCAD emerged from these beginnings. The remainder of the paper reports on the activities at NioCAD.

## II. BRIEF HISTORY

### *A. Research in Stellenbosch*

Superconductive electronics research in South Africa started in earnest in 1996, when Prof Willem Perold,

now Vice Dean of Research at the Faculty of Engineering, in Stellenbosch, returned from a sabbatical at the laboratory of Prof Theodore van Duzer [8] at the University of California, Berkeley. The resulting research group has always been small, but has over the years published numerous peer-reviewed papers in the fields of SQUIDs [9], RSFQ [10][11][12], COSL [13], ADCs [14], 3D parameter extraction [15][16], optimisation [17], EDA tools [18][19][20], cryo-packaging and High-$T_c$ manufacturing [21][22]. Test circuits have to date targeted either the IPHT [23] or Hypres [24] fabrication (foundry) processes.

Members of the group have been participating in S-PULSE [25], a European FP7 project, and attended a number of the workshops hosted by the European FLUXONICS Society [26]. In December 2009, the university became a member of the FLUXONICS Society.

Stellenbosch University, in conjunction with the Cape Peninsula University of Technology [27] and University of Pretoria [28], organised and hosted the first South African Conference on Semi- and Superconductive Technology (SACSST) [29] in Stellenbosch in April 2009. The conference is supported by the IEEE and will be hosted every two years.

### *B. Establishment of NioCAD*

In 2001, the SAND group started to explore EDA tools and techniques. These investigations were partly sparked by the limitations of the existing low-cost and free design tools. Due to the limited funding available to the group, it was difficult to purchase commercial semi-conductor tools. During this time Retief Gerber, one of the researchers, built a number of prototypes to assist with the design of circuits and to test EDA techniques. Based on the experience gained during this period, Prof Perold, Dr Coenrad Fourie and Retief Gerber started searching for funding to turn their research into a professional commercial product. With the support of InnovUS, the technology transfer company of Stellenbosch University, their efforts paid off when they were awarded a R8.1 million (approximately €870,000) grant by the South African National Research Foundation's Innovation Fund [30] to start the commercial development of an EDA tool.

The development project started in February 2007 at Stellenbosch University. By the end of the project the development team had expanded to six full-time individuals with backgrounds in electronic engineering and computer science. The team's efforts gave rise to the software package now called NioPulse.

In November 2009 NioCAD (Pty) Ltd was established to commercialise NioPulse, while continuing research and product development. This was made possible by means of a R12.5 million (approximately €1.35 million) investment from the Industrial Development Corporation [31] of South Africa. NioCAD opened offices in Stellenbosch and currently employs ten full-time staff members.

In December 2009, NioCAD became a member of the European FLUXONICS Society. Membership in FLUXONICS is viewed as important, because NioCAD aims to form strong relationships with European partners.

Basing a software development organisation in South Africa has its advantages, such as lower cost of development, but it does put one far away from the technology's international customer base. However, over the years NioCAD has built close relations with individuals and organisations in Europe, USA and Japan. The support and encouragement NioCAD has received from numerous important role-players are tremendous and fuel the team's passion to develop the best EDA suite for SCE design.

## III. NIOPULSE

### *A. Overview*

NioPulse is an integrated EDA suite, specifically designed for SCE integrated circuit design. It enables engineers to design, analyse, optimise, layout and verify analogue and digital SCE circuits, such as RSFQ circuits.

The existing SCE market is small and, in order for it to grow, advancements must be made in a number of fields, including fabrication processes, chip I/O, cryogenics, packaging and EDA tools [32]. An EDA tool may contribute by reducing the design time, reducing design errors, enabling more complex designs

and making it easier for designers that are unfamiliar with SCE to design working circuits. NioPulse aims to achieve these goals.

Currently, SCE designers use multiple custom applications and modified semi-conductor EDA tools during the various stages of the development of SCE designs [33][34]. These solutions typically consist of a number of stand-alone tools that are not always interoperable or offer only limited integration support. In contrast, NioPulse makes use of a shared data model and integrated tools that allow transparent communication between different stages of the design process. This streamlines development while ensuring data integrity and reducing the possibility of unnecessary errors creeping into a design. The suite offers fast, closed-cycle design capability and yields designs that are ready for fabrication. NioPulse is designed to be easy to learn and easy to use, with the goal of making it possible for people inexperienced with SCE technologies to rapidly design working circuits. These design requirements and goals are achieved by reducing both the complexity of the design process and the length of the product design cycle.

NioPulse is developed in Java [35] and available for Mac OS X, Linux and Windows systems. The application's foundation is a modern, modular platform that was designed to be generic and adaptable for the rapidly changing requirements of new and cutting-edge technologies.

The suite can support multiple Simulation Program with Integrated Circuit Emphasis (SPICE) and Hardware Description Language (HDL) engines, with built-in support for SPICE3F5 [36], JSim [37][38], WRSpice [39] and Verilog [40][41]. For physical layouts, the IPHT 1kA/cm$^2$ [23], Hypres 1kA/cm$^2$ and Hypres 4.5kA/cm$^2$ [24] processes are supported.

NioPulse is composed of a component designer, process designer, schematic designer, numerous circuit analysis capabilities and circuit optimisation tools. Furthermore, a physical layout designer with real-time Layout-Versus-Schematic (LVS), Electrical Rule Checking (ERC), Design Rule Checking (DRC), physical and parasitic extraction and Graphic Data System II (GDSII) [42] export capabilities is included. The suite also provides integrated scripting, parallel processing and version control for components and circuits. These functions are described in more detail in the following sections.

### *B. Component Designer*

A component is the basic building block of a circuit design and the Component Designer is used to create and modify such components. A component can contain a schematic symbol, multiple SPICE definitions, multiple HDL definitions and multiple physical layouts.

### *C. Process Designer*

The Process Designer is used to create and modify fabrication process definitions. A process definition describes layers and their properties, design rules and predefined vias. Minimum contact, minimum size, minimum spacing and minimum surround design rules are supported [23][24]. A predefined via is a parametric cell [43] that describes a convenient connection between two or more process layers that adheres to the design rules of the process.

### *D. Schematic Designer*

The Schematic Designer is used to design circuits, sub-circuits and create test benches. A circuit can be designed for simulation using SPICE, HDL or both.

The Schematic Designer can also be used to create sub-circuits, as it enables hierarchical design. NioPulse provides a generic method to support parameterised sub-circuits that are independent of the SPICE engine used.

Finally, to allow for multiple test configurations on a circuit, the Schematic Designer is wrapped in a test bench environment. A circuit's operations are tested in this environment. Depending on the circuit type, a test configuration may be set up for simulation in SPICE, HDL or both. Each configuration can test either the ideal circuit or the circuit extracted from a physical layout. The test bench environment enables design for manufacturability by allowing for the separation of the design that will be manufactured and the components that is used to test and evaluate the design.

### *E. Analysis Capabilities*

NioPulse provides basic circuit analyses methods, such as SPICE or HDL. The team is currently working on allowing mixed-technology, mixed-mode and mixed-signal simulation capabilities. Advanced circuit analysis methods such as margin, yield and yield roll-off [44] are also provided. In order for the advanced methods to work, a simple Pass-Fail (PF) analysis is used to verify correct circuit operation by tracking the phase of each Josephson junction (JJ) in the circuit over time to determine if and when the JJs switched. We are also implementing a PF analysis based on a behavioural description of the circuit [45].

### *F. Circuit Optimisation*

Optimisation is an important component of circuit design, with numerous algorithms being used by different designers [46][47][48]. NioPulse provides a generic schematic circuit optimisation framework. The framework supports multiple optimisation methods, multiple circuit evaluation measures and techniques to combine these measurements (circuit fitness values) into a single fitness measure. The optimiser allows the user to select the circuit components to optimise, select the circuit evaluation criteria to use, configure the selected criteria and select and configure the optimisation method to use. Furthermore, NioPulse provides an Application Programmers Interface (API) to enable third parties to develop their own fitness measures and optimisers.

### *G. Physical Layout Designer*

The Physical Layout Designer (PLD) is used to create physical manifestations of a schematic circuit. A layout is realised by drawing primitive components or by placing previously defined cells for predefined components or sub-circuits. Connections between layers can be generated automatically using the fabrication process' via definitions. Parametric cell [43] functionality will be provided in the near future to make layout easier and faster.

In NioPulse the netlists of a schematic circuit and physical layout are kept synchronised during the design process. This allows for real-time LVS and ERC checking. Missing connections, illegal connections, component parameters with incorrect values, *etc*., are visually indicated in real-time. The immediate feedback allows the designer to identify errors early in the design process.

DRC is performed on request from the designer and violations are visually indicated.

Extractions of physical component parameter values and parasitic components are performed from the PLD. Accurate 3D extraction is supported through FastHenry [49][50] and InductEx [15][16]. NioPulse will soon provide fast 2D extraction using LMeter [51]. A modified schematic circuit, which includes the parasitic components and uses the extracted component values, may be generated for a physical layout. The designer can simulate this circuit from a test bench and compare the functionality with that of the ideal schematic circuit.

The layout may be exported to the GDSII format. The export process ensures that the exported physical design data adheres to the specification of the GDSII format and the fabrication facility.

### *H. Scripting*

A scripting interface provides full access to all application functionality, enabling power users to automate repetitive tasks, create complete circuit designs or rapidly develop advanced features.

Through the Java Scripting Interface [52] NioPulse may support many of the popular programming languages, including Python, Ruby, JavaScript and Groovy. Python, which is popular in the scientific community, is selected as the default language.

### *I. Parallel Processing*

EDA tools require a number of operations that are processor intensive. NioPulse is designed to transparently make use of multiple processors and multiple cores (if available) for operations that may be parallelised. This includes margin analysis, yield analysis, yield roll-off analysis, circuit optimisation, physical and parasitic extraction.

### *J. Version Control*

NioPulse supports multiple versions of all stored entities, such as components and circuits. This makes it possible to create a new, possibly incompatible, version of an entity, while allowing existing designs to use the previous version. Versioning ensures that older designs remain functional while the user implements improved versions of existing components and circuits.

## IV. CONCLUDING REMARKS

We outlined how research in superconductive electronics started in South Africa, reviewed some of the previous and current research activities at Stellenbosch University and recounted how NioCAD (Pty) Ltd was established. An overview of NioPulse, an integrated suite of superconductive EDA tools for analogue and digital integrated circuit design, was provided.

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