Superconductor Electronics and the International Roadmap for Devices and Systems

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Sorrento, Italy
SCE and the International Roadmap for Devices and Systems (IRDS)

- How we got to IRDS
  - Electronics technology roadmaps
  - Rebooting Computing Initiative
- SCE (Superconductor Electronics)
  - Applications and Drivers
  - Benchmarking and Metrics
  - Technology Roadmaps
- Conclusions
Electronics Technology Roadmaps

- **1993-1997 NTRS**: National Technology Roadmap for Semiconductors

![Roadmap Table](image-url)
Electronics Technology Roadmaps

- **1993-1997 NTRS**: National Technology Roadmap for Semiconductors
- **1998-2013 ITRS**: International Technology Roadmap for Semiconductors
  - Applied Moore’s Law to integrated circuits
  - Physical scaling worked until about 2004, then cores, 3D, ...
  - 2010: First selection of post-CMOS devices

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>31</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>19.8</td>
<td>17.7</td>
<td>15.7</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>17</td>
<td>15.3</td>
<td>14.0</td>
<td>12.8</td>
</tr>
<tr>
<td>Trench width at top (nm) [A]</td>
<td>38.4</td>
<td>32.4</td>
<td>28.4</td>
<td>25.2</td>
<td>22.6</td>
<td>20.2</td>
<td>18.0</td>
</tr>
<tr>
<td>Trench sidewall angle (degrees) [B]</td>
<td>&gt;88.2</td>
<td>&gt;88.2</td>
<td>&gt;88.5</td>
<td>&gt;88.7</td>
<td>&gt;88.8</td>
<td>&gt;88.9</td>
<td>&gt;88.0</td>
</tr>
<tr>
<td>Line edge roughness (nm) [C]</td>
<td>2.4</td>
<td>1.5</td>
<td>0.8</td>
<td>0.4</td>
<td>0.2</td>
<td>0.1</td>
<td>0.0</td>
</tr>
<tr>
<td>Lgate 3σ variation (nm) [D]</td>
<td>2.65</td>
<td>2.42</td>
<td>2.21</td>
<td>2.02</td>
<td>1.84</td>
<td>1.68</td>
<td>1.53</td>
</tr>
<tr>
<td>Lgate line width roughness 3σ (nm) [E]</td>
<td>2.1</td>
<td>1.91</td>
<td>1.74</td>
<td>1.6</td>
<td>1.46</td>
<td>1.33</td>
<td>1.21</td>
</tr>
<tr>
<td>Across chip Lgate variation 3σ (nm) [F]</td>
<td>0.91</td>
<td>0.84</td>
<td>0.77</td>
<td>0.7</td>
<td>0.64</td>
<td>0.58</td>
<td>0.53</td>
</tr>
<tr>
<td>Across wafer Lgate variation 3σ (nm) [G]</td>
<td>0.55</td>
<td>0.5</td>
<td>0.46</td>
<td>0.41</td>
<td>0.38</td>
<td>0.35</td>
<td>0.32</td>
</tr>
<tr>
<td>Lot to lot Lgate 3σ (nm)</td>
<td>0.55</td>
<td>0.5</td>
<td>0.46</td>
<td>0.41</td>
<td>0.38</td>
<td>0.35</td>
<td>0.32</td>
</tr>
<tr>
<td>Dummy Gate Stack Removal Induced Lgate Variation 3σ (nm) [II]</td>
<td>0.59</td>
<td>0.55</td>
<td>0.50</td>
<td>0.45</td>
<td>0.42</td>
<td>0.37</td>
<td>0.35</td>
</tr>
<tr>
<td>Minimum measurable gate dielectric remaining (post gate etch clean) [II]</td>
<td>&gt;0</td>
<td>&gt;0</td>
<td>&gt;0</td>
<td>&gt;0</td>
<td>&gt;0</td>
<td>&gt;0</td>
<td>&gt;0</td>
</tr>
<tr>
<td>Profile control (side wall angle) [J]</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
</tr>
</tbody>
</table>
Electronics Technology Roadmaps

- **1993-1997** **NTRS**: National Technology Roadmap for Semiconductors
- **1998-2013** **ITRS**: International Technology Roadmap for Semiconductors
  - Applied Moore’s Law to integrated circuits
  - Physical scaling worked until about 2004, then cores, 3D, ...
  - 2010: First selection of post-CMOS devices
- **2014-2015** **ITRS 2.0**
  - Driver changed from scaling to applications
  - 2015: Post-CMOS map of devices
- **2016+** **IRDS**: International Roadmap for Devices and Systems
  - Opened the door to non-semiconductor technologies
  - 2017: First roadmaps expected in November
Rebooting Computing

- IEEE Rebooting Computing
  - 2013-16: 3 summits, 1 conference

- Elie Track
  - IEEE Rebooting Computing co-chair
  - IEEE Council on Superconductivity past president
  - Hypres past president

- Erik DeBenedicts
  - Sandia National Laboratories
  - ITRS Emerging Research Architectures

- Paolo Gargini
  - ITRS Chairman 1998-2016
  - Intel Fellow and Director of Technology Strategy (retired)
Rebooting Computing Summit 2
- Goal Setting

2014 May 12-14
Santa Cruz, CA

D. Scott Holmes, Ph.D.
Facilitator
IRDS Organization

- International Focus Teams (IFTs)
  - Application Benchmarking
  - More Moore
  - **Beyond CMOS**
    - Memory
    - Logic
    - Charge state variable
    - Non-charge state variable
      - Spin
      - **Cryogenic Electronics** (here?)
    - **Cryogenic Electronics** (or here?)
  - Outside System Connectivity
  - Factory Integration
  - Metrology
  - Environment, Health, and Safety
  - Yield
  - System and Architecture (prelim.)

SCE and the International Roadmap for Devices and Systems (IRDS)

- How we got to IRDS
  - Electronics technology roadmaps
  - Rebooting Computing Initiative

- SCE (Superconductor Electronics)
  - Applications and Drivers
  - Benchmarking and Metrics
  - Technology Roadmaps

- Conclusions
# SCE Applications and Drivers

<table>
<thead>
<tr>
<th>Application</th>
<th>Drivers</th>
<th>Metrics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research &amp; development</td>
<td>Quantum information processing, advanced sensors, computing, government funding</td>
<td>Foundries, process design kits, process capability, layer count, feature sizes, yield</td>
</tr>
<tr>
<td>Metrology</td>
<td>Voltage standard</td>
<td>Accuracy, precision, voltage range, frequency range (for ac)</td>
</tr>
<tr>
<td>RF signal processing &amp; control</td>
<td>RF processor</td>
<td>Clock rate, signal-to-noise ratio, bandwidth</td>
</tr>
<tr>
<td>Data pre-processing</td>
<td>DSP: digital signal processor</td>
<td>Clock rate, throughput, bits, circuit density</td>
</tr>
<tr>
<td>Network routing</td>
<td>SOC-NW: system-on-chip, networking</td>
<td>throughput</td>
</tr>
<tr>
<td>High performance computing</td>
<td>MPU-HP: microprocessor unit, high performance</td>
<td>Floating point computation, memory performance, data rate, chip area, physical volume, energy efficiency</td>
</tr>
<tr>
<td>Data center</td>
<td>Microserver</td>
<td>Integer computation, memory performance, data rate, chip area, physical volume, energy efficiency</td>
</tr>
</tbody>
</table>
SCE Benchmarking and Metrics

- Superconducting SFQ looks good based on switching energy-delay, but:
  - Refrigeration requires x400 to x5000 energy
  - Wiring + leakage losses dominate for other technologies

- Conclusions:
  - Full system evaluation is required for SFQ
  - Better metrics and figures-of-merit needed!

https://www.nsa.gov/research/tnw/tnw203/article2.shtml
Energy–Delay Metrics: 32 bit Add

- **RQL**: Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic;
  \[ J_c = 100 \text{ µA/µm}^2, \text{ 12.1 GHz} \]
  - **RCA**: ripple-carry adder
  - **STPPA**: sparse-tree parallel-prefix adder

- 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range \( I : 400–10,000 \text{ W/W} \))

Source for RQL data:
doi: 10.1109/TASC.2014.2368354 (Table I)

Added to:
doi: 10.1109/JXCDC.2015.2418033

**FIGURE 5.** Switching energy versus delay of a 32-bit adder.
Energy–Delay Metrics: 32 bit ALU

- **RQL**: Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic;
  \[ J_c = 100 \mu A/\mu m^2,\ 16.3 \text{ GHz},\ 205 \text{ fJ/op (32 bit), 402 ps} \]

- 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range \( I : 400 \text{–} 10,000 \text{ W/W} \))

Source for RQL data:
doi: 10.1109/TASC.2014.2368354 (Table I)

Added to:
doi: 10.1109/JXCDC.2015.2418033

**FIGURE 6. Switching energy versus delay of a 32-bit ALU.**
Energy–Delay Metrics: Wiring

- **RQL**: Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic, \( J_c = 100 \, \mu A/\mu m^2 \)
  - **JTL**: Josephson transmission line
    - (0.13 fJ/bit, 5.5 ps)
  - **PTL**: passive transmission line
    - (0.26 fJ/bit 0.01–20 mm, 6.5 ps)

- 4.2 K operation; energy per bit at room temperature with 1000 W/W refrigeration (range 1: 400–10,000 W/W)

  doi: 10.1109/TASC.2014.2368354 (Fig. 1)

- **Added to**: Pan, Chang, Naeemi, "Performance analyses and benchmarking for spintronic devices and interconnects," 2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), San Jose, CA, 2016. doi: 10.1109/IITC-AMC.2016.7507679

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Fig. 5. Comparison between CMOS and spintronic devices in terms of (a) wire energy versus delay
Metric: Throughput & Power Density

- **RQL**: Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic; \( J_c = 100 \mu A/\mu m^2 \), 16.3 GHz, 9950 JJs, 205 fJ/iop (32 bit), \(~5.6 \text{ mm}^2\)
  
  - 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range \( I : 400–10,000 \text{ W/W} \))

- Source for RQL data:

  - Private communication for areas (250 nm process)

- Added to (10 nm processes):

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**FIGURE 8.** Dissipated power versus computational throughput (capped at 10 W/cm²) related to a 32-bit ALU.
Metrics: Next Steps

- **Models** for devices and circuits
  - Variety of superconductor technologies (e.g., RSFQ, AQFP)
  - Core metrics: circuit area, delay, and energy
  - Scaling models

- **Metrics** for applications
  - Logic, Memory, Interconnects

- **Refrigeration**: standard multipliers (vs. operating T, capacity) and ranges
SCE Technology Roadmap

- 15+ year span
  - Current (-1)
  - Near term (0 to +7)
  - Long term (+8 to +15)
  - Will be far less detailed than for CMOS

- First roadmap for digital computing

- Key areas:
  - Foundry and fabrication processes
  - Circuit parameters
  - Design tools
  - Packaging and integration
Past roadmaps provide a base for future efforts

Balance

- Progress (distance)
- Speed of Innovation (change rate × difficulty)
Conclusions

- IRDS is a **golden opportunity** for SCE
- Your participation is encouraged!